Design Techniques for Low Power High Gain OTA Using Miller Circuit

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***Abstract*— The power consumption has become a critical issue, and hence a great attention and high importance is given to design of low voltage(LV) low power (LP) and high gain integrated circuits in last few decades. In order to achieve high performance analog circuits are usually combined with digital circuits in mixed signal systems. Opamp's are highly power hungry analog block used in large number of applications. Hence OTAs are preferred over Opamp. As technology scales down OTA design becomes more challenging since supply voltage scales down but keeping threshold voltage relatively constant. This paper deals with design of gate driven and bulk driven OTA using cadence virtuoso in 180nm technology with the supply voltage 1.6 V and 0.4 V respectively. Different performance parameter like DC gain, power consumption, transconductance, gain margin and phase margin, CMRR and unity gain bandwidth are analyzed.**

Keywords—gain, Miller OTA, gate driven, bulk driven, gain margin, phase margin, CMRR.

I. INTRODUCTION

Circuits which operate in low voltage also results in low power dissipation. In analog circuits channel length reduction and threshold voltage reduction will affect the circuit performance badly. Hence there is high requirement of analog circuit which can operate easily in reduced supply voltage. Supply voltage can be minimized if and only if all transistors operates in sub-threshold region. Bulk transconductance has small transconductance value and hence can be used for biomedical applications which operates at low frequency and low power.

There are two different categories of recognizing OTA based filters. 1) Single-output(SO) OTA using voltage mode 2) Dual (DO) or multiple output (MO) OTA using current mode [1]. Low power simple incorporated analog circuits for signal processing are very important building blocks for the biomedical devices. To achieve low cut-off frequency which is in the range of about 10 mHz to 100 Hz, a high value of capacitor and resistor or small transconductance is required. OTA based filter consumes very low power due to the fact that it can be easily biased in weak inversion. Numerous techniques such as series parallel current mirror technique, source degeneration technique, current division and cancellation method etc can be used to achieve low transconductance. The techniques such as current cancellation and attenuation can provide very low transconductance. But transistor sizing and noise are the main drawback of such systems [8]. Power efficiency is important factor in filter design. Re-configurability is another preferred feature in design of filters.

This particular paper presents a methodology to design and implement a low voltage, high gain and low power OTA. Here section II explains brief overview of gate driven and bulk driven technique and section III deals with the design of OTA using gate driven technique. The OTA design using bulk driven technique is described in section IV. Section V deals with the simulation results and in section VI final view of paper is concluded.

II. OVERVIEW OF GATE DRIVEN AND BULK DRIVEN TECHNIQUE

A MOSFET has four different terminals namely Drain (D), Source (S), Gate (G) and bulk or the body (B). The cross section of MOSFET and the symbol with different regions is shown in Fig.1. There are two different techniques by which we can design an OTA circuit. They are 1) Bulk Driven OTA 2) Gate Driven OTA. Fig.2 shows the symbol of gate driven and bulk driven NMOS circuit. In case of gate driven circuit the input is provided at the gate and the bulk is grounded. In case of bulk driven circuit the input is provided at the bulk with gate being connected to the supply voltage. In this paper we use gate driven and bulk driven technique to implement the OTA design and to compare the various characteristics of OTA. Depending on the technology such as n-well process, p-well process or twin-tub for gate driven MOSFET the bulk terminal or the body is connected to either supply voltage or ground for PMOS or NMOS respectively [6]. In order to vary the MOSFET drain current, input voltage applied at the gate terminal or the bulk terminal has to be varied for gate driven and bulk driven circuits respectively.

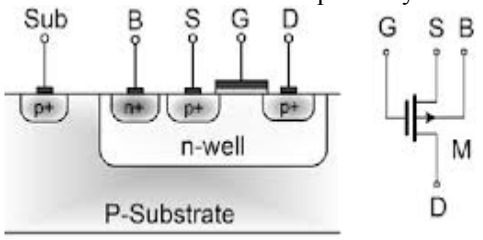

Fig. 1 (a) Cross section of MOSFET (b) Symbol of MOSFET

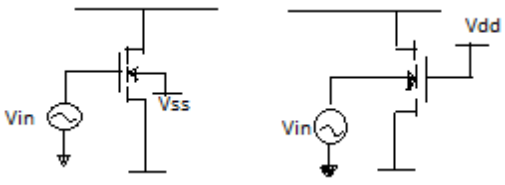

Fig. 2 (a) Gate driven NMOS (b) Bulk driven NMOS

MOSFET to operate in saturation or triode region gate to source voltage has to be greater than the threshold voltage ($V_{GS} > V_{TH}$). The drain current can be calculated as below [5].

For Triode region

$$I_{dn} = \beta_n[(V_{gs} - V_{tn})V_{ds} - \frac{V_{ds}^2}{2}] \qquad \text{(for NMOS)} \qquad (1)$$

$$I_{dp} = -\beta_p[(V_{gs} - V_{tp})V_{ds} - \frac{V_{ds}^2}{2}] \quad \text{(for PMOS)} \qquad (2)$$

For saturation region

$$I_{dn} = \beta_n \frac{1}{2}(V_{gs} - V_{tn})^2 \quad \text{(for NMOS)} \qquad (3)$$

$$I_{dp} = -\beta_p \frac{1}{2}(V_{gs} - V_{tp})^2 \quad \text{(for PMOS)} \qquad (4)$$

III. Design Of Gate Driven Miller OTA

output current of OTA is function of differential input voltage. OTA are the significant block in analog circuit design. Usually for biomedical application amplifiers with low voltage and high gain are required. Fig. 3 shows the schematic outline of two stage OTA using gate driven technique [5].

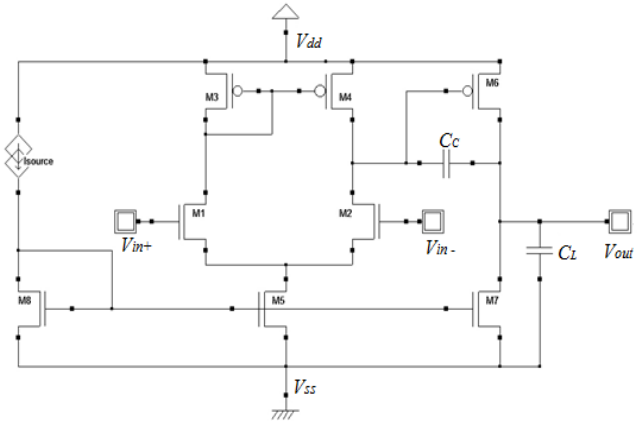

Fig. 3 Circuit outline of two stage OTA

Following parameters are used for the design of OTA.

- Load Capacitance (C_L)
- Slew Rate (SR)
- Output Voltage
- Phase Margin
- Gain Margin
- Power Dissipation (P_d)
- Gain Bandwidth (GB)

Design steps for proposed OTA are as follows:

1. Minimum value for coupling capacitor has to be selected from the preferred phase margin. For phase margin of value 60° we select
$$C_c > 0.22C_L \qquad (5)$$

2. Tail current at M_5 has to calculated using
$$I_5 = SR \cdot C_c \qquad (6)$$

3. Using the requirement specification of maximum input voltage S_3 has to be designed
$$S_1 = S_3 = \frac{I_5}{K_3\{V_{dd} - V_{in(min)} - |V_{to3(max)}| + V_{t1(min)}\}^2} \qquad (7)$$

4. Let g_{m3} be the transconductance of M_3. Check that $C_{gs3} = C_{gs4} = (0.67\ W_3\ L_3\ C_{ox})$ should be greater than 10GB.
$$\frac{g_{m3}}{2C_{gs3}} \geq 10GB \qquad (8)$$

5. Let g_{m1} be the transconductance of transistor M_1. The aspect ratios S_1 and S_2 are designed to attain required gain bandwidth GB.
$$g_{m1} = GB \cdot C_c \qquad (9)$$
$$S_2 = S_4 = \frac{{g_{m1}}^2}{2K_1 \cdot I_5} \qquad (10)$$

6. To design S_5 first $V_{d5(sat)}$ is calculated then S_5 is designed using minimum input voltage.
$$V_{ds5(sat)} = V_{in(\min)} - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{t1(\min)} \geq 100\ mV \qquad (11)$$
$$S_5 = S_8 = \frac{2I_5}{K_5[V_{ds5(sat)}]^2} \qquad (12)$$

7. Let g_{m2}, g_{m4}, g_{m6} be the transconductance of M_2, M_4, M6 transistors.
$$V_{gs4} = V_{gs6} \qquad (13)$$
$$g_{m6} = \frac{2.2g_{m2} \cdot C_L}{C_C} \qquad (14)$$
$$S_6 = \frac{g_{m6} \cdot S_4}{g_{m4}} \qquad (15)$$
$$I_6 = \frac{S_6}{S_4} I_4 \qquad (16)$$

8. The aspect ratio of M_7 can be calculated using below equation.
$$S_7 = \frac{I_6 \cdot S_5}{I_5} \qquad (17)$$

9. Using the below equation power desipation can be calculated.
$$P_{diss} = (I_5 + I_6)V_{dd} \qquad (18)$$

10. The circuit is simulated to check if all the required specifications are met. Aspect ratio of transistors from M_1 to M_8 is represented by S_1 to S_8.

Gate driven OTA is designed and simulated with Cadence virtuoso simulation tool with supply of 1.6 V at 180 nm CMOS technology. The schematic diagram of gate driven OTA for differential mode and common mode with supply of 1.6 V at 180 nm CMOS technology is shown in Fig.4 and Fig.5 respectively. Different parameters such as gain margin, phase margin, power dissipation, CMRR, Slew rate, unity gain bandwidth are calculated for the same.

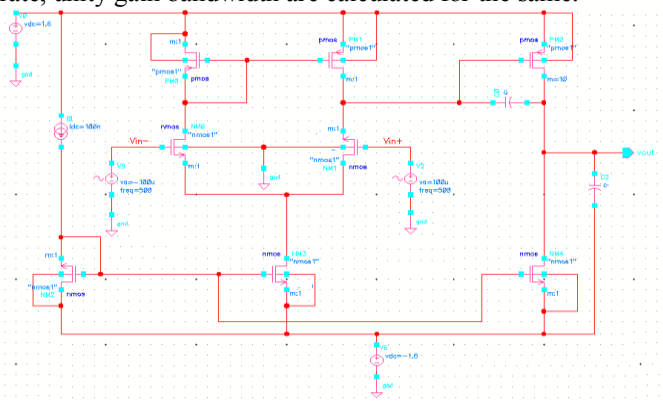

Fig. 4 Schematic of Gate driven OTA with differential mode inputs

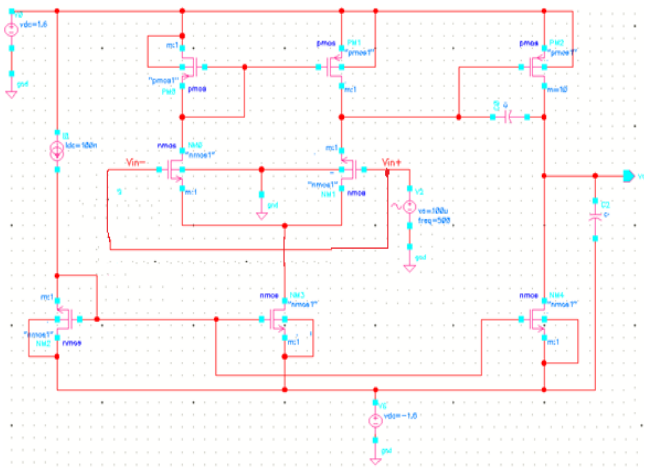

Fig. 5 Schematic of Gate driven OTA with common mode inputs

The input stage is a differential amplifier with PMOS transistors as active load in gate driven Miller OTA. Gate driven technique provides high Common mode rejection ratio and high gain. Gate driven voltage to current transconductor is based on square law I-V characteristics of the MOSFET in the saturation region, provided all MOSFET's are perfectly matched transistors and channel length modulation is absent. The second stage is a common source amplifier which provides the gain [2].

IV. Design of Bulk Driven Miller OTA

Bulk driven technique is most common technique to achieve power reduction. In MOS circuit design many a times the bulk terminal is ignored by just connecting it the ground or supply [6]. Main advantage of bulk driven technique is that it requires very low threshold value than the gate driven technique.

Bulk driven OTA is designed and simulated with Cadence virtuoso simulation with supply of 0.4 V at 180 nm CMOS technology. The schematic diagram of bulk driven OTA for differential mode and common mode with supply of 0.4 V at 180 nm CMOS technology is shown in Fig.6 and Fig.7 respectively. Different parameters such as gain margin, phase margin, power dissipation, CMRR, Slew rate, unity gain bandwidth are calculated for the same.

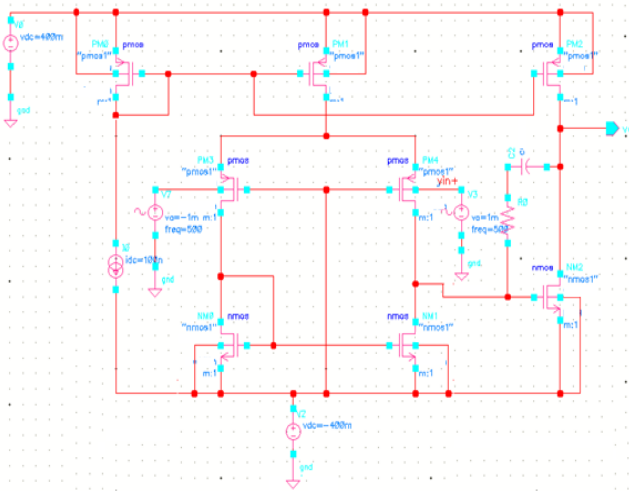

Fig. 6 Schematic of Bulk driven OTA with differential mode inputs

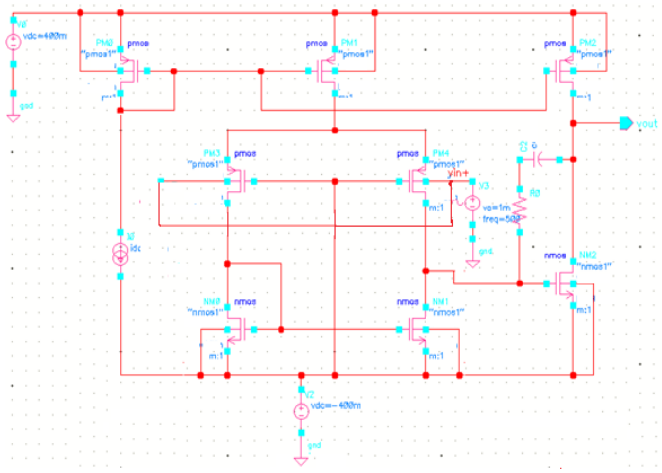

Fig. 7 Schematic of Bulk driven OTA with common mode inputs

In nanometer scale CMOS technology Bulk driven Miller technology helps to overcome the issues of low transconductance and low output impedance. Bulk driven Miller OTA consists of two stages. First stage consists of PMOS input transistor and current mirror which acts as an active load. The second stage acts as gain boosting stage and it consists of simple common source amplifier with the two transistors [4]. Miller compensation capacitor C_C helps to stabilize the amplifier. The load capacitor C_L is connected as shown. Bias current is provided for the first and second stage of the OTA.

V. Simulation, Analysis and Results

A. Gate Driven Technique

The proposed gate driven OTA is implemented using Cadence virtuoso 180 nm CMOS technology with 1.6 V supply voltage. The transient response of the circuit with differential inputs is shown in Fig. 8 and the gain and phase margin is shown in Fig. 9. In Fig. 10 AC response of gate driven Miller OTA with common mode inputs is shown. DC sweep error and the power curve for gate driven Miller circuit are shown in Fig. 11 and 12 respectively.

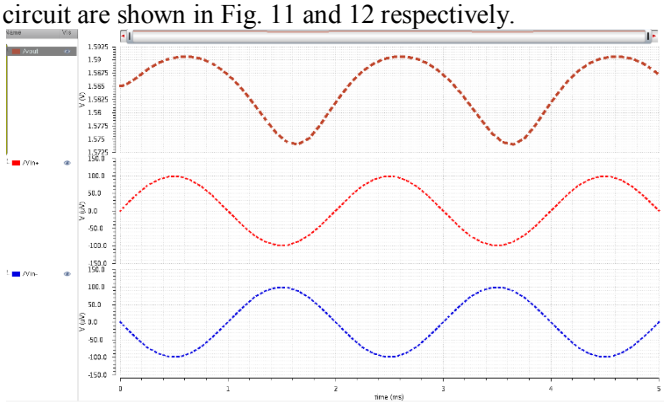

Fig.8 Transient response of gate driven Miller OTA with differential inputs

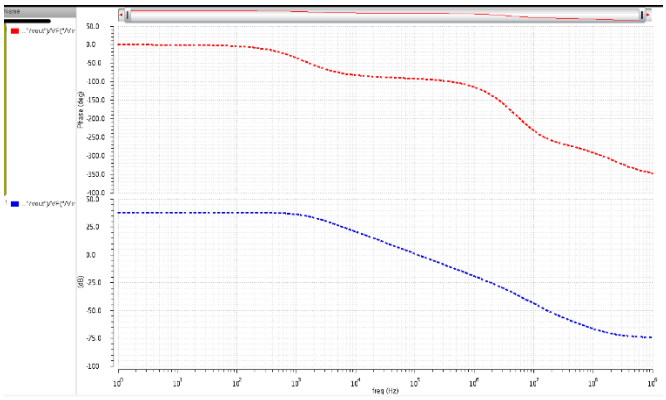

Fig.9 Gain and phase margin of gate driven Miller OTA

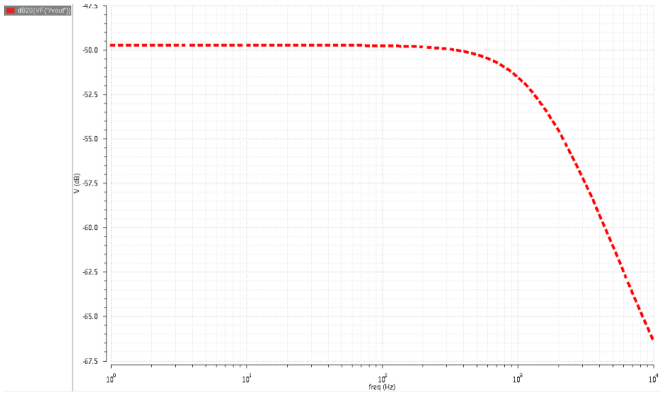

Fig.10 AC response of gate driven Miller OTA with common mode input

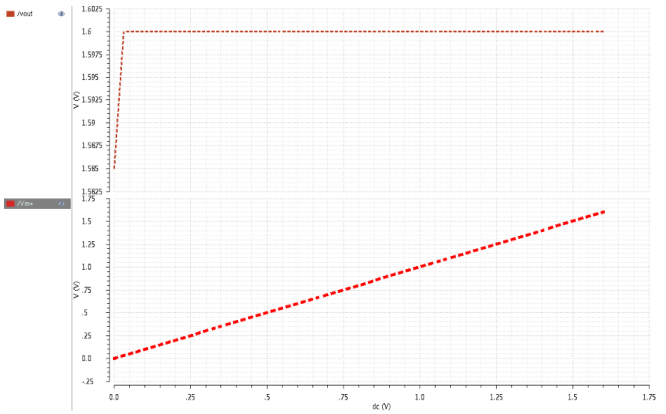

Fig.11 DC sweep error of gate driven Miller OTA

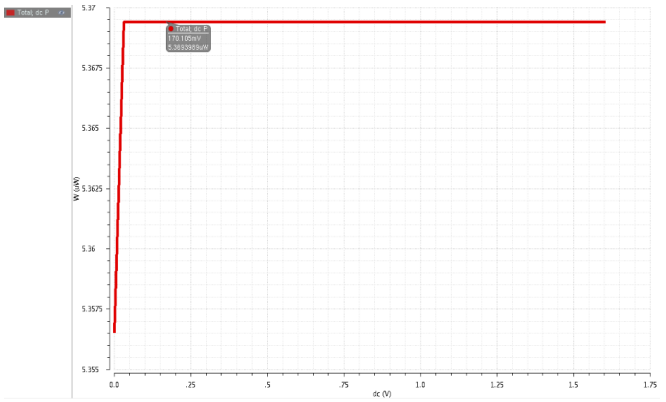

Fig.12 Power curve of gate driven Miller OTA

Transient response of gate driven Miller OTA is shown in Fig.8. For ±80 mV peak to peak of input, output swing of 15 mV is obtained. The curve of DC sweep error gives the linearity behavior of the circuit and it is found to be linear from 0 to 1.6 V. The DC gain of Gate driven Miller OTA is 41.53 dB. As shown in Fig. 9, Gain and phase margin are observed to be 33.32 dB and 81°. From Fig. 10, the common mode gain of 49.73 dB can be observed. Unity gain bandwidth of the circuit is seen to be 148.8 kHz and high CMRR of 91.27 dB is obtained. Average power consumption of 5.36 µW can be observed fron the Fig. 12.

B. Bulk Driven Technique

The proposed bulk driven OTA is implemented using Cadence virtuoso 180nm CMOS technology with 0.4 V supply voltage. The transient response of the circuit with differential inputs is shown in Fig. 13 and the gain and phase margin is shown in Fig. 14. In Fig. 15 AC response of bulk driven Miller OTA with common mode inputs is shown. DC sweep error and the power curve for bulk driven Miller circuit are shown in Fig. 16 and 17 respectively.

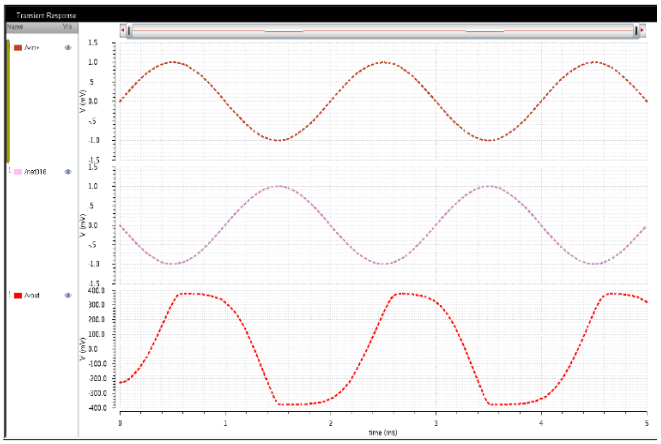

Fig.13 Transient response of bulk driven Miller OTA with differential inputs

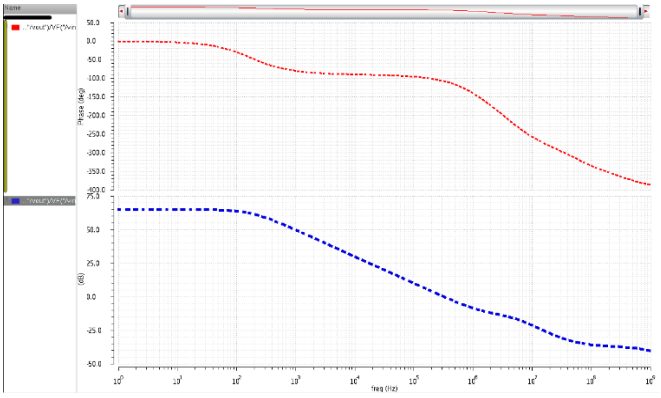

Fig.14 Gain and phase margin of bulk driven Miller OTA

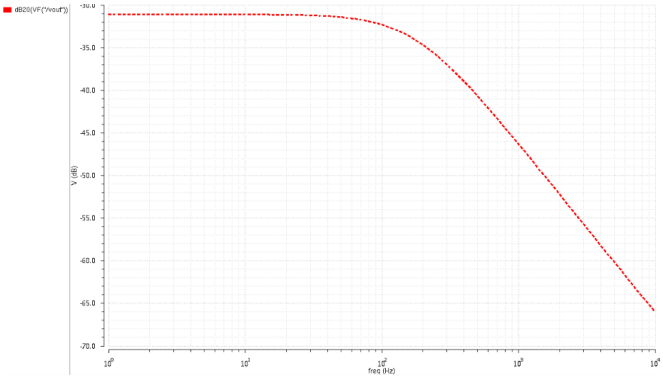

Fig.15 AC response of bulk driven Miller OTA with common mode input

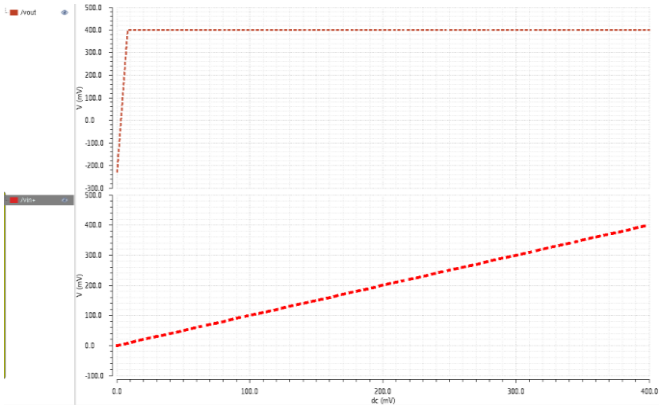

Fig.16 DC sweep error of bulk driven Miller OTA

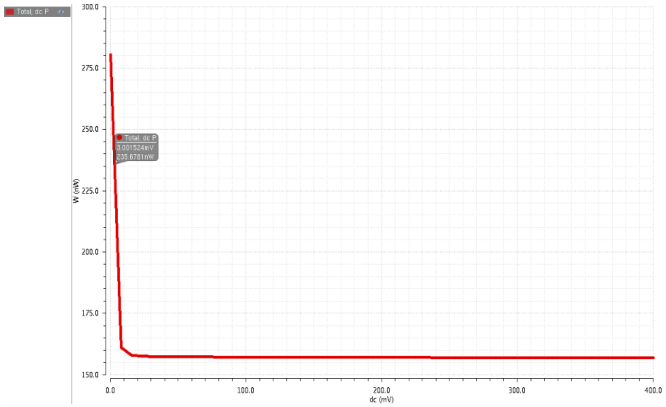

Fig.17 Power curve of bulk driven Miller OTA

Transient response of bulk driven Miller OTA is shown in Fig.11. For ±1 mV peak to peak of input, output swing of ±1 mV is obtained. The curve of DC sweep error gives the linearity behavior of the circuit and it is found to be linear from 0 to 0.4 V. The DC gain of Gate driven Miller OTA is 57.04 dB. As shown in Fig. 12, Gain and phase margin are observed to be 61.13 dB and 50.3°. From Fig. 13, the common mode gain of 31.09 dB can be observed. Unity gain bandwidth of the circuit is seen to be 126 kHz and high CMRR of 88.66 dB is obtained. Average power consumption of 158.4 nW is observed from the Fig.17.

Table 1 shows summary of simulated results for the gate and bulk driven OTA is proposed. From the comparison of gate and bulk driven Miller OTA circuit it is noted that the power consumption of bulk driven Miller circuit is very less and in terms of nano-Watts. Along with the low power high gain is also achieved in bulk driven Miller circuit than the gate driven equivalent. But high CMRR and better phase margin is obtained for gate driven Miller OTA.

TABLE I SUMMARY OF SIMULATED RESULTS FOR PROPOSED OTA

Specification	Gate Driven Miller OTA	Bulk Driven Miller OTA
V_{DD}(V)	1.6	0.4
I_{BIAS} (nA)	100	100
Bandwidth(kHz)	5.47	0.176
Gain margin(dB)	33.32	61.13
Phase margin	81°	50.3°
UGBW(kHz)	148.8	126
Gain BW product(kHz)	228.4	125.6
Common mode gain(dB)	49.73	31.09
DC gain(dB)	41.53	57.04
CMRR(dB)	91.27	88.16
Power (nW)	5.36	0.1584

VI. CONCLUSION

Power and voltage are the two significant constraints in the field of analog and mixed mode signals and systems in today's world. Implementation and simulation of gate driven and bulk driven OTA is designed in this paper using Cadence virtuoso in 180nm CMOS technology. Gate driven circuit is operated at supply of 1.6 V and for bulk driven technique a low voltage of 0.4 V is supplied. Bulk driven technique results in very low power consumption and high gain is obtained compared to gate driven circuit. In case of gate driven circuit high CMRR can be achieved. As technology scales down further the CMRR can be improved by using appropriate gain boosting technique. Deep understanding of circuit topologies and a careful circuit analysis and device operations can lead to additional optimization of performance parameter of the OTA.

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