Design Considerations on CMOS Bulk-Driven Differential Input Stages

Juan M. Carrillo, J. Francisco Duque-Carrillo

Dpto. de Ing. Eléctrica, Electrónica y Automática
Universidad de Extremadura
Avda. de Elvas s/n, 06006 Badajoz, Spain
E-mail: jmcarcal@unex.es

Guido Torelli

Dip.to di Ingegneria Industriale e dell'Informazione
Università di Pavia
Via Ferrata 1, 27100 Pavia, Italy
E-mail: guido.torelli@unipv.it

Abstract—**Design considerations regarding the DC behaviour of CMOS bulk-driven differential input stages are addressed in this paper. Unlike in conventional gate-driven circuits, the input terminal of a bulk-driven transistor consists of a *pn* junction, whose real behaviour is critical to determine the input performance of the overall circuit. In this work, the simulated and experimental performance of a bulk-driven differential pair are illustrated and compared in order to draw design hints. The conclusions drawn are applied to the design of a low-voltage bulk-driven voltage-to-current converter in 0.35-μm standard CMOS technology.**

Keywords-bulk-driven MOS transistors; CMOS analog integrated circuits; low-voltage; voltage-to-current converter

I. INTRODUCTION

The fast down scaling of device sizes as well as the demand for lower and lower power consumption have forced the decrease of the total supply voltage of modern CMOS integrated circuits. Nevertheless, noise sources have substantially remained unchanged. As a consequence, wide voltage swing has become an important feature in most analog applications, in order not to limit the signal to noise ratio (SNR) [1]. In practice, this requirement results in the need for a high common-mode (CM) [1] and/or differential-mode (DM) [2] input voltage range. As the reduction of the transistor threshold voltage is not being proportional to the supply voltage decrease, novel solutions have to be developed to meet the required large input voltage ranges.

Figure 1(a) illustrates a conventional gate-driven PMOS differential pair. The input signal is applied to the gate of transistors MG1 and MG2, whereas their bulk terminals may be connected either to the supply voltage V_{DD} or to the common source terminal of the pair when an *n*-well technology is used. The minimum supply voltage required for proper operation of this basic building block is:

$$V_{DD} \geq V_{SG} + \left|V_{DSat}\right| + V_{Signal} \approx \left|V_{TH}\right| + 2\left|V_{DSat}\right| + V_{Signal} \quad (1)$$

where V_{SG}, V_{DSat}, and V_{TH} are the quiescent source-to-gate voltage, the minimum drain-to-source saturation voltage, and the threshold voltage of a PMOS transistor, respectively, and V_{Signal} stands for the peak amplitude of the input signal. In the presence of a low-voltage supply ($V_{DD,min} \sim V_{SG} + V_{DSat}$), the
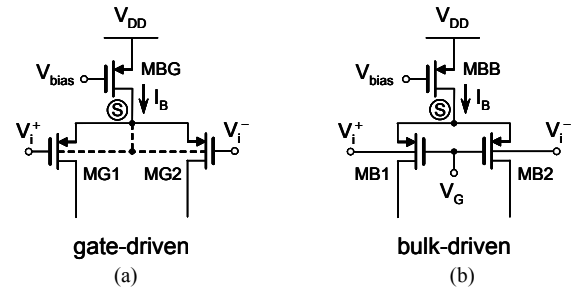
Figure 1. (a) Gate-driven and (b) bulk-driven PMOS differential pairs.

allowed room for the signal is very much reduced. Besides, in the case of a PMOS differential pair, the available input voltage range is restricted to the region close to the negative supply.

A suitable solution to obtain a wide input CM swing in a low-voltage environment is based on the use of bulk-driven MOS transistors [3], as illustrated in Fig. 1(b). With this approach, the input CM voltage range of the differential pair is extended, as the voltage constraint represented by V_{TH} is removed from the signal path. The main drawback of using bulk-driven transistors is that the bulk transconductance (g_{mb}) is smaller than the gate transconductance (g_m) by a factor from 2 to 5, depending on the fabrication technology used. This fact leads to lower amplifier gain and gain-bandwidth product, along with other limitations associated to a reduced input transconductance, such as higher input referred noise and offset voltage [3, 4]. Nevertheless, the value of the effective transconductance ($g_{m,eff}$) of a bulk-driven input stage may be increased with the help of appropriate circuit techniques [5].

The source-bulk *pn* junction of input devices MB1 and MB2 in Fig. 1(b), that in conventional gate-driven transistors is never forward biased, goes from reverse to forward operation when the input voltage signals (V_i^+, V_i^-) move from V_{DD} to ground. Therefore, the study of the performance of a bulk-driven differential pair over the input CM and DM voltage ranges is important when the amplifier is required to feature wide input swing capability. Circuit simulation in the design phase can greatly help in this respect, provided that its results are reliable over the whole input voltage range. In this paper, the DC behaviour of a bulk-driven differential pair as a function of input CM and DM signals ($V_{i,cm}$ and $V_{i,dm}$ respectively) is experimentally characterized and compared to the simulated behaviour using a level 53 MOS BSIM3v3 model.
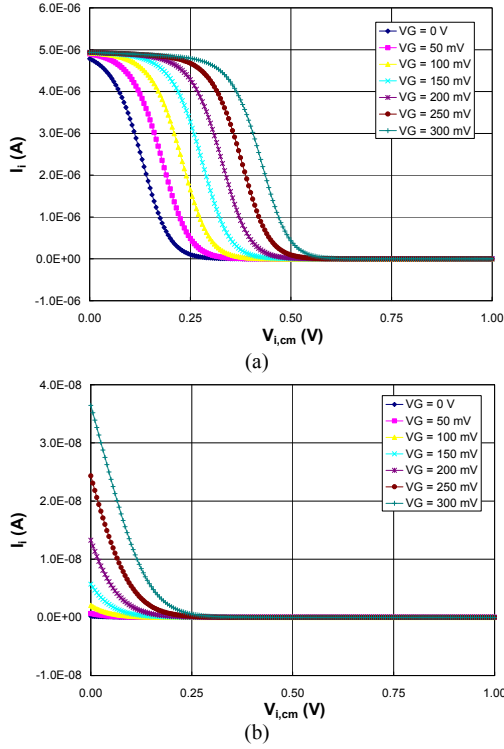
Figure 2. Input current of the bulk-driven differential pair as a function of $V_{i,cm}$ for different values of V_G: (a) simulations and (b) measurements.
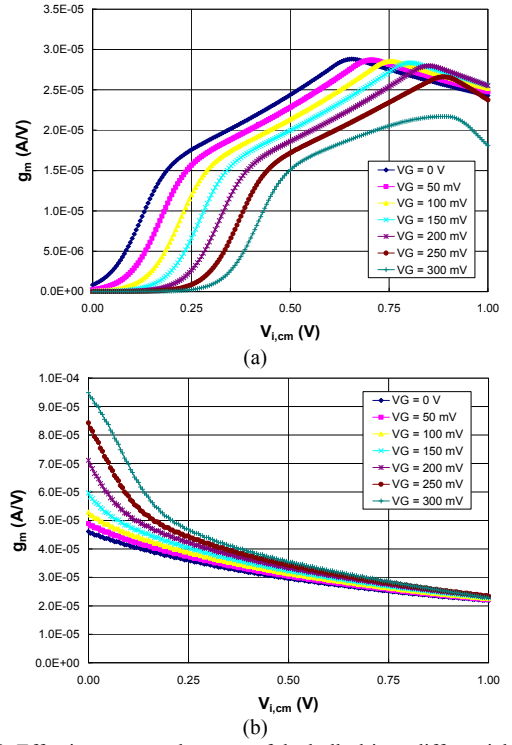

Figure 3. Effective transconductance of the bulk-driven differential pair vs. $V_{i,cm}$ for different values of V_G: (a) simulations and (b) measurements.

II. CMOS BULK-DRIVEN INPUT DIFFERENTIAL STAGE

In the bulk-driven approach, Fig. 1(b), the input signals (V_i^+, V_i^-) are applied to the bulk terminals of transistors MB1 and MB2, whereas the gate terminals of these devices are biased with a suitable level V_G in order form the channel. A PMOS realization has been selected since an *n*-well fabrication technology is considered. The drain current of an MOS transistor depends on the value of the threshold voltage, which for a *p*-channel device can be expressed as

$$|V_{TH}| = |V_{TH0}| + \gamma \cdot \left[\sqrt{2|\phi_F| + V_{BS}} - \sqrt{2|\phi_F|}\right] \qquad (2)$$

where V_{TH0} is the value of the threshold voltage V_{TH} when the body-to-source voltage V_{BS} is zero, γ is the body effect parameter, and ϕ_F is Fermi potential. The operation of a bulk-driven device is based on the body effect, that is, on the dependence of V_{TH} on V_{BS}. Indeed, I_D changes when changing V_{BS} and, hence, a transconductance function between the bulk voltage and the drain current is achieved.

A. Common-mode voltage behaviour

When a CM signal $V_{i,cm}$ is applied to the bulk-driven differential pair in Fig. 1(b), assuming V_G to be a constant bias voltage, the voltage at the common source node of the pair, *S*, follows the input signal with a gain $V_S/V_{i,cm} \sim g_{mb}/(g_{mb}+g_m)$. In the used technology, g_m is around five times larger than g_{mb}, which entails that V_S follows $V_{i,cm}$ with high attenuation ($V_S/V_{i,cm} \sim 1/6$). To be specific, in this Section we will consider

an implementation of the bulk-driven differential pair in Fig. 1(b) in standard 0.35-μm CMOS technology, $V_{TH0,P} = -0.65$ V, $V_{DD} = 1$ V, $(W/L)_{MB1-MB2} = 200/0.7$ μm/μm and $I_B = 10$ μA. When $V_{i,cm} = V_{DD}$, the DC voltage at node *S* is far below this level (around 730 mV when $V_G = 0$ V), thus allowing transistor MBB to operate in saturation. As $V_{i,cm}$ is reduced, signal V_S decreases, existing a voltage level of $V_{i,cm}$ for which V_B becomes lower than V_S (at around 670 mV). For $V_{i,cm}$ ranging from this point to ground, the source-bulk *pn* junction of MB1 and MB2 operates in the forward bias region.

One of the main features of an MOS transistor is the DC isolation of its gate terminal. Therefore, it is important to know the actual behaviour of a CMOS bulk-driven input stage, as a high bulk current could cause important loading effects on the preceding stage. With this goal, the above bulk-driven differential pair was designed and fabricated. During the design phase, simulations showed that the input current, illustrated in Fig. 2(a) for different values of V_G, was very high when the input *pn* junction is forward biased. In order to confirm these results, the circuit was experimentally characterized, thus obtaining the curves depicted in Fig. 2(b). As observed, the measured input current for low values of $V_{i,cm}$ is much smaller (even by more than two orders of magnitude) than its simulated counterpart, which evidences that the simulation model of the MOS transistor (level 53 BSIM3v3) is not adequate when the input *pn* junction is forward biased. Specifically, the simulated input current saturates to one half the tail current source I_B for a single input terminal, whereas the measured input current is kept below 40 nA even under the worst-case forward biasing conditions. Indeed, in CMOS technologies, process parameters of diodes are usually characterized for reverse bias operation.
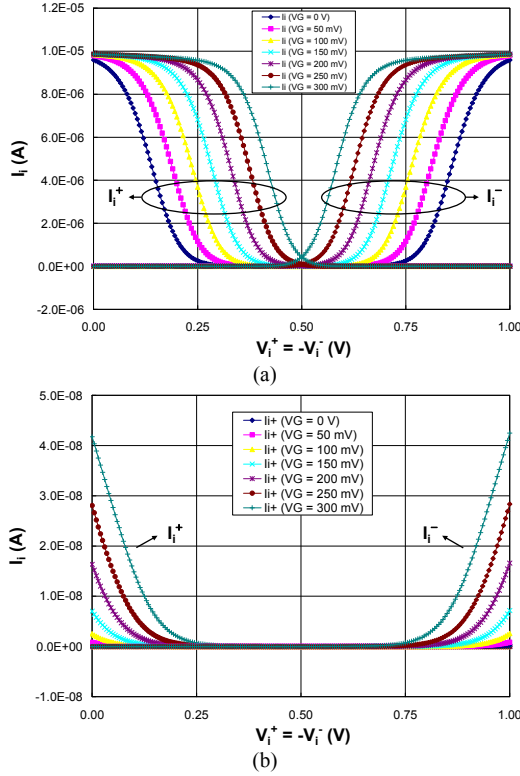
Figure 4. Input current of the bulk-driven differential pair as a function of $V_{i,dm}$ for different V_G values ($V_{i,cm} = 0.5$ V): (a) simulations and (b) measurements.
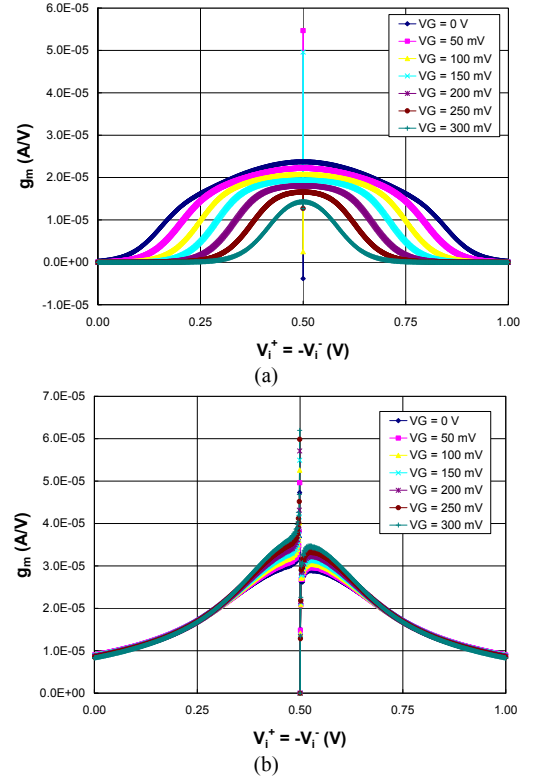

Figure 5. Effective transconductance of the bulk-driven differential pair vs. $V_{i,dm}$ for different V_G values ($V_{i,cm} = 0.5$ V): (a) simulations and (b) measurements.

In particular, in the technology used, it is explicitly suggested not to rely on diode models under forward biasing.

The DC behaviour characterization of the bulk-driven differential pair was completed by analyzing the response of the transconductance for different values of $V_{i,cm}$. Simulated and experimental results were obtained by superimposing a differential signal $V_{i,dm} = 50$ mV to V_{icm}. The transconductance was obtained as a function of the input CM voltage by dividing the differential output current and the constant differential input voltage. Again, a disagreement is apparent between simulated [Fig. 3(a)] and experimental [Fig. 3(b)] results. The measured curves show that trasnconductance monotonically increases as $V_{i,cm}$ moves towards the negative supply. This behaviour is consistent with the fact that, as $V_{i,cm}$ is made smaller, voltage V_{BS} is made negative and higher, thus reducing the absolute value of the effective threshold voltage. The reduction of $|V_{TH}|$ results in an increase of the effective transconductance of the differential pair. In contrast, the simulated transconductance of the pair displays a maximum at the value of $V_{i,cm}$ where the input source-bulk pn junction becomes forward biased. This fact confirms that the simulation model of the MOS transistor is not correct when the input pn junction is forward biased. Indeed, in simulations, a non negligible part of the tail current of the pair flows through the input pn junctions under forward biasing conditions, thereby reducing the drain current of MOS transistors MB1 and MB2 and, hence, their transconductance.

B. Differential-mode voltage behaviour

The small-signal equivalent circuit of a bulk-driven differential pair for a DM input signal is similar to that of its gate-driven counterpart, except for the fact that g_m is replaced by g_{mb}. The voltage controlled current source representing the gate transconductance in the equivalent circuit of the input bulk-driven MOS transistors is cancelled out, as the gate of these devices is connected to a DC voltage and their common source terminal may be considered as AC ground. As a consequence, the transconductance of the bulk-driven differential pair coincides with the g_{mb} of the input transistors, which leads to the degradation of circuit parameters relying on the input stage transconductance. It is also worth to point out that the response of a bulk-driven differential pair to a large DM input signal is similar to that of its gate-driven counterpart. A substantial difference is that the lower transconductance of bulk-driven MOS transistors leads to a wider linear operating range for the differential pair, as a larger input DM voltage is required to force its operation in the slew region.

The DM response of the bulk-driven differential pair in Fig. 1(b) was characterized by applying an input DM signal with a constant CM level of 0.5 V for different values of V_G. The input DM signal was swept over the whole allowed range. Figure 4(a) illustrates the simulated input current, whereas measurements are provided in Fig. 4(b). A similar disagreement as in the case of the CM response is observed between the two sets of results. Regarding the effective transconductance, simulated [Fig. 5(a)] and experimental [Fig. 5(b)] results have a similar shape. Nevertheless, in the simulated case, the differential pair goes out of its linear region for larger values of the input DM signal, this effect being more appreciable for increasing values of V_G. These results are consistent with the decreased transconductance observed in simulations under forward biasing conditions for
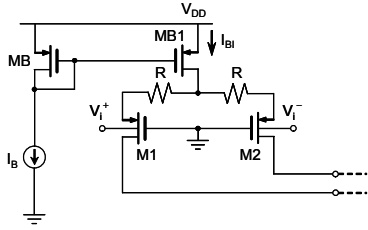
Figure 6. Proposed CMOS bulk-driven voltage-to-current converter.

the input *pn* junctions. The singularity in both simulated and experimental curves at $V_i^+ = V_i^- = 0.5$ V is due to the fact that, in our analysis, the transconductance is calculated as the ratio between the differential output current and the differential input voltage, which becomes zero in this particular point.

It may be concluded that the simulated input current of a CMOS bulk-driven differential pair is overestimated by circuit simulations as compared to the experimental behaviour. The inaccuracy of the model arises in the voltage region where the input source-bulk *pn* junction is forward biased and also affects other circuit parameters, such as the transconductance. The behaviour considerations regarding the CM voltage have been applied to the design of non-inverting applications, where the input CM voltage range is of paramount importance [6]. The following of this contribution presents a bulk-driven circuit application in which both the CM and DM input ranges are considered, and provides a comparison between the simulated and the measured input current.

III. APPLICATION CASE: LOW-VOLTAGE BULK-DRIVEN VOLTAGE-TO-CURRENT CONVERTER

A. Circuit scheme

Figure 6 shows a low-voltage voltage-to-current converter, implemented by means of a CMOS bulk-driven differential pair with source degeneration. This circuit section is a part of the input stage of an instrumentation amplifier intended to amplify the voltage signal of a piezoresistive bridge-based sensor with a total supply voltage of 1 V. The resistive bridge provides a signal with a DC component around midsupply, i.e., 0.5 V. This voltage level is not enough to turn either an NMOS or a PMOS gate-driven differential pair on. For this reason, input bulk-driven MOS transistors have been used.

B. Simulated and experimental results

The instrumentation amplifier including the voltage-to-current converter in Fig. 6 was designed to operate with a 1-V supply and fabricated in standard 0.35-μm CMOS technology, threshold voltages equal to 0.5 V and –0.65 V for NMOS and PMOS transistors, respectively. The simulation model used for the MOS transistors was a level 53 BSIM3v3. The biasing current of the input differential pair, I_{BI}, was set to 1 μA and the value of passive resistors R was equal to 10 kΩ. Finally, the input common-mode voltage, $V_{i,cm}$, was set to 0.5 V.

The simulated and experimental input currents, I_i, of the circuit are plotted in Fig. 7 as a function of the input differential voltage. A logarithmic scale has been used to
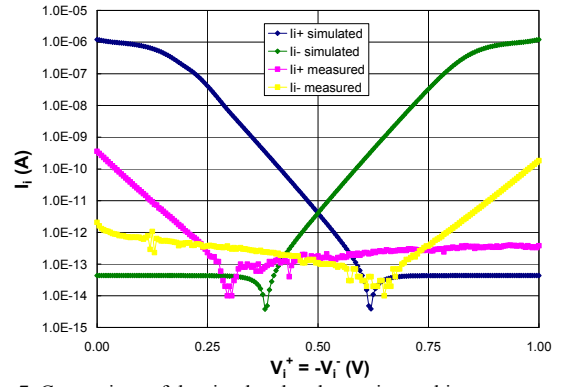

Figure 7. Comparison of the simulated and experimental input current of the bulk-driven instrumentation amplifier as a function of $V_{i,dm}$ ($V_{i,cm} = 0.5$ V).

facilitate comparison, which illustrates a disagreement by three orders of magnitude. As observed, the simulated worst-case input current approaches the biasing current of the differential pair. In contrast, the measured absolute value of I_i is kept below 0.5 nA even for the worst-case forward biasing of the source-bulk *pn* junction, i.e., when V_{in}^+ is equal to ground and V_{in}^- to V_{DD} and vice versa. In these cases, the effective input resistance of each individual input terminal is above 100 MΩ, which is equivalent to present a nearly isolated input.

IV. CONCLUSION AND FUTURE WORK

The simulated and experimental DC behaviours of a bulk-driven differential pair have been provided. The comparison of the two responses demonstrates that the simulation model of the MOS transistor is not accurate in the voltage region where the input source-bulk *pn* junction is forward biased. The main result of the model inaccuracy is the overestimation of the differential pair input current. The design of a bulk-driven low voltage voltage-to-current converter has been introduced as an application case in which the comparison conclusions are applied. The future work will be focused on the analysis of the simulation model, so as to suggest modifications in order to obtain a simulated behaviour closer to the actual one.

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