Lab 7

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Question 1

The hit rates for various cache configurations for Program 1 with L1 set to (8,8) are as follows : (L,B and W denote lines, blocks and ways respectively)

Configuration	Hits	Misses	Hit-rate
L = 1,2,3,4,5 and B = 0 and W = 2	49	17	0.7424
B = 1 and L = 3 and W = 0	33	33	0.5
B = 2 and L = 3 and W = 0	49	17	0.7424
B = 3 and L = 3 and W = 0	57	9	0.8636
B = 4 and L = 3 and W = 0	61	5	0.9242
B = 5 and L = 3 and W = 0	63	3	0.9545
W = 0,1,2 and B = 2 and L = 3	49	17	0.7424

The hit rates for various cache configurations for Program 1 with L1 set to (8,16) are as follows : (L,B and W denote lines, blocks and ways respectively)

Configuration	Hits	Misses	Hit-rate
L = 1,2,3,4,5 and B = 0 and W = 2	97	33	0.7462
B = 1 and L = 3 and W = 0	65	65	0.5
B = 2 and L = 3 and W = 0	97	33	0.7462
B = 3 and L = 3 and W = 0	113	17	0.8692
B = 4 and L = 3 and W = 0	121	9	0.9308
B = 5 and L = 3 and W = 0	125	5	0.9615
W = 0,1,2 and B = 2 and L = 3	97	33	0.7462

The hit rates for various cache configurations for Program 1 with L1 set to (16,8) are exactly the same as those when L1 is set to (8,16).

The hit rates for various cache configurations for Program 1 with L1 set to (16,16) are as follows : (L,B and W denote lines, blocks and ways respectively)

Configuration	Hits	Misses	Hit-rate
L = 1,2,3,4,5 and B = 0 and W = 2	193	65	0.7481
B = 1 and L = 3 and W = 0	129	129	0.5
B = 2 and L = 3 and W = 0	193	65	0.7481
B = 3 and L = 3 and W = 0	225	33	0.8721
B = 4 and L = 3 and W = 0	241	17	0.9341
B = 5 and L = 3 and W = 0	249	9	0.9651
W = 0,1,2 and B = 2 and L = 3	193	65	0.7481

The hit rates for various cache configurations for Program 2 with L1 set to (8,8) are as follows : (L,B and W denote lines, blocks and ways respectively)

Configuration	Hits	Misses	Hit-rate
L = 1,2 and B = 0 and W = 2	2	64	0.0303
L = 3 and B = 0 and W = 2	3	63	0.04545
L = 4,5 and B = 0 and W = 2	49	17	0.7424
B = 1 and L = 3 and W = 0	1	65	0.01515
B = 2 and L = 3 and W = 0	3	63	0.04545
B = 3 and L = 3 and W = 0	57	9	0.8636
B = 4 and L = 3 and W = 0	61	5	0.9242
B = 5 and L = 3 and W = 0	63	3	0.9545
W = 0 and B = 2 and L = 3	3	63	0.04545
W = 1,2 and B = 2 and L = 3	49	17	0.7424

The hit rates for various cache configurations for Program 2 with L1 set to (8,16) are as follows : (L,B and W denote lines, blocks and ways respectively)

Configuration	Hits	Misses	Hit-rate
L = 1,2,3,4,5 and B = 0 and W = 2	2	128	0.01538
B = 1 and L = 3 and W = 0	1	129	0.007692
B = 2,3,4 and L = 3 and W = 0	2	128	0.01538
B = 5 and L = 3 and W = 0	122	8	0.9385
W = 0,1,2 and B = 2 and L = 3	2	128	0.01538

The hit rates for various cache configurations for Program 2 with L1 set to (16,8) are as follows : (L,B and W denote lines, blocks and ways respectively)

Configuration	Hits	Misses	Hit-rate
L = 1,2 and B = 0 and W = 2	2	128	0.01538
L = 3 and B = 0 and W = 2	5	125	0.03846
L = 4,5 and B = 0 and W = 2	111	19	0.8538
B = 1 and L = 3 and W = 0	1	129	0.007692
B = 2 and L = 3 and W = 0	5	125	0.03846
B = 3 and L = 3 and W = 0	120	10	0.9231
B = 4 and L = 3 and W = 0	125	5	0.9615
B = 5 and L = 3 and W = 0	127	3	0.9769
W = 0 and B = 2 and L = 3	5	125	0.03846
W = 1,2 and B = 2 and L = 3	111	19	0.8538

The hit rates for various cache configurations for Program 2 with L1 set to (16,16) are as follows : (L,B and W denote lines, blocks and ways respectively)

Configuration	Hits	Misses	Hit-rate
L = 1,2,3,4 and B = 0 and W = 2	2	256	0.007752
L = 5 and B = 0 and W = 2	3	255	0.01163
B = 1 and L = 3 and W = 0	1	257	0.003876
B = 2,3 and L = 3 and W = 0	2	256	0.007752
B = 4 and L = 3 and W = 0	3	255	0.01163
B = 5 and L = 3 and W = 0	247	11	0.9574
W = 0,1,2 and B = 2 and L = 3	2	256	0.007752

Question 2

The hit rates for various cache configurations for Program 1 with L1 set to (8,8) are as follows : (WT and WB denote Write-through and Write-back policies respectively, WA and WnA denote with allocate and without allocate respectively)

Configuration	Hits	Misses	Hit-rate
WT and WA	49	17	0.7424
WT and WnA	3	63	0.04545
WB and WA	49	17	0.7424
WB and WnA	3	63	0.04545

The hit rates for various cache configurations for Program 1 with L1 set to (8,16) **or** (16,8) are as follows : (WT and WB denote Write-through and Write-back policies respectively, WA and WnA denote with allocate and without allocate respectively)

Configuration	Hits	Misses	Hit-rate
WT and WA	97	33	0.7462
WT and WnA	3	127	0.02308
WB and WA	97	33	0.7462
WB and WnA	3	127	0.02308

The hit rates for various cache configurations for Program 1 with L1 set to (16,16) are as follows : (WT and WB denote Write-through and Write-back policies respectively, WA and WnA denote with allocate and without allocate respectively)

Configuration	Hits	Misses	Hit-rate
WT and WA	193	65	0.7481
WT and WnA	3	255	0.01163
WB and WA	193	65	0.7481
WB and WnA	3	255	0.01163

The hit rates for various cache configurations for Program 2 with L1 set to (8,8) are as follows : (WT and WB denote Write-through and Write-back policies respectively, WA and WnA denote with allocate and without allocate respectively)

Configuration	Hits	Misses	Hit-rate
WT and WA	49	17	0.7424
WT and WnA	3	63	0.04545
WB and WA	49	17	0.7424
WB and WnA	3	63	0.04545

The hit rates for various cache configurations for Program 2 with L1 set to (8,16) are as follows : (WT and WB denote Write-through and Write-back policies respectively, WA and WnA denote with allocate and without allocate respectively)

Configuration	Hits	Misses	Hit-rate
WT and WA	2	128	0.01538
WT and WnA	3	127	0.02308
WB and WA	2	128	0.01538
WB and WnA	3	127	0.02308

The hit rates for various cache configurations for Program 2 with L1 set to (16,8) are as follows : (WT and WB denote Write-through and Write-back policies respectively, WA and WnA denote with allocate and without allocate respectively)

Configuration	Hits	Misses	Hit-rate
WT and WA	111	19	0.8538
WT and WnA	3	127	0.02308
WB and WA	111	19	0.8538
WB and WnA	3	127	0.02308

The hit rates for various cache configurations for Program 2 with L1 set to (16,16) are as follows : (WT and WB denote Write-through and Write-back policies respectively, WA and WnA denote with allocate and without allocate respectively)

Configuration	Hits	Misses	Hit-rate
WT and WA	3	255	0.01163
WT and WnA	3	255	0.01163
WB and WA	3	255	0.01163
WB and WnA	3	255	0.01163

Question 3

The hit rates for various cache configurations for Program 1 with L1 set to (8,8) are as follows :

Configuration	Hits	Misses	Hit-rate
Direct mapped	49	17	0.7424
2-way Set associative	49	17	0.7424
Fully associative	49	17	0.7424

The hit rates for various cache configurations for Program 1 with L1 set to (8,16) **or** (16,8) are as follows :

Configuration	Hits	Misses	Hit-rate
Direct mapped	97	33	0.7462
2-way Set associative	97	33	0.7462
Fully associative	97	33	0.7462

The hit rates for various cache configurations for Program 1 with L1 set to (16,16) are as follows :

Configuration	Hits	Misses	Hit-rate
Direct mapped	193	65	0.7481
2-way Set associative	193	65	0.7481
Fully associative	193	65	0.7481

The hit rates for various cache configurations for Program 2 with L1 set to (8,8) are as follows :

Configuration	Hits	Misses	Hit-rate
Direct mapped	49	17	0.7424
2-way Set associative	49	17	0.7424
Fully associative	49	17	0.7424

The hit rates for various cache configurations for Program 2 with L1 set to (8,16) are as follows :

Configuration	Hits	Misses	Hit-rate
Direct mapped	2	128	0.01538
2-way Set associative	2	128	0.01538
Fully associative	82	48	0.6308

The hit rates for various cache configurations for Program 2 with L1 set to (16,8) are as follows :

Configuration	Hits	Misses	Hit-rate
Direct mapped	111	19	0.8538
2-way Set associative	111	19	0.8538
Fully associative	111	19	0.8538

The hit rates for various cache configurations for Program 2 with L1 set to (16,16) are as follows :

Configuration	Hits	Misses	Hit-rate
Direct mapped	3	255	0.01163
2-way Set associative	2	256	0.007752
Fully associative	178	80	0.6899

The hit rates for various cache configurations for Program 3 with L1 set to (8,8) are as follows :

Configuration	Hits	Misses	Hit-rate
Direct mapped	2	128	0.01538
2-way Set associative	96	34	0.7385
Fully associative	96	34	0.7385

The hit rates for various cache configurations for Program 3 with L1 set to (8,16) **or** (16,8) are as follows :

Configuration	Hits	Misses	Hit-rate
Direct mapped	3	255	0.01163
2-way Set associative	192	66	0.7742
Fully associative	192	66	0.7742

The hit rates for various cache configurations for Program 3 with L1 set to (16,16) are as follows :

Configuration	Hits	Misses	Hit-rate
Direct mapped	35	479	0.06809
2-way Set associative	384	130	0.7471
Fully associative	384	130	0.7471

Conclusions

The following observations can be made from above tabulated data :

- The hit rate is unchanged when we change the number of lines or ways in Program 1 for any set of values present in L1 label although hit rate increases on increasing the number of blocks. For Program 2, increasing the number of lines increases the hit rate with an exception of the setting where L1 is (8,16). For this program, increasing the number of blocks increases the hit rate for any set of values present in L1 label. Also, increasing the number of lines increases the hit rate only when L1 is (8,8) or (16,8).

- Write-through and Write-back policies with allocate give a better hit rate when compared to without allocate in Program 1 for all the label settings. For Program 2 also this holds true with the exception of the setting when label L1 is (8,16) in which without allocate outperforms with allocate by a small margin.

- In Program 1 for a particular setting of label L1, Direct mapped, 2-way Set associative and Fully associative configurations give same hit rates. But hit rate increases as we change L1 from (8,8) to (16,16). On a flip side, in Program 2 the hit rate increase is not monotonic. It decreases from (8,8) to (8,16), increases from (8,16) to (16,8) and finally decreases from (16,8) to (16,16). For Program 3, the variation in hit rates between various settings of label L1 is not as high that of Program 2. For Programs 2 and 3, 2-way Set associative and Fully associative configurations give better hit rates when compared to Direct mapped configuration on an average.