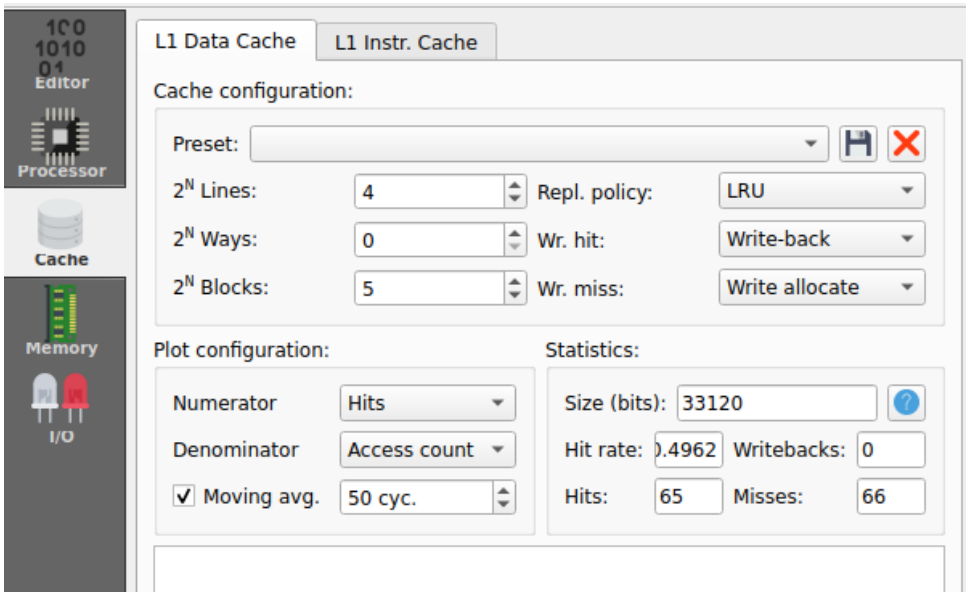
Computer Architecture - CS2323. Autumn 2022

Lab-7 (Understanding Cache Operation)

In this lab assignment, we will use Ripes simulator to execute different assembly codes with different cache configurations and understand the effect on the hit/miss rate of the data cache. In Ripes, there is a button named “Cache” on the left which opens a cache analysis window on click.
You may execute some portion of this step by step to understand the animation of how the cache is filled and evicted for different instructions.



1. Cache reads: Execute the assembly programs 1 and 2 and observe the hit rates for various data cache configurations.
   You should vary the configurations atleast as per the following (you are free to explore more combinations as well):
   Lines: 1, 2, 3, 4, 5 keeping Blocks as 2 and Ways as 0
   Blocks: 1, 2, 3, 4, 5 keping Lines as 3 and Ways as 0
   Ways: 0, 1, 2 keeping Blocks as 2 and Lines as 3
2. Write-policies: Modify programs 1 and 2 to replace “ld x20, 0(x12)” to “sd x20, 0(x12)”. Use the preset cache configuration (32-entry 4-word direct mapped). Run program-1 and program-2 for various combinations of Write-through and Write-back policies (with allocate and without allocate).
3. Associativity: Execute programs 1, 2, and 3 and vary the following configurations:
   a. 32-entry 4-word direct mapped
   b. 32-entry 4-word 2-way set associative
   c. 32-entry 4-word fully associative

Repeat the above experiments for four different settings in the assembly code:
L1: (8, 8), (8,16), (16,8), (16,16)

Submission instructions:

Prepare a report where you tabulate the hit rate, number of hits, number of misses, and total accesses. Summarize the observations and explain the trend that you observe during this experiment. You may create some line plots or bar plots that indicate the results better.

An example observation could be “Increasing Lines does not improve the hit rate in program-1 because … However, it improves the hit rate in program-2 because…”, or
“Changing parameters L1 from 8,8 to 16,16 reduces the hit rate because …”

Submit the report in pdf format with name CSYYBTECHZZZZZ.pdf.

Deadline: 22 Nov 2022 (Tuesday), 10.00 pm
Late submission: No late submission allowed for this assignment.
Note: Submissions are subject to similarity check and hence submit only your own work.

Optional (for learning): You may run your matrix multiplication code from Lab-5 to understand how its hit rate changes with various cache configurations.

Program-1

```
.data
L1: .dword 8, 8
A:

.text
la x3, L1
ld x4, 0(x3)
ld x5, 8(x3)
addi x3, x3, 16

   addi x10, x0, 0
   add x12, x3, x0
lf1: beq x4, x10, end1
      addi x11, x0, 0
lf2:    beq x5, x11, end2
          ld x20, 0(x12)
          addi x12, x12, 8
          addi x11, x11, 1
          beq x0, x0, lf2
end2:   addi x10, x10, 1
      beq x0, x0, lf1
end1: nop
```

Program-2:

```
.data
L1: .dword 8, 8
A:

.text
la x3, L1
ld x4, 0(x3)
ld x5, 8(x3)
addi x3, x3, 16

   addi x10, x0, 0
   add x12, x3, x0
lf1: beq x4, x10, end1
      addi x11, x0, 0
      slli x15, x10, 3
      add x12, x3, x15
lf2:   beq x5, x11, end2
         ld x20, 0(x12)
         slli x15, x5, 3
         add x12, x12, x15
         addi x11, x11, 1
         beq x0, x0, lf2
end2:  addi x10, x10, 1
      beq x0, x0, lf1
end1: nop
```

Program-3:

```
.data
L1: .dword 8, 8
A:

.text
la x3, L1
ld x4, 0(x3)
ld x5, 8(x3)
addi x3, x3, 16

   addi x10, x0, 0
   add x12, x3, x0
lf1: beq x4, x10, end1
      addi x11, x0, 0
lf2:    beq x5, x11, end2
          ld x20, 0(x12)
          ld x20, 1024(x12)
          addi x12, x12, 8
          addi x11, x11, 1
          beq x0, x0, lf2
end2:   addi x10, x10, 1
      beq x0, x0, lf1
end1: nop
```