Mod-5 Synchronous Counter

Edit History: Added Setup Time and max frequency on Page 17 & 18.

Rahul Kumar

2021EEN2023

ELP831 IEC Lab

Prof. Jayadeva

Objective

- To design a mod-5 synchronous counter using JK Flip Flop.
- Draw a transistor level schematic for each gate and use those gates to create higher level blocks.
- Verify that the schematic works as intended.
- Draw a layout for the entire design from scratch.
- Clear the DRC errors, verify the LVS and perform a PEX analysis

Index and components used

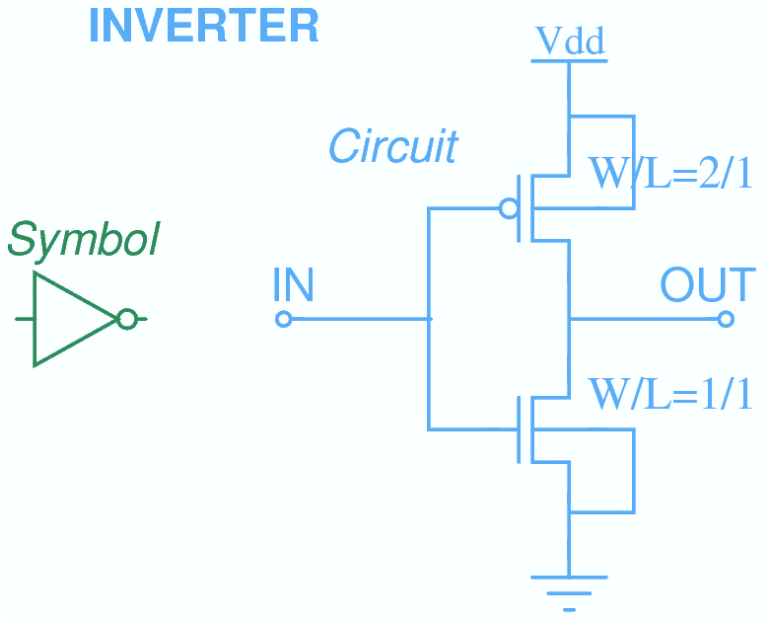
1. Inverter
2. AND gate
3. NAND-2 Gate
4. NAND-3 Gate
5. SR Latch
6. Master Slave JK Flip Flop
7. Mod-5 Counter

General Information

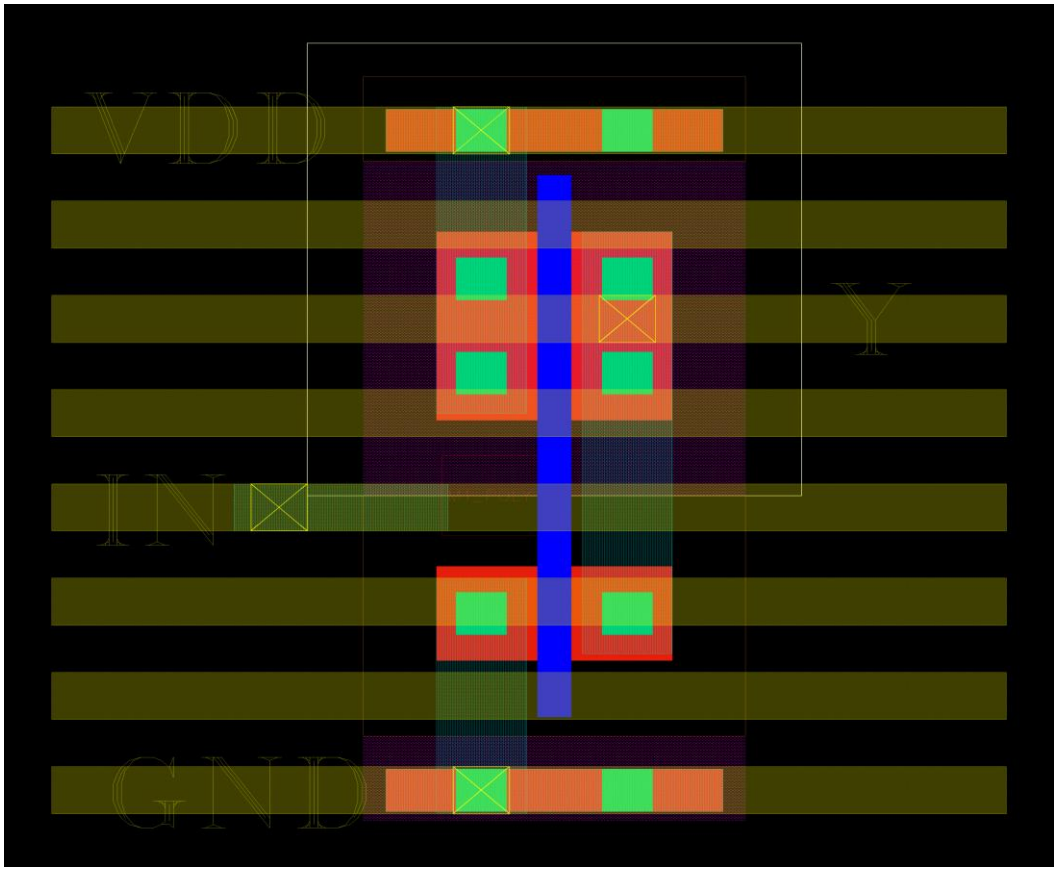
- All the schematics are drawn using **XCircuit software**
- Rise time and fall time of all the inputs is **10 femto-seconds**
- Input frequency is 250 MHz
- All the value reported in timing information tables are in **Pico-seconds**
- Height of standard cell is 1.4 um

1. Inverter Gate

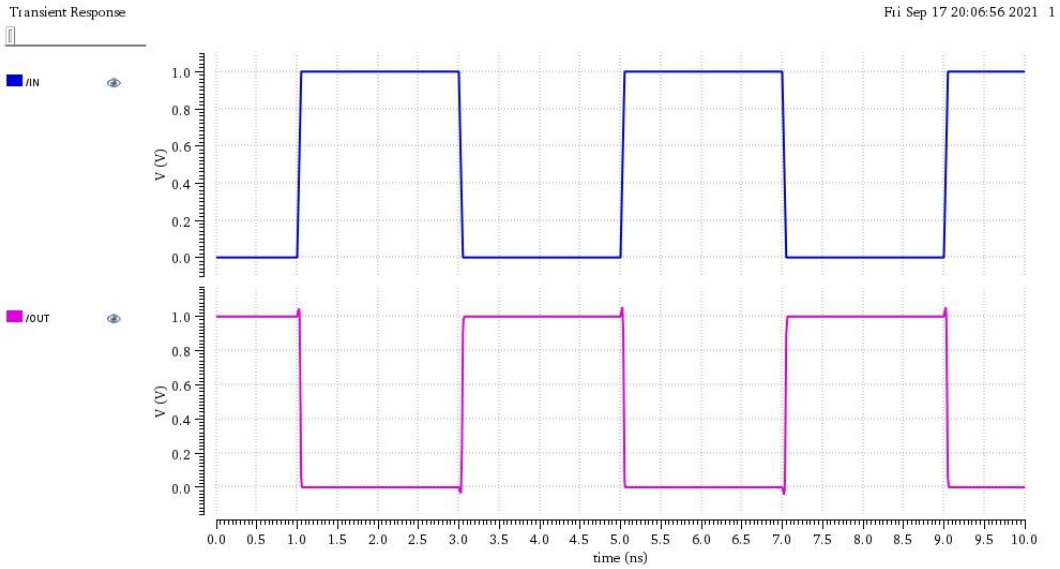
1.1 Schematic



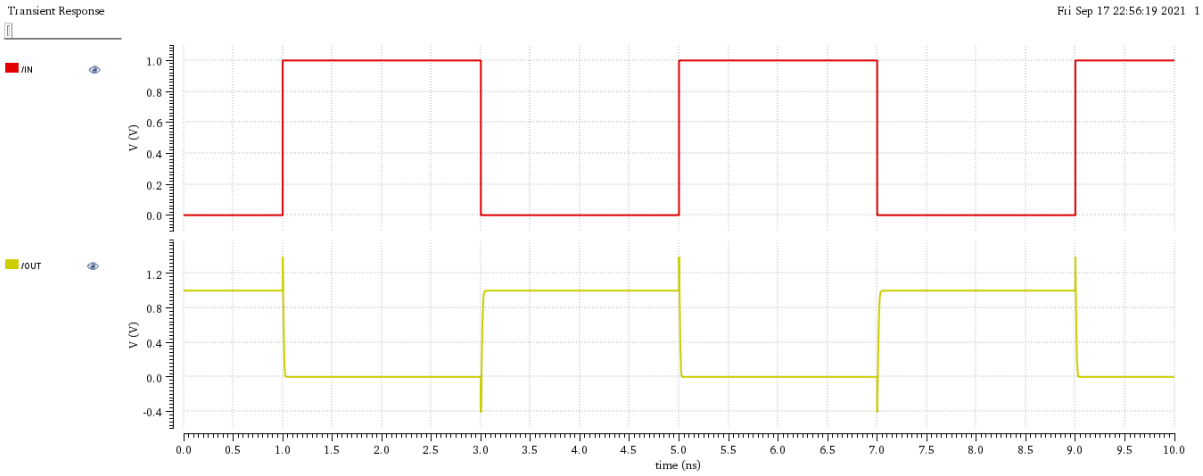
1.2 Layout



1.3 Pre-Layout Simulation



1.4 Post-Layout Simulation

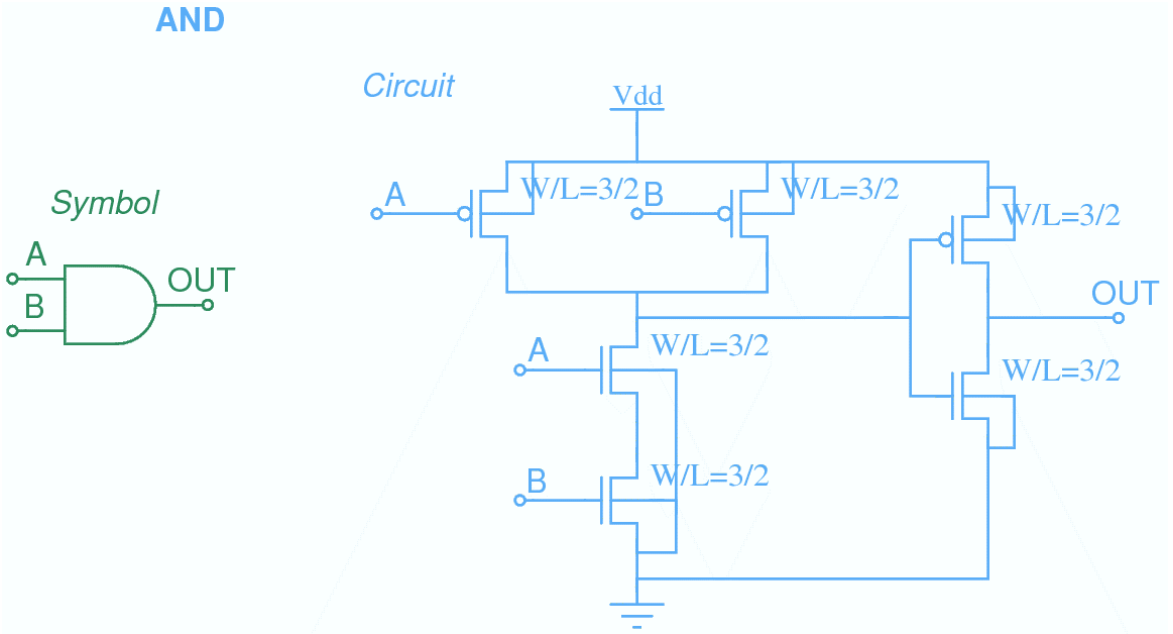


1.5 Timing Information

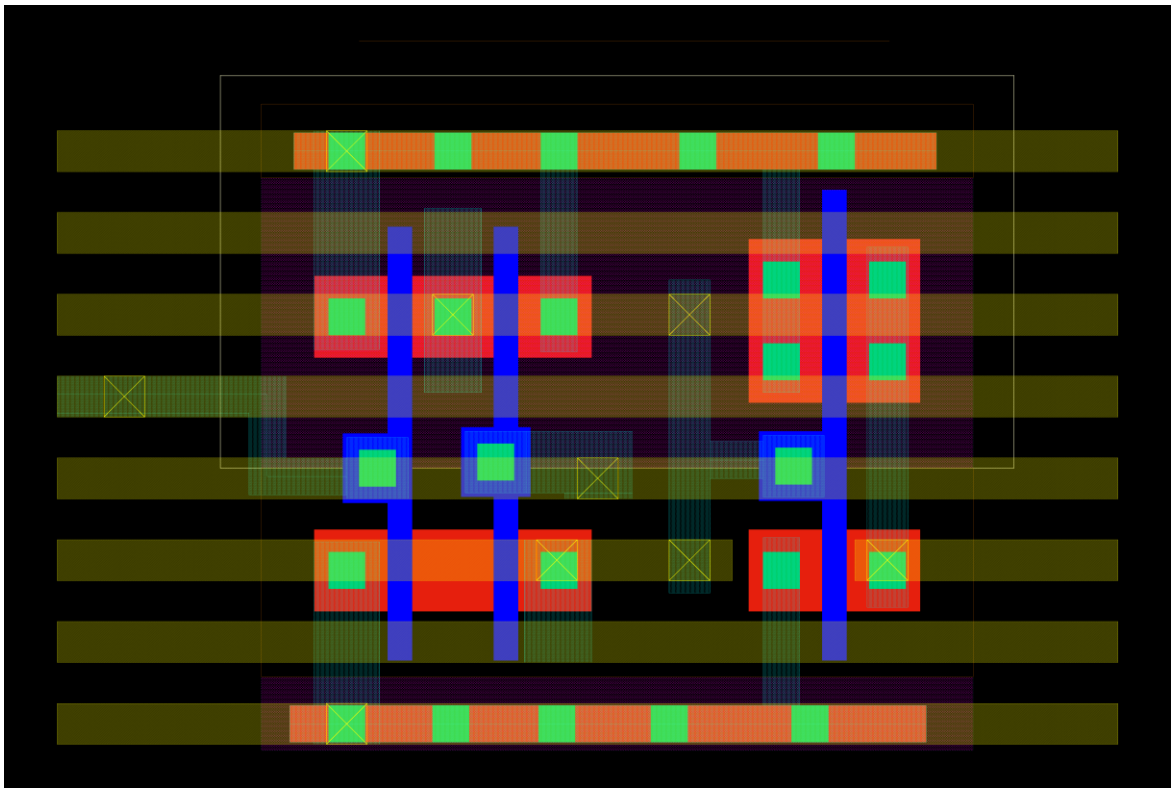
	Rise Time **Tr**	Fall Time **T_f**	**T_{PHL}**	**T_{PLH}**	Propagation Delay **T_P**
Pre-Layout	7.615	6.5	5.937	6.0033	5.97015
Post-Layout	17.2665	13.068	11.262	14.1405	12.70125

2. AND Gate

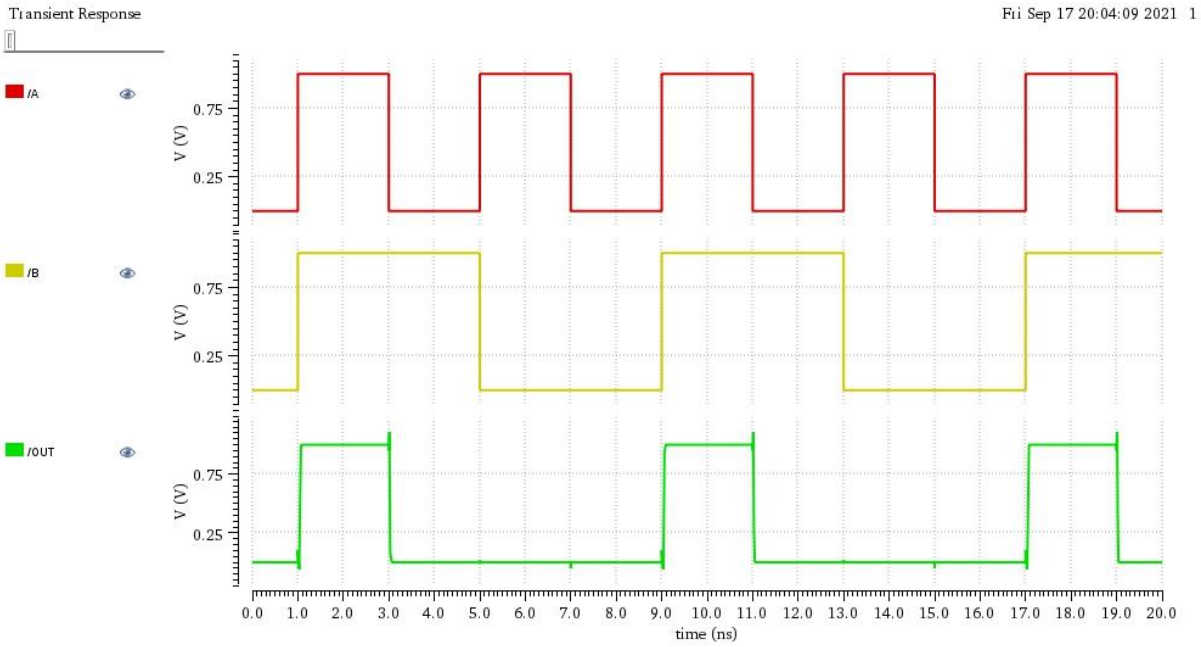
2.1 Schematic



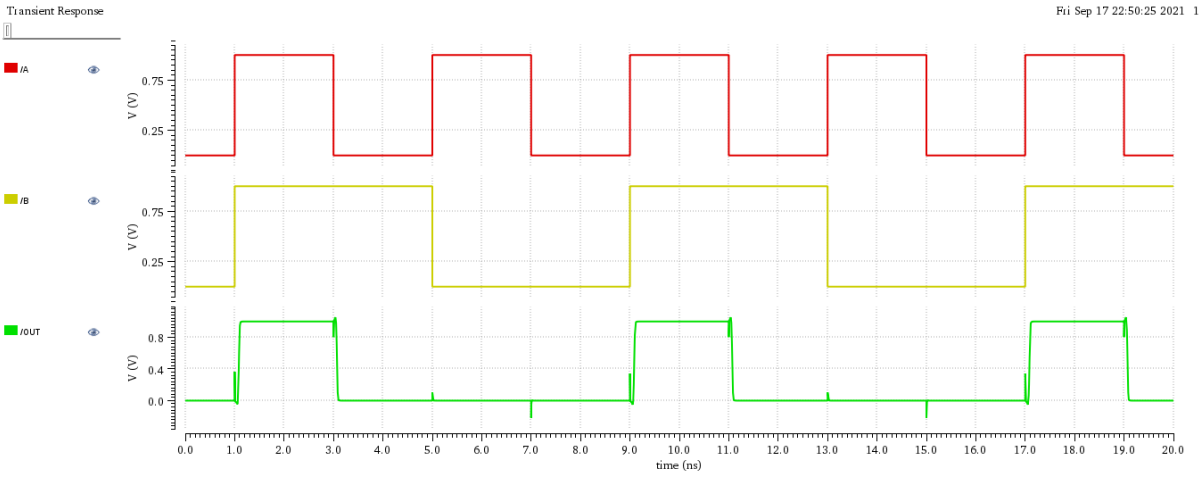
2.2 Layout



2.3 Pre-Layout Simulation



2.4 Post-Layout Simulation



2.5 Timing Information

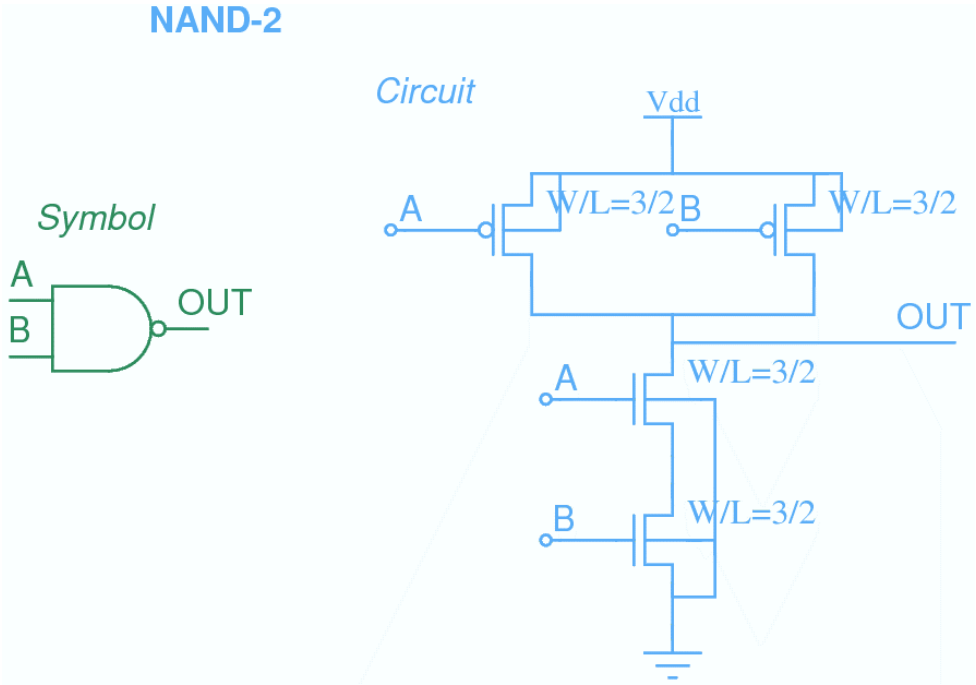
Input A: Time period = 4 ns

Input B: Time Period = 8 ns

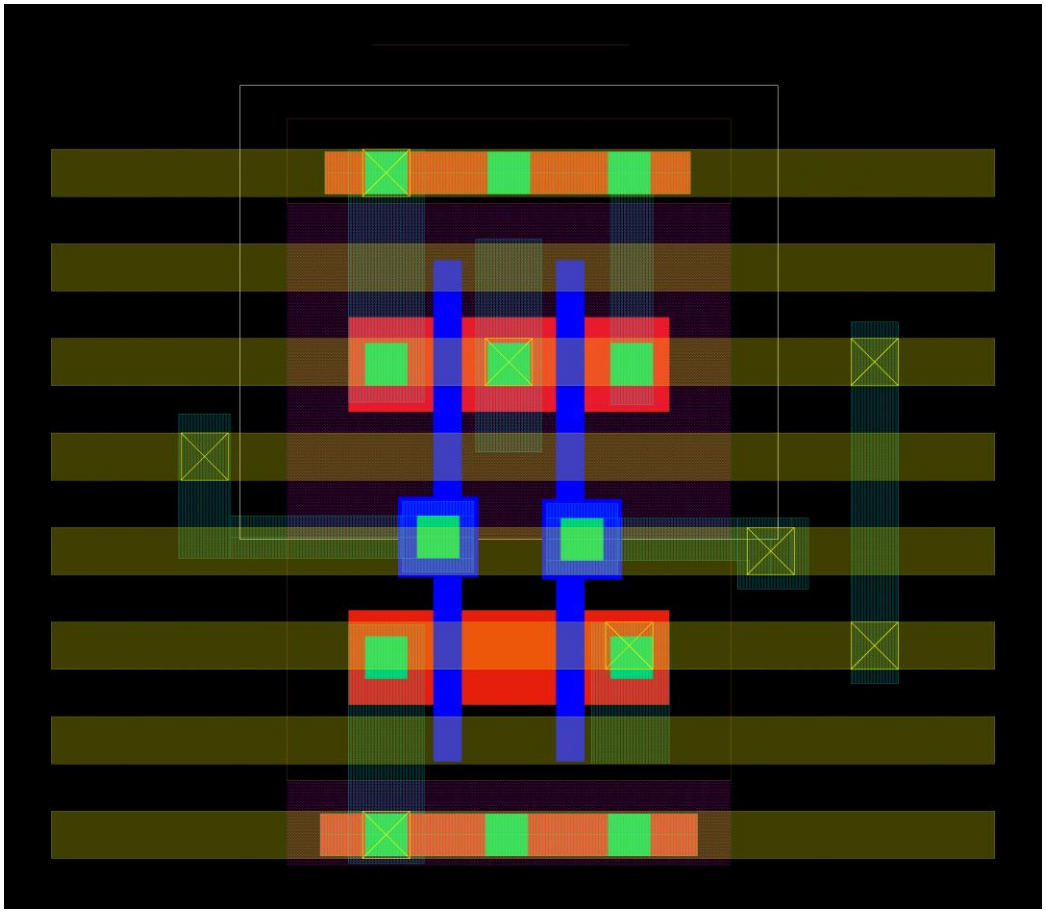
	Rise Time **Tr**	Fall Time **T_f**	**T_{PHL}**	**T_{PLH}**	Propagation Delay **T_P**
Pre-Layout	16.89	11.03	24.82	47.012	35.916
Post-Layout	29.7265	27.6878	71.223	87.043	79.133

3. NAND-2 Gate

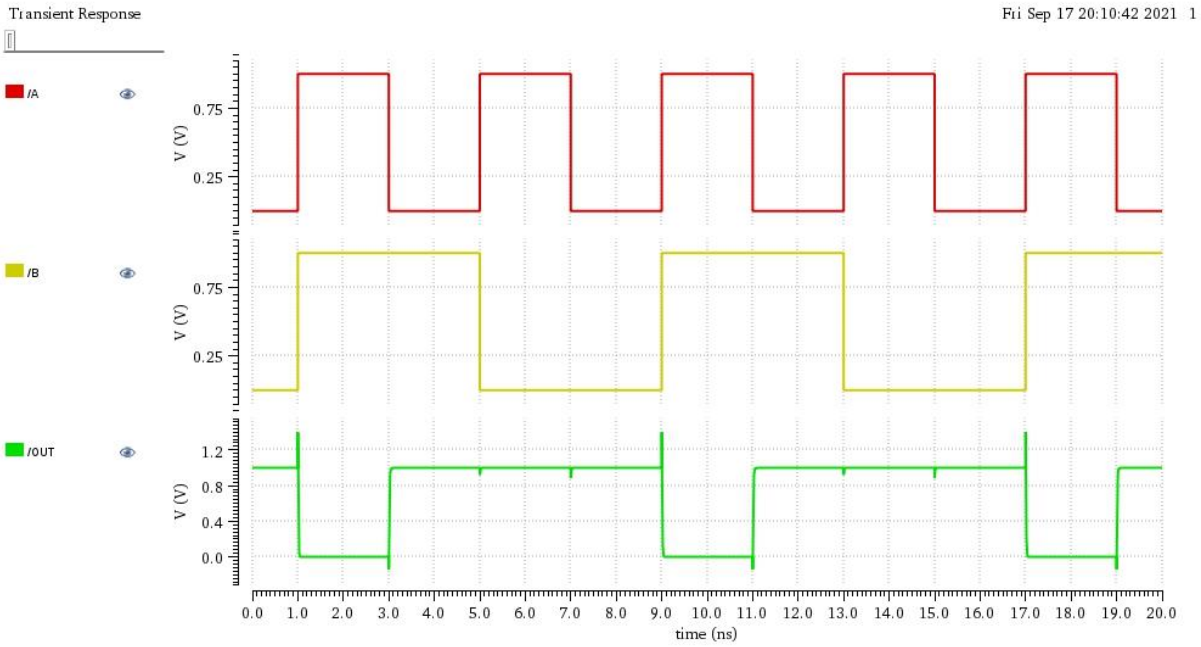
3.1 Schematic



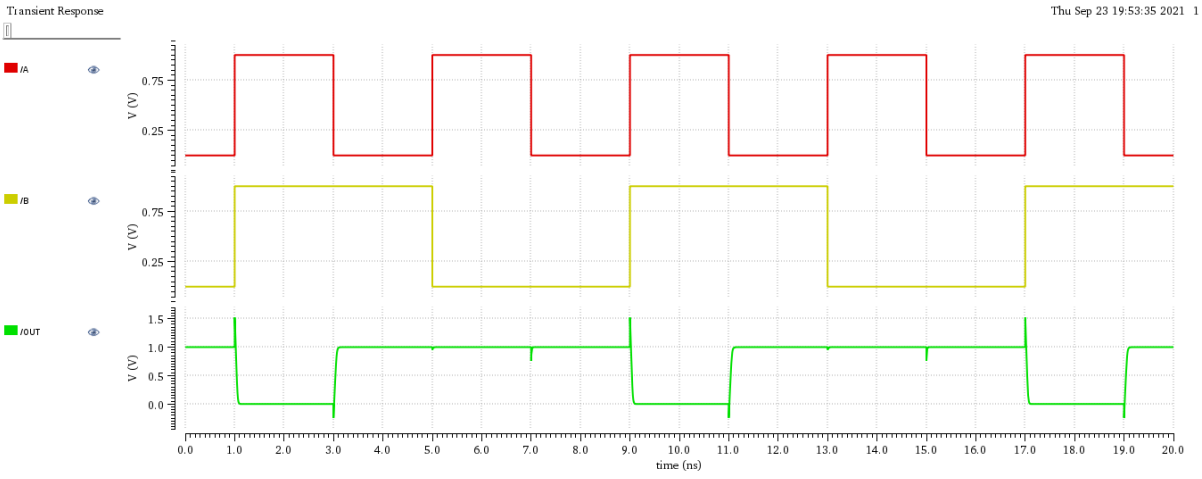
3.2 Layout



3.3 Pre-Layout Simulation



3.4 Post-Layout Simulation



3.5 Timing Information

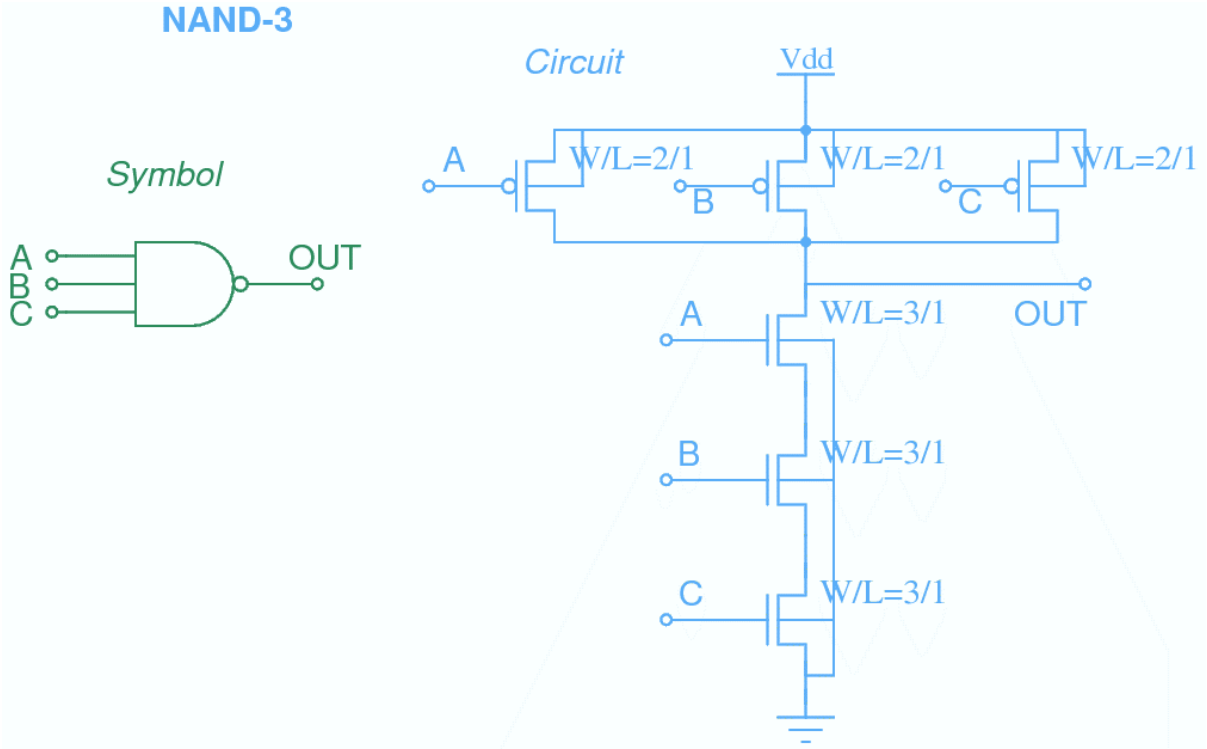
Input A: Time period = 4ns

Input B: Time Period = 8ns

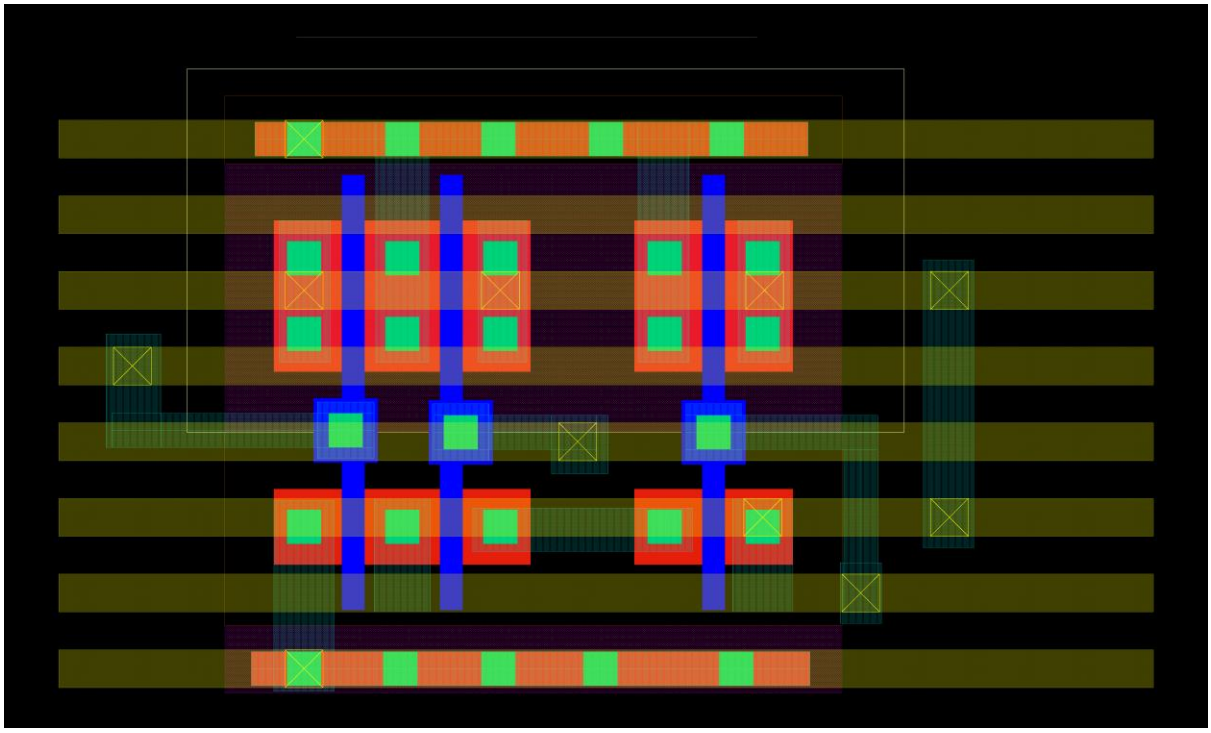
	Rise Time **Tr**	Fall Time **T_f**	**T_{PHL}**	**T_{PLH}**	Propagation Delay **T_P**
Pre-Layout	21.224	15.376	15.586	14.966	15.276
Post-Layout	52.7141	40.2342	41.2213	38.86	40.04065

4. NAND-3

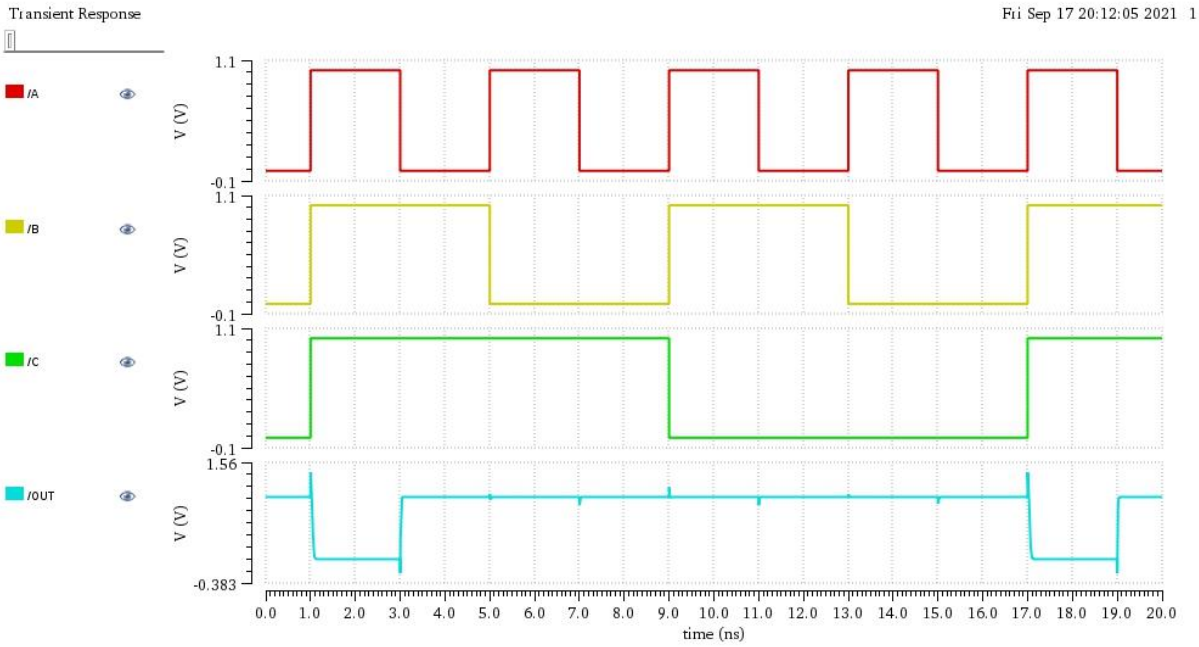
4.1 Schematic



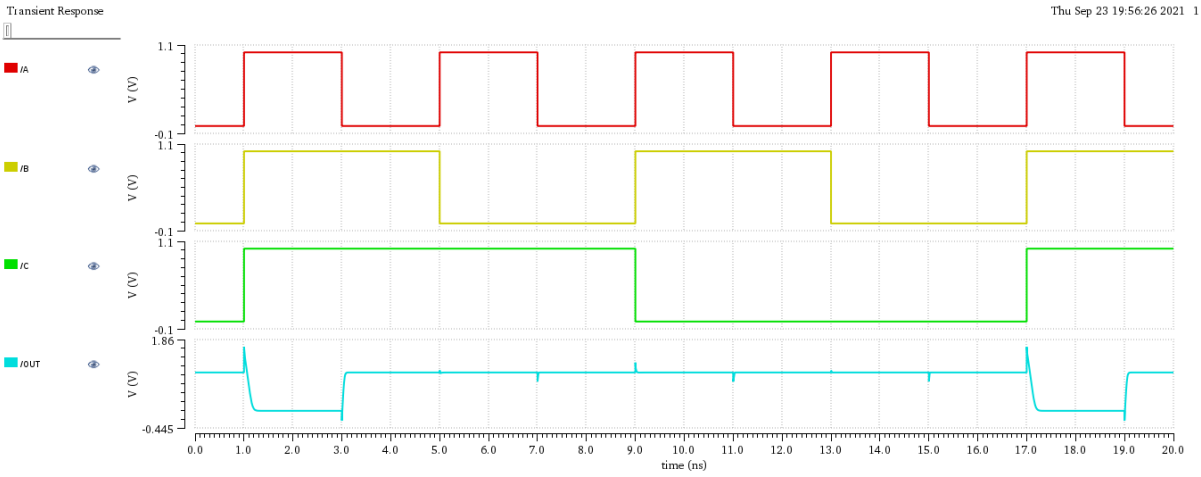
4.2 Layout



4.3 Pre-Layout Simulation



4.4 Post-Layout Simulation



4.5 Timing Information

Input A: Time period = 4 ns

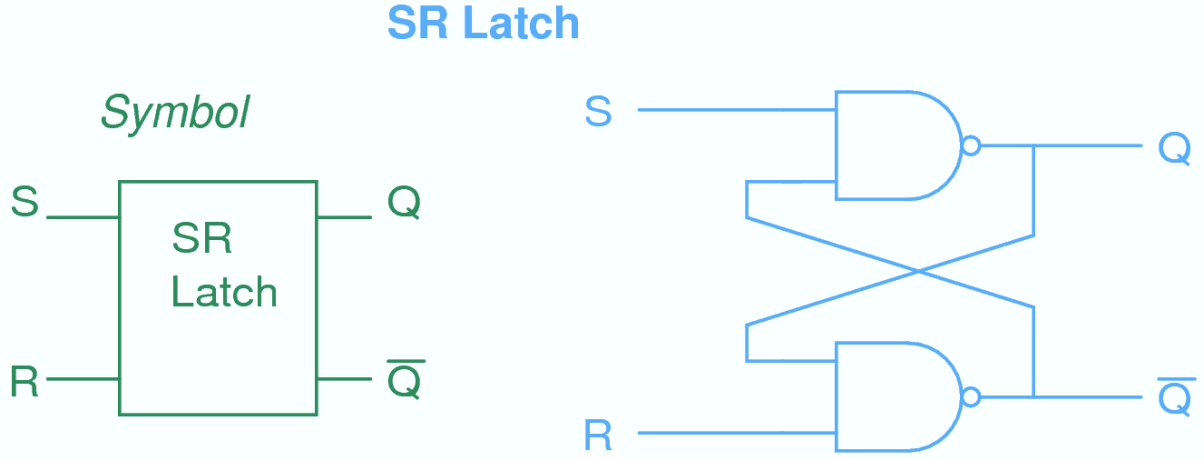
Input B: Time Period = 8 ns

Input C: Time Period = 16 ns

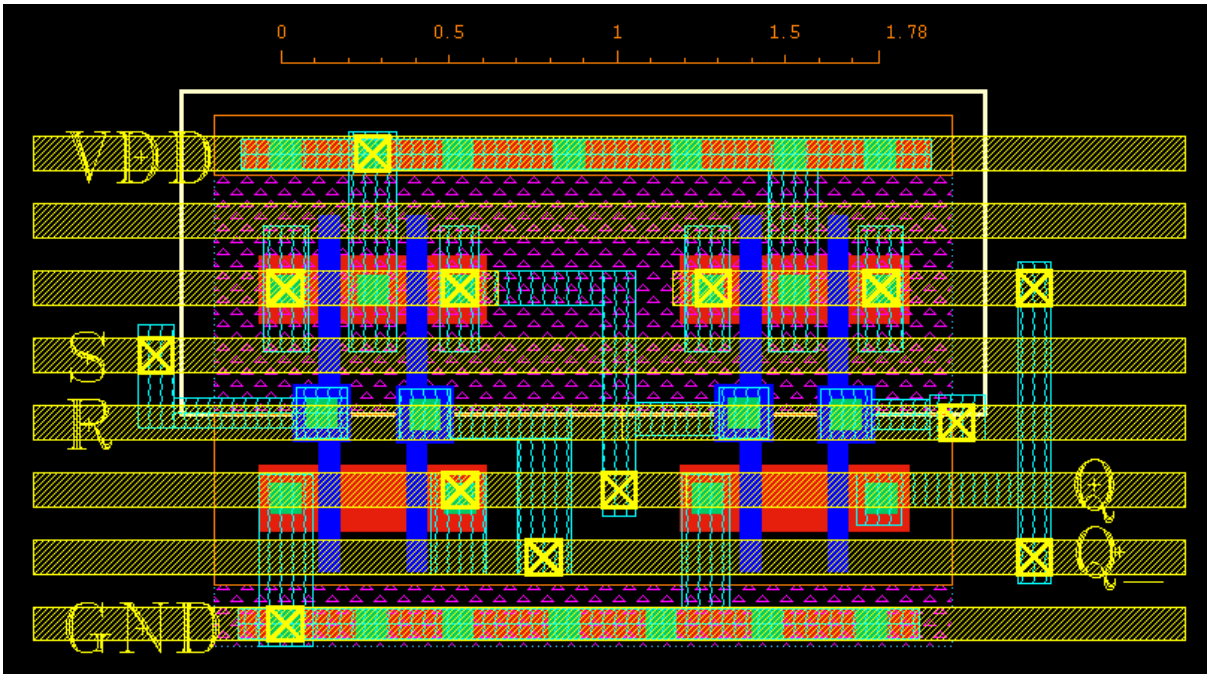
	Rise Time **Tr**	Fall Time **T_f**	**T_{PHL}**	**T_{PLH}**	Propagation Delay **T_P**
Pre-Layout	17.022	44.526	48.469	9.888	29.1785
Post-Layout	46.8024	110.241	117.078	31.2411	74.15955

5. SR Latch

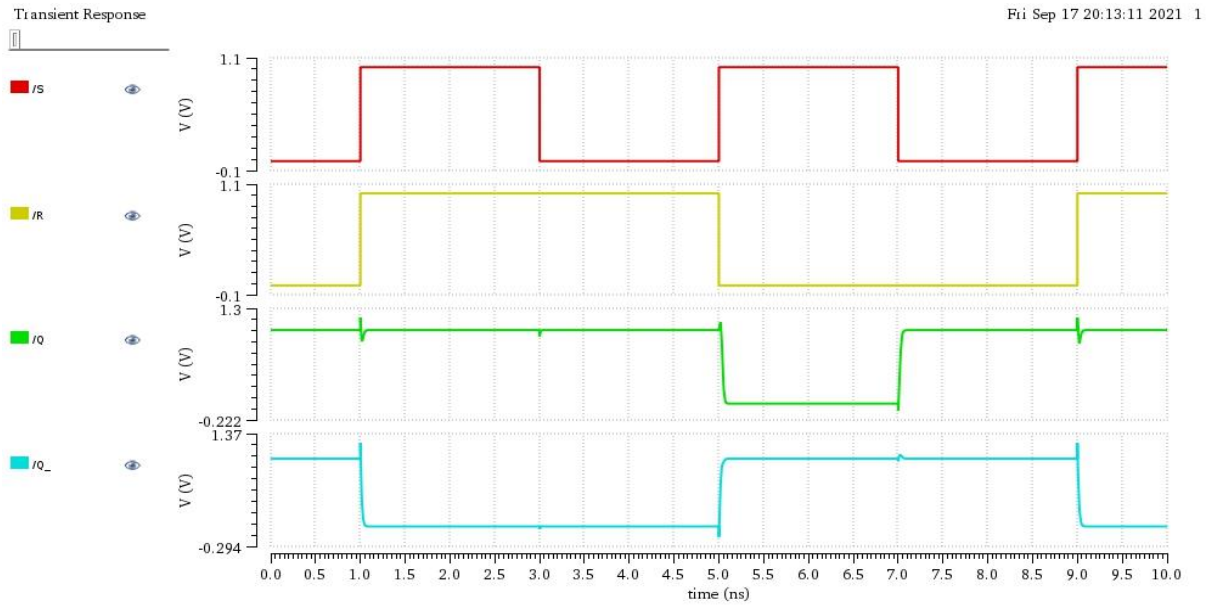
5.1 Schematic



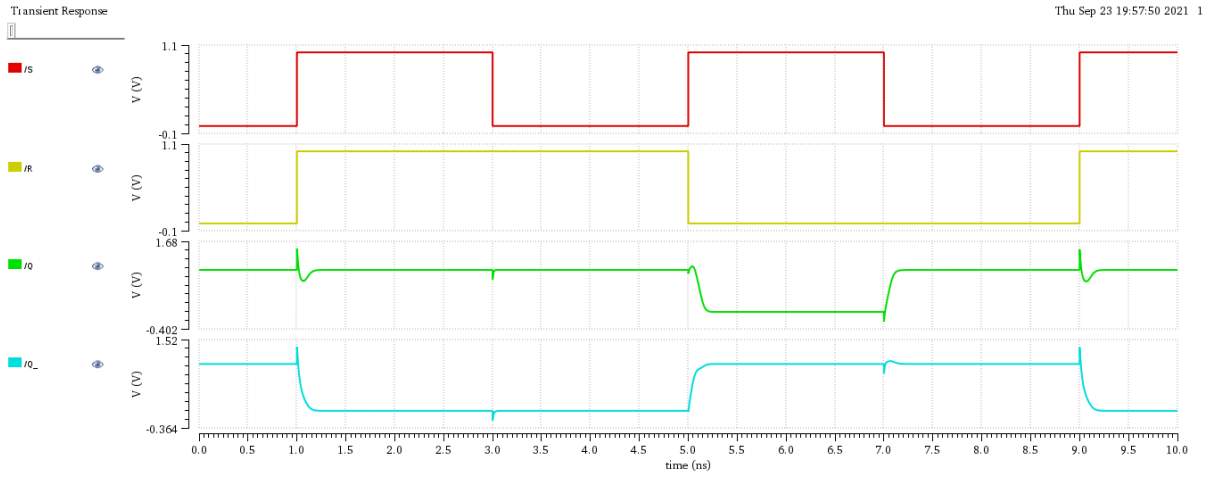
5.2 Layout



5.3 Pre-Layout Simulation



5.4 Post-Layout Simulation



5.5 Timing Information

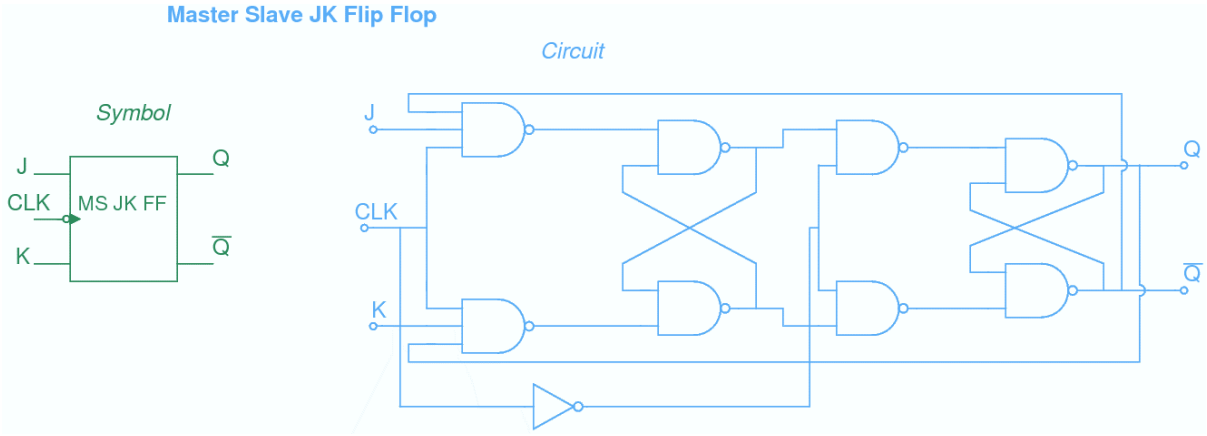
Input S: Time period = 4 ns

Input R: Time Period = 8 ns

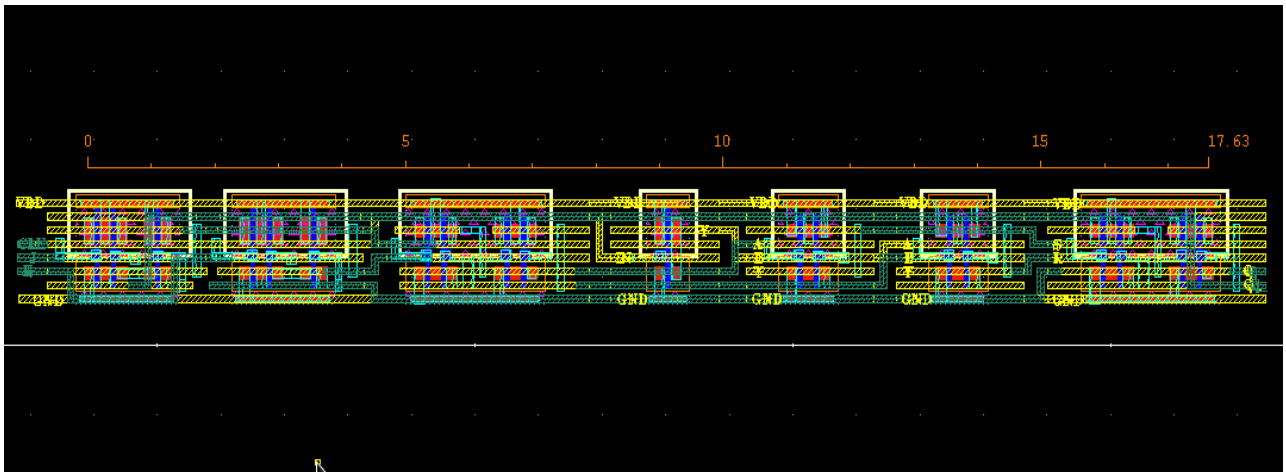
		Rise Time **Tr**	Fall Time T_f	T_{PHL}	T_{PLH}	Propagation Delay T_P
Pre-Layout	Q	33.441	30.716	42.9261	20.649	31.78755
	Q'	29.886	28.4106	12.797	15.236	14.0165
Post-Layout	Q	86.016	89.4688	119.1474	51.995	85.5712
	Q'	107.6638	100.3943	41.472	37.6599	39.56595

6. Master Slave JK Flip Flop

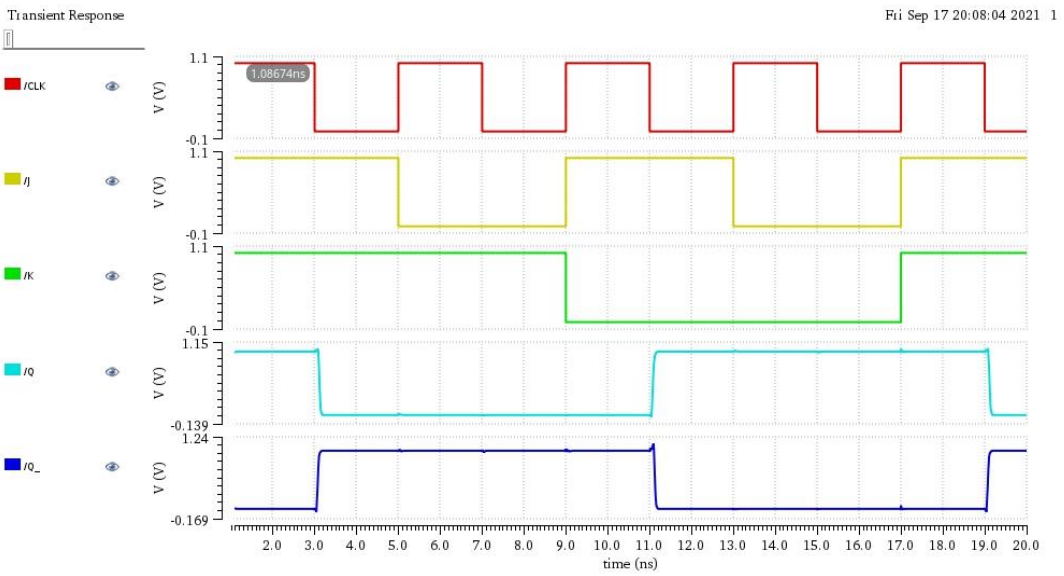
6.1 Schematic



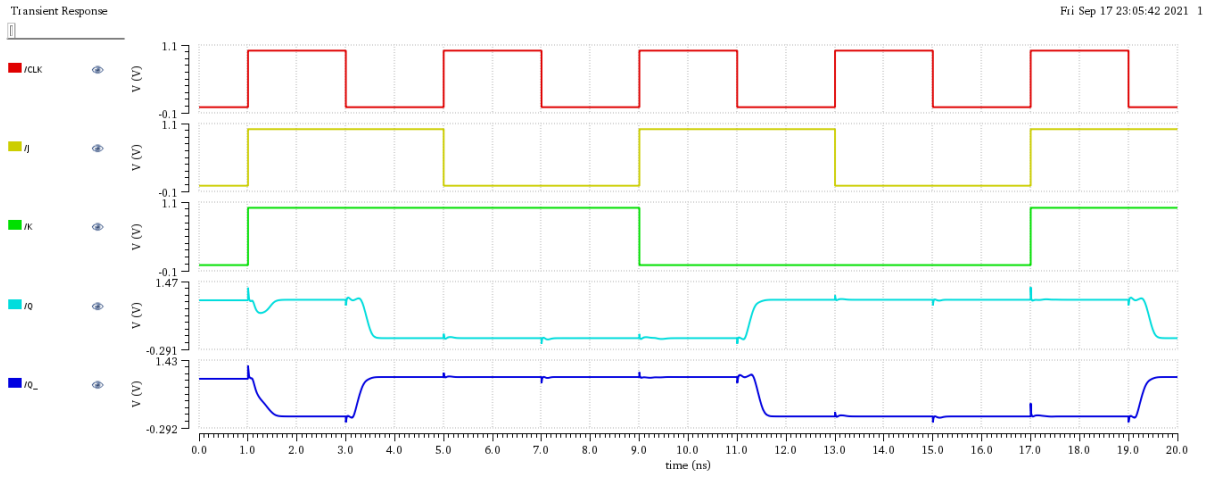
6.2 Layout



6.3 Pre-Layout Simulation



6.4 Post-Layout Simulation



6.5 Timing Information

Clock: Time Period = 4 ns

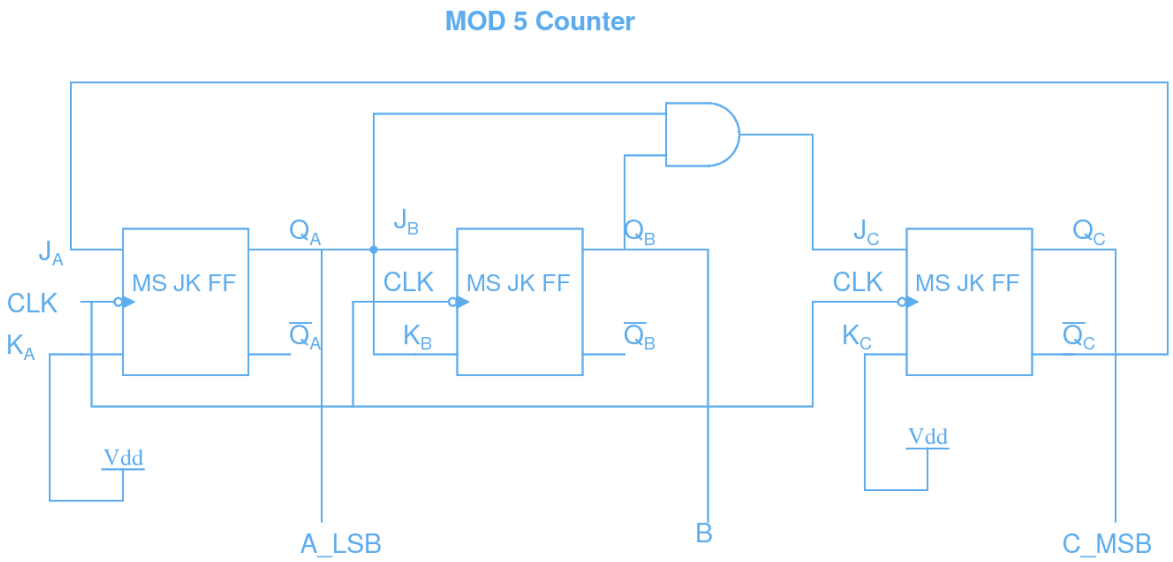
Input J: Time period = 8 ns

Input K: Time Period = 16 ns

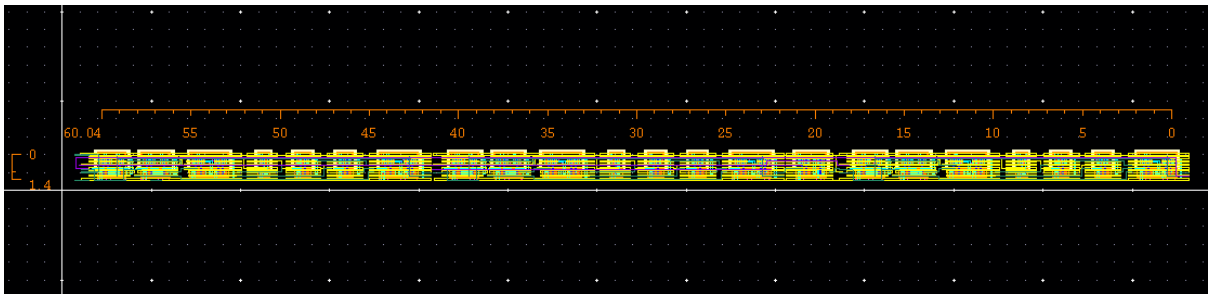
		Rise Time **Tr**	Fall Time **T_f**	**T_{PHL}**	**T_{PLH}**	Propagation Delay **T_P**
Pre-Layout	Q	59.7506	48.5045	115.9917	77.4671	96.7294
	Q’	46.893	44.55	125.46	77.026	101.243
Post-Layout	Q	218.3845	197.776	433.054	272.882	352.968
	Q’	231.644	198.019	448.1077	269.622	358.8649

7. Mod-5 Synchronous Counter

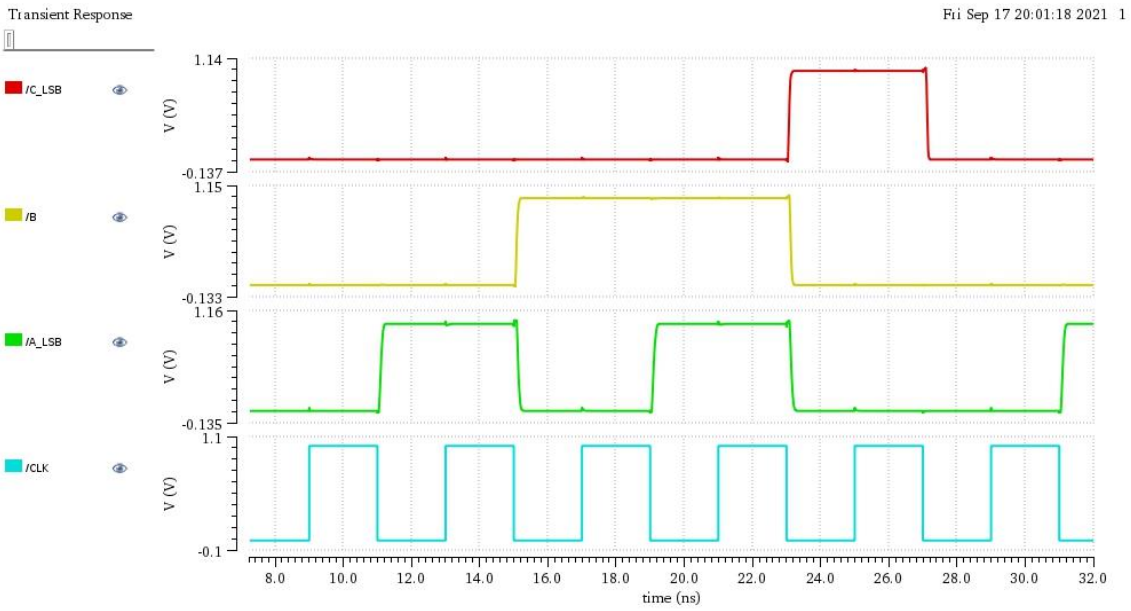
7.1 Schematic



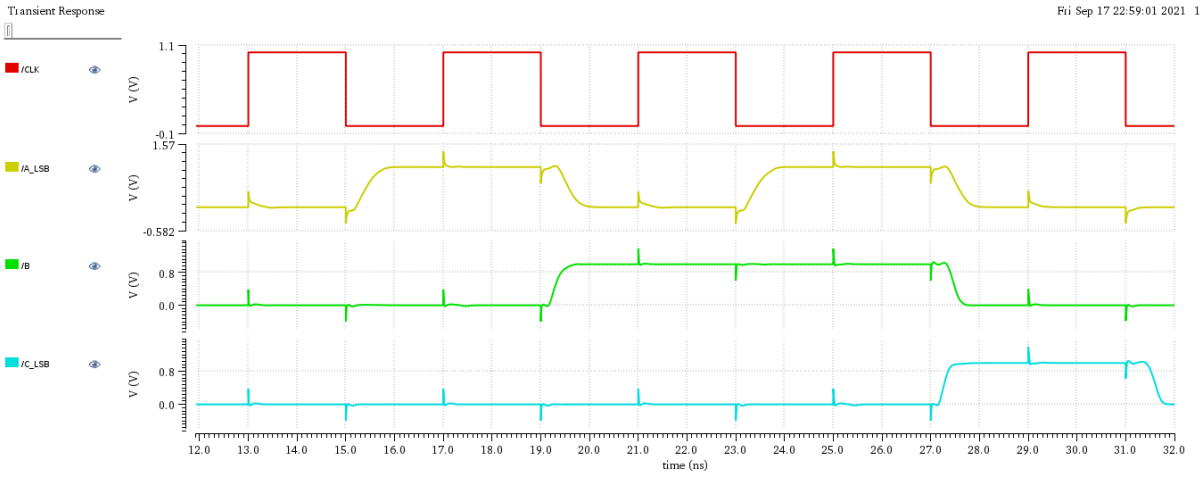
7.2 Layout



7.3 Pre-Layout Simulation



7.4 Post-Layout Simulation



7.5 Timing Information

Clock: Time Period = 4 ns

		Rise Time **Tr**	Fall Time **T_f**	**T_{PHL}**	**T_{PLH}**	Propagation Delay **T_P**
Pre-Layout	A_LSB	100.5987	94.998	139.554	101.373	120.4635
	B	80.721	65.31715	122.876	85.799	104.3375
	C_MSB	58.8039	51.125	127.546	77.524	102.535
Post-Layout	A_LSB	478.85	400.439	557.328	423.762	490.545
	B	306.617	246.138	478.938	303.247	391.0925
	C_MSB	211.729	247.758	604.542	278.4579	441.5

Setup Time

Setup Time: The amount of time the data at the synchronous input (j, k) must be stable before the active edge of clock

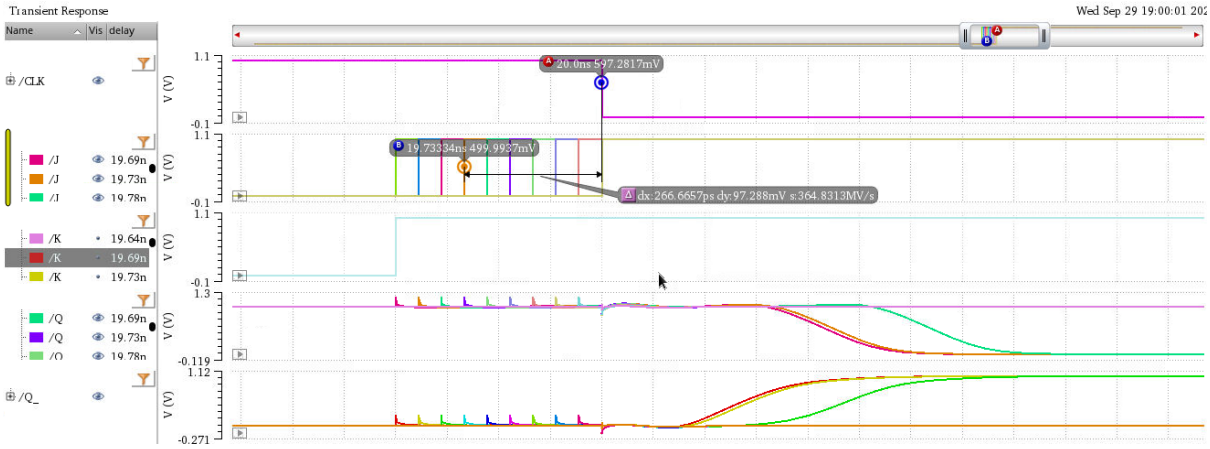
Hold Time: The amount of time the data at the synchronous input (j, k) must be stable after the active edge of clock.

Setup Time Calculation

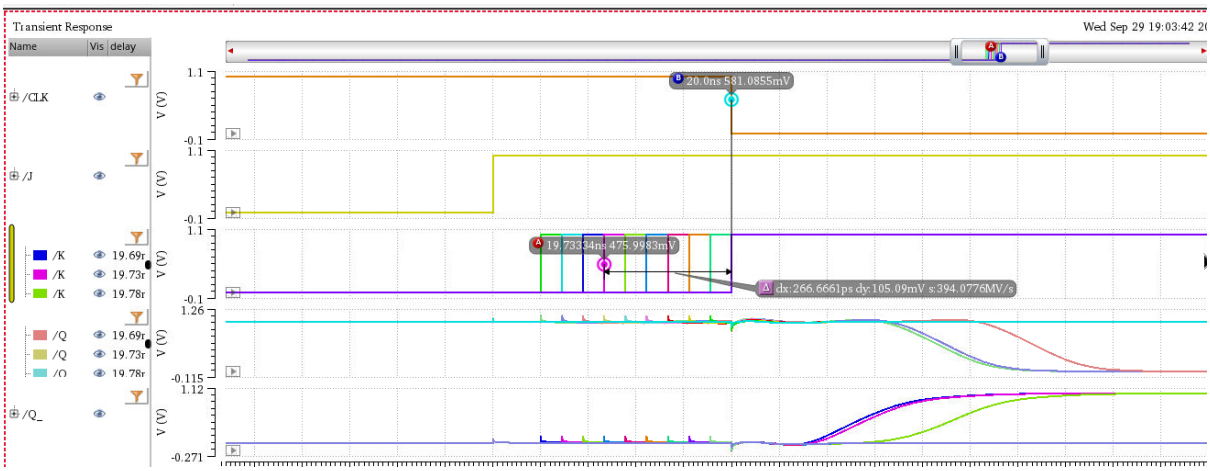
Procedure: first input K is given a setup signal and input J is varied from 0 -> 1 with variable delay. This variable delay is varied with different values around active (negative) edge of the clock to see for which delay, output remains the same i.e., output doesn't change. This delay is the setup time of corresponding to input J.

Similar procedure is done for input K.

Here Input J is sweeped and setup time is 266.66ps



Here input K is sweeped and setup time is 266.66ps

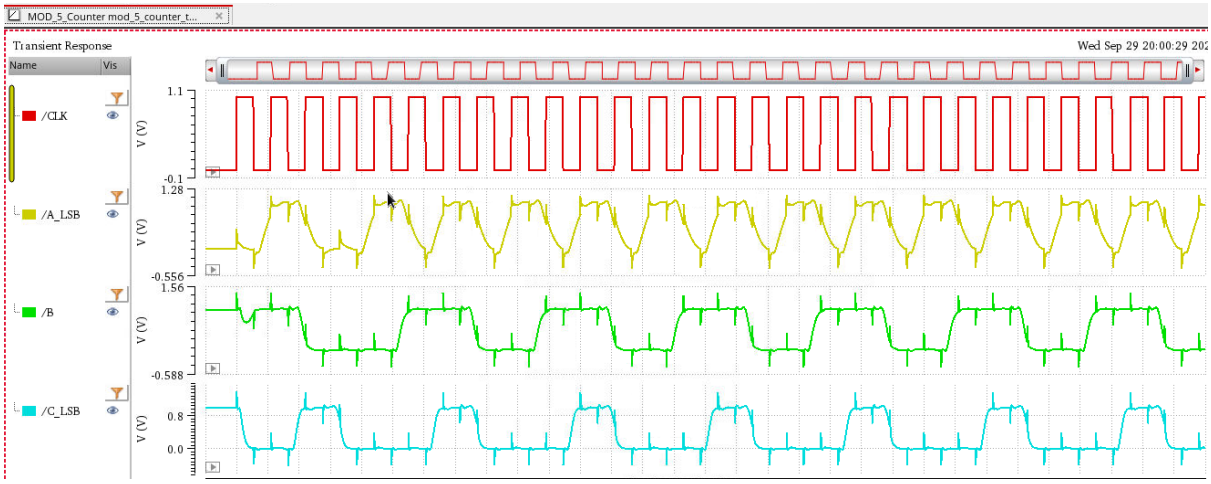


Therefore, setup time = max (266.66, 266.66) ps.

Setup Time = 266.66 ps.

Max Frequency

After 909 MHz output of counter becomes too noisy.



Targets Achieved

- Designed Mod-5 Synchronous UP counter using Master slave JK flip flop
- Width of Master slave JK Flip Flop = **17.63 um**
- Width of Mod-5 synchronous counter = **60.04 um**
- Maximum frequency **= 909 MHz**
- DRC, LVS and PEX is performed for every component without any errors.