MOD 5 Counter

RTL to GDSII Flow

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Objective

- RTL to GSDII Flow for mod 5 Counter
- Synthesis and physical design of mod 5 counter

GitHub Link and Server Path

GitHub Link: GitHub Link

Sever Path: EEN212023

Folder Structure

This is my folder structure which shows all the files and folder before starting any process.

```
PhysicalDesign_65nm
          LEF_file
                    trial_gcd.lef
          timing_lib
                    uk65lscllmvbbr_090c125_wc_ccs.lib
                    uk65lscllmvbbr_110c-40_bc_ccs.lib
          counter
                    rtl
                              counter.v
                              counter_tb.v
                    synthesis
                              counter.tcl
                              counter.sdc
                    physical_design
                              Default.view
           qrcTechFile.tch
           power_rail_commands
```

Verilog Code and Testbench

Verilog Code is located at PhysicalDesign_65nm -> counter -> rtl -> counter.v

```
`timescale 1ns / 1ps

module counter(
        clk,
        rst,
        count
    );

    parameter MOD = 5;                  // Mod value
    input clk;                          // Clock signal
    input rst;                          // Reset signal
    output reg [2:0] count;             // Three-bit output

    always@(negedge clk) begin          // Falling edge of the clock

        if(!rst || count == MOD-1)      // count = 0, if reset is low or
            count<=0;                   // When count = 4

        else                            // Increment the value of count
            count<=count+1;
    end

endmodule
```

Test Bench code is located at PhysicalDesign_65nm -> counter -> rtl -> counter_tb.v

```
`timescale 1ns / 1ps

module counter_tb();

    reg clk;
    reg rst;
    wire [2:0] count;

    initial begin
        clk=0;              // start clock with low value
        rst=0; #20;         // keep reset = 0 for 20 ns
        rst=1; #100;        // then making reset = 1 for 100 ns
        $finish;            // stop the simulation after 120 ns
    end

// instantiating module counter here

    counter DUT (.clk(clk),
                 .rst(rst),
                 .count(count));

    always #5 clk = ~clk;   // generating clock signal with period = 10 ns

endmodule
```

TCL File

TCL file is located at PhysicalDesign_65nm -> counter -> synthesis -> counter.tcl

```
set search_path
"/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs"
set_attribute lib_search_path
"/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs"
set_attribute hdl_search_path "../rtl/"
set_attribute library "uk65lscllmvbbr_100c25_tc_ccs.lib"

read_hdl counter.v
elaborate
check_design -unresolved
read_sdc counter.sdc
synthesize -to_mapped -effort medium
write_hdl > ../physical_design/counter_netlist.v
write_sdc > ../physical_design/counter_sdc.sdc

write_sdf -timescale ns -nonegchecks -recrem split -edges check_edge  -setuphold
split > delays.sdf
```

Above counter.tcl file contains list of commands to generate Verilog code and sdc file to be used in the next stage of physical design. Output files will be stored in physical_design folder.

SDC File

SDC File is located at PhysicalDesign_65nm -> counter -> synthesis -> counter.sdc

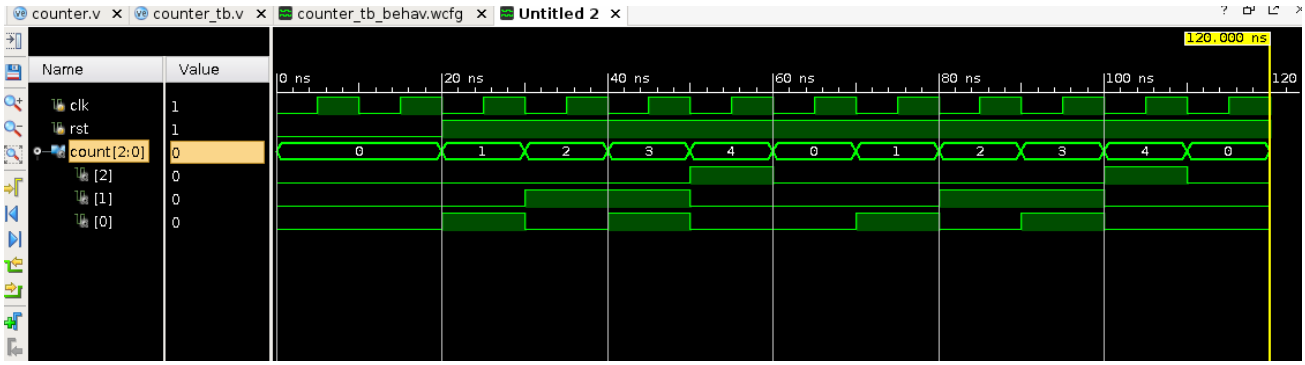
```
set sdc_version 1.7

set_units -capacitance 1000fF
set_units -time 1000ps

# Set the current design
current_design counter

create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainity 0.1 [get_ports "clk"]

set_input_delay -max 1.0 [get_ports "rst"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "count"] -clock [get_clocks "clk"]

set_wire_load_mode "top"
```

Above counter.sdc file specifies the timing constraints on clock period, clock rise time, clock fall time and delay for reset and count signals

Simulation of Verilog Code

Waveform

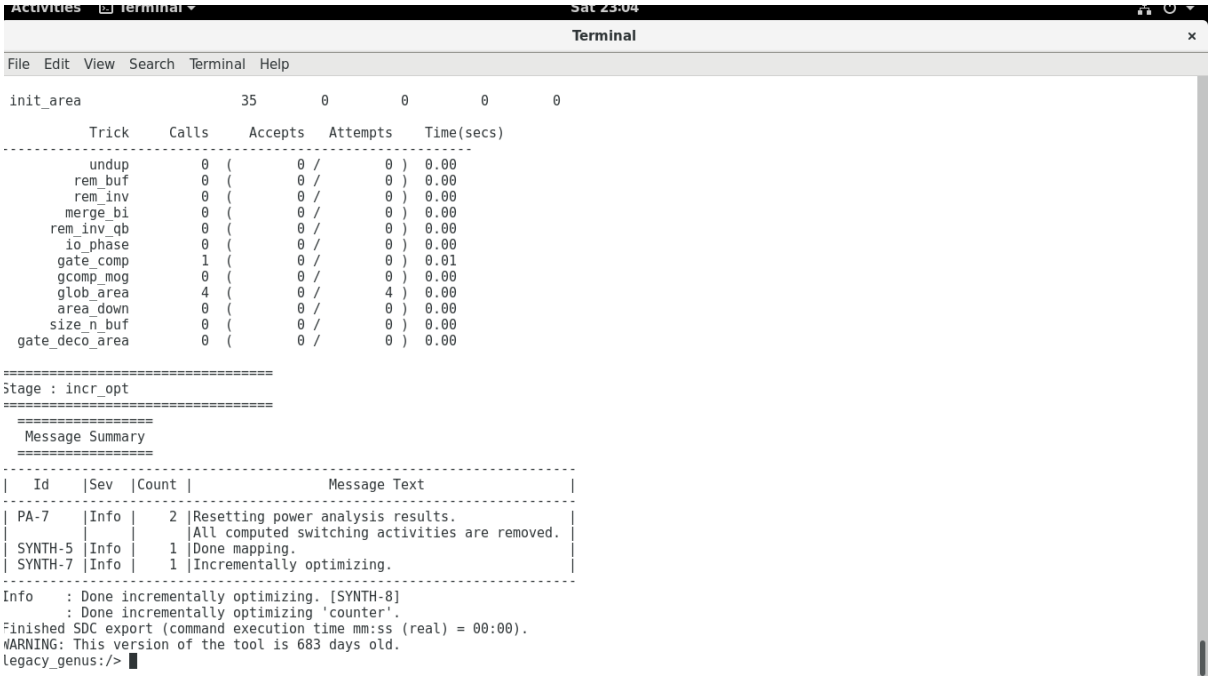
counter.v and counter_tb.v is used for simulation. 3-bit output goes from 0 to 4 when reset signal is high otherwise output remains zero.



Synthesis

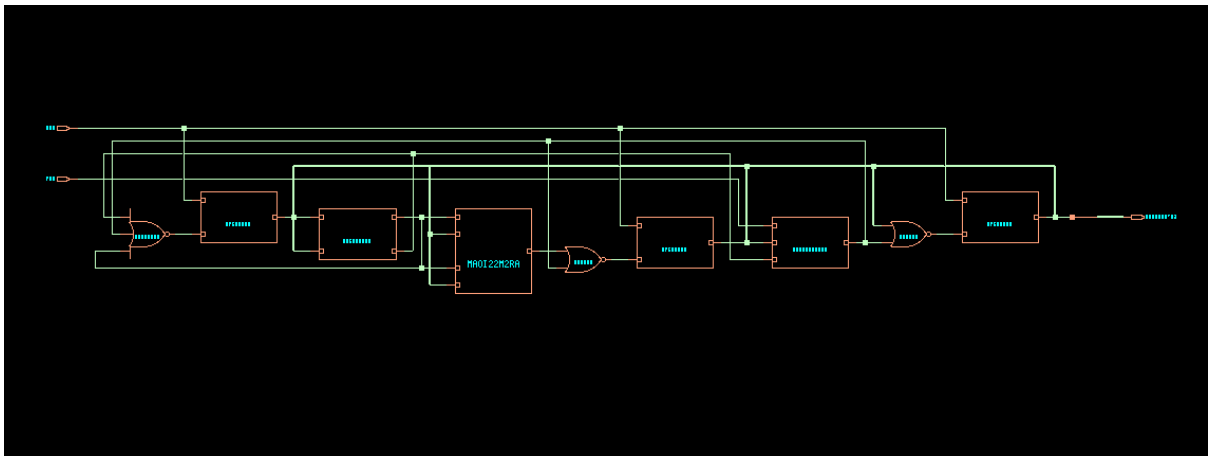
```
cd synthesis
load_module encounter
rc -f counter.tcl
```

Output of above commands



Gate level Netlist in GUI

gui_show

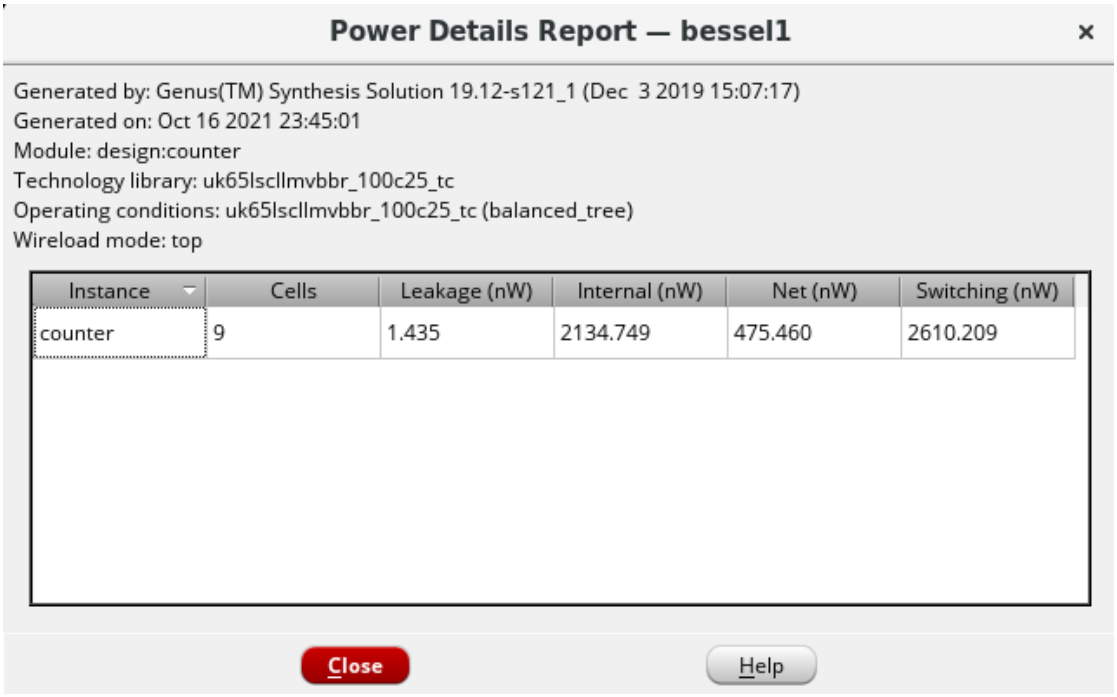


Timing Report

```
report_timing_summary
legacy_genus:/> report_timing
Warning : Timing problems have been detected in this design. [TIM-11]
        : The design is 'counter'.
============================================================
  Generated by:           Genus(TM) Synthesis Solution 19.12-s121_1
  Generated on:           Oct 16 2021  11:46:50 pm
  Module:                 counter
  Technology library:     uk65lscllmvbbr_100c25_tc
  Operating conditions:   uk65lscllmvbbr_100c25_tc (balanced_tree)
  Wireload mode:          top
  Area mode:              timing library
============================================================

          Pin                      Type       Fanout Load Slew Delay Arrival
                                                     (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------------------------
(clock clk)                    launch                                  5000 F
count_reg[0]/CKB                                          100          5000 F
count_reg[0]/Q                 DFCQM2RA           3  3.8   52  +229    5229 R
count[0]                 <<<   interconnect               52    +0    5229 R
                               out port                        +0    5229 R
(counter.sdc_line_18_2_1)      ext delay                    +1000    6229 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock clk)                    capture                                10000 R
-------------------------------------------------------------------------------
Cost Group   : 'clk' (path_group 'clk')
Timing slack :    3771ps
Start-point  : count_reg[0]/CKB
End-point    : count[0]

legacy_genus:/>
```

Power Report

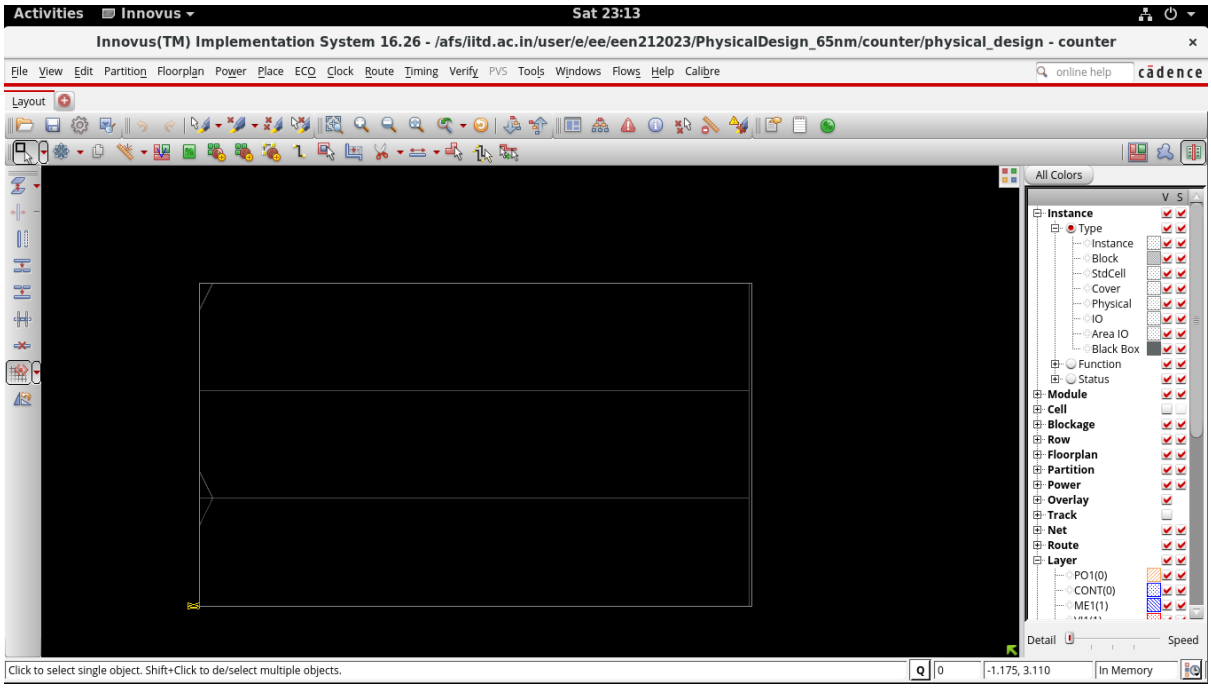
```
legacy_genus:/> report power
Info    : Joules engine is used. [RPT-16]
        : Joules engine is being used for the command report_power.
Instance: /counter
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total     Row%
  ------------------------------------------------------------------------------
       memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     register     9.61831e-10  1.95137e-06  1.01284e-07  2.05362e-06  78.63%
        latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        logic     4.73233e-10  1.83381e-07  1.64176e-07  3.48030e-07  13.33%
         bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        clock     0.00000e+00  0.00000e+00  2.10000e-07  2.10000e-07   8.04%
          pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
           pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------------
    Subtotal     1.43506e-09  2.13475e-06  4.75460e-07  2.61165e-06 100.00%
  Percentage           0.05%       81.74%       18.21%      100.00% 100.00%
  ------------------------------------------------------------------------------
legacy_genus:/>
```



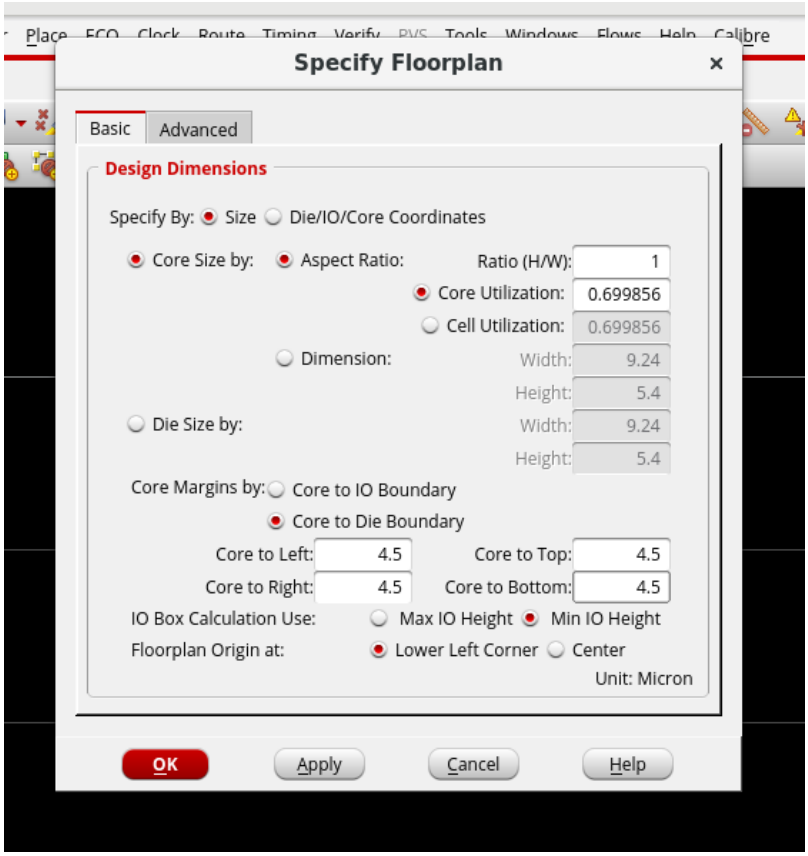
Physical Design

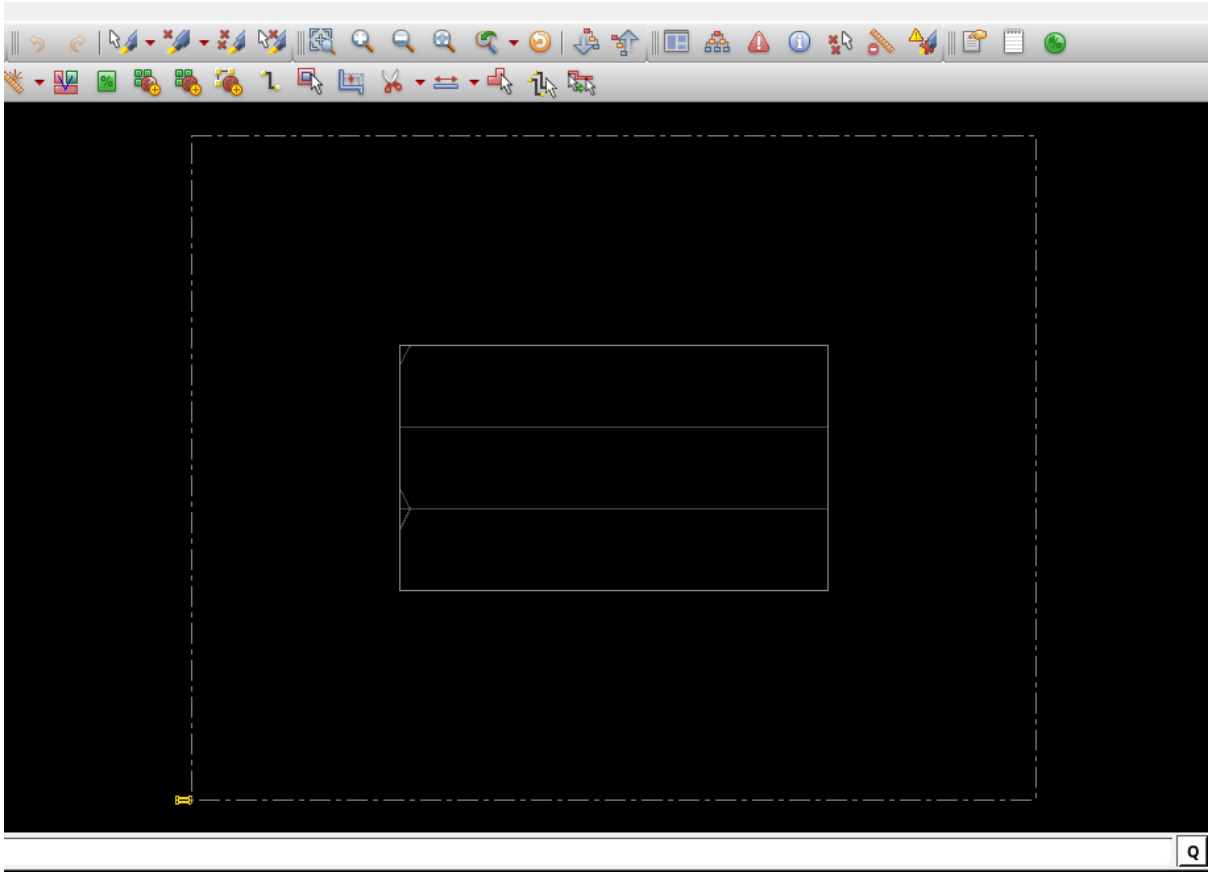
Step by step process of physical design has been described in this section

```
encounter
```



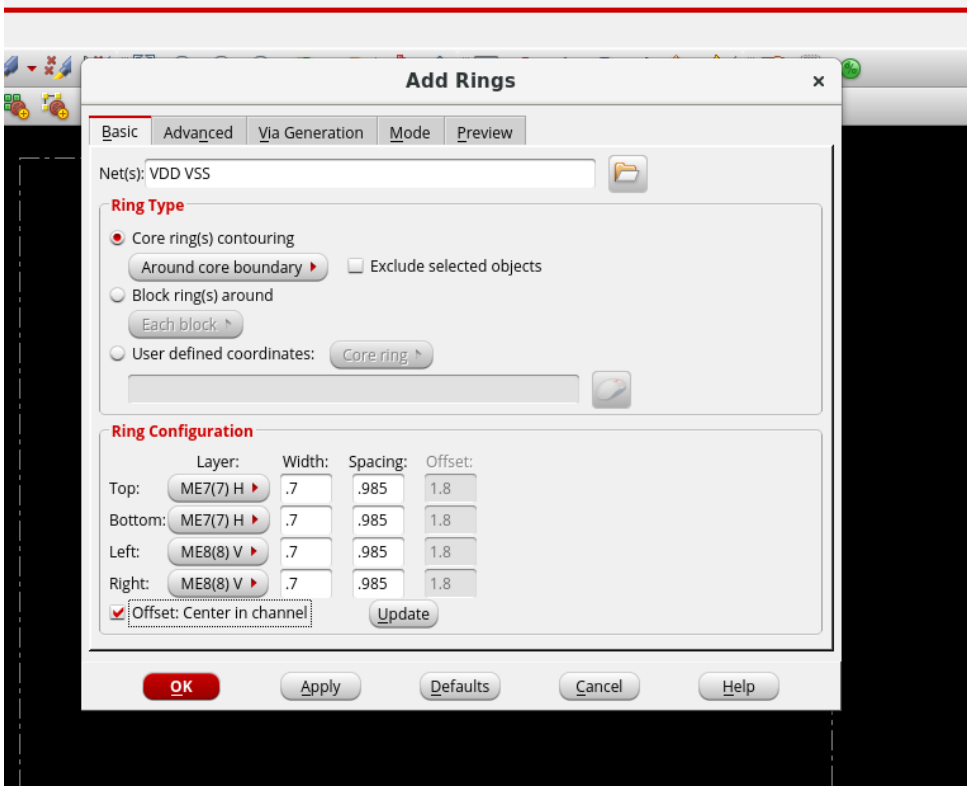
Floor planning

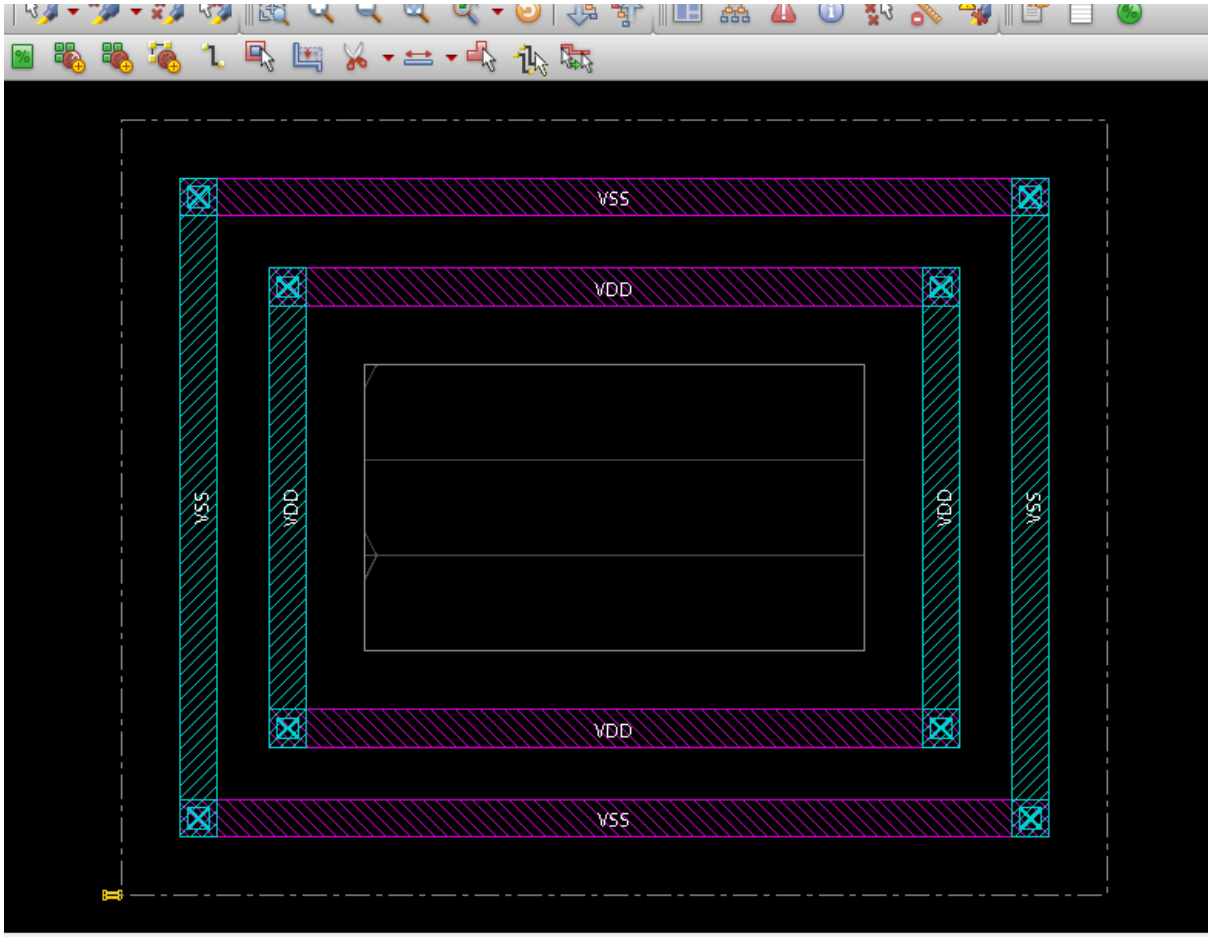




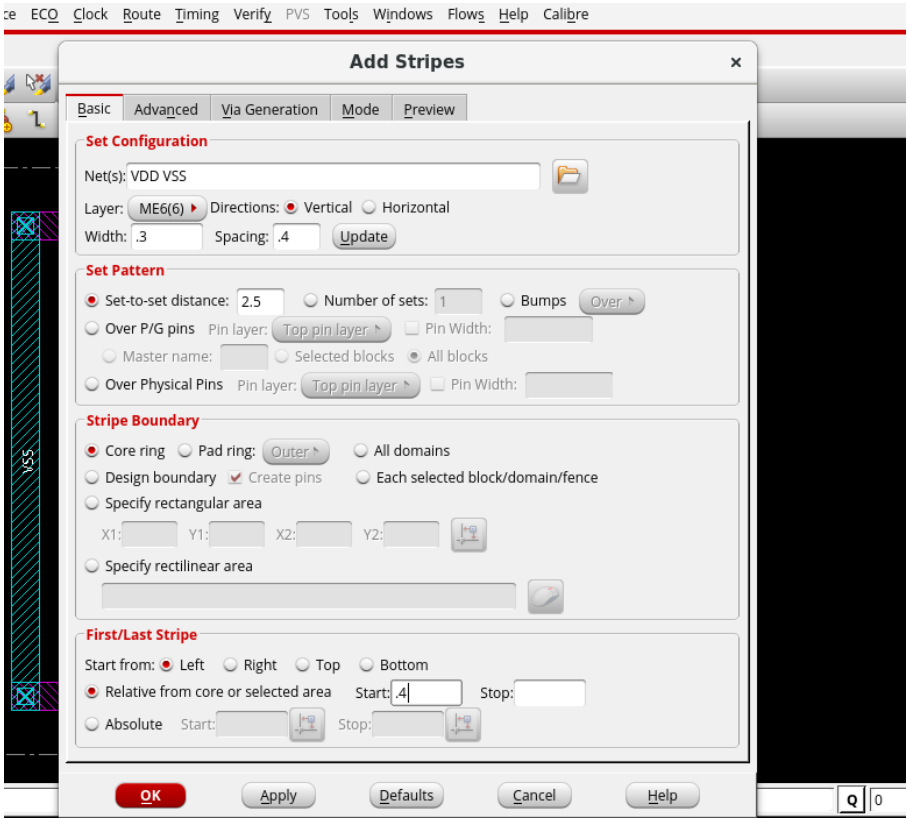
Power Planning

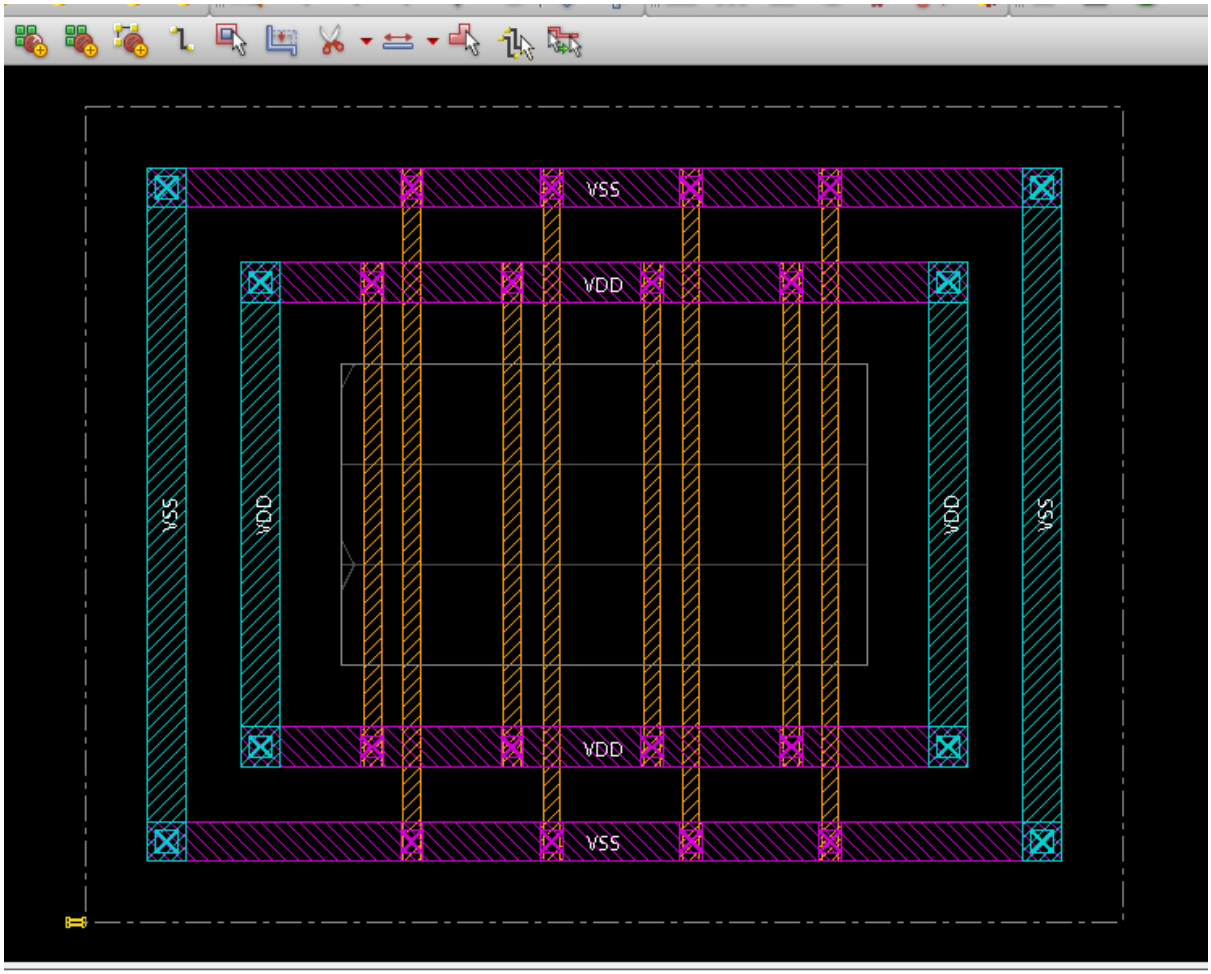
Rings




VSS
VDD
VSS
VDD
VDD
VSS
VDD
VSS

Stripes


ce ECO Clock Route Timing Verify PVS Tools Windows Flows Help Calibre
Add Stripes
Basic
Advanced
Via Generation
Mode
Preview
Set Configuration
Net(s): VDD VSS
Layer: ME6(6)
Directions: Vertical Horizontal
Width: .3
Spacing: .4
Update
Set Pattern
Set-to-set distance: 2.5
Number of sets: 1
Bumps
Over
Over P/G pins
Pin layer:
Top pin layer
Pin Width:
Master name:
Selected blocks
All blocks
Over Physical Pins
Stripe Boundary
Core ring
Pad ring:
Outer
All domains
Design boundary
Create pins
Each selected block/domain/fence
Specify rectangular area
X1:
Y1:
X2:
Y2:
Specify rectilinear area
First/Last Stripe
Start from: Left Right Top Bottom
Relative from core or selected area
Start: .4
Stop:
Absolute
OK
Apply
Defaults
Cancel
Help
VSS



Terminal output

Terminal

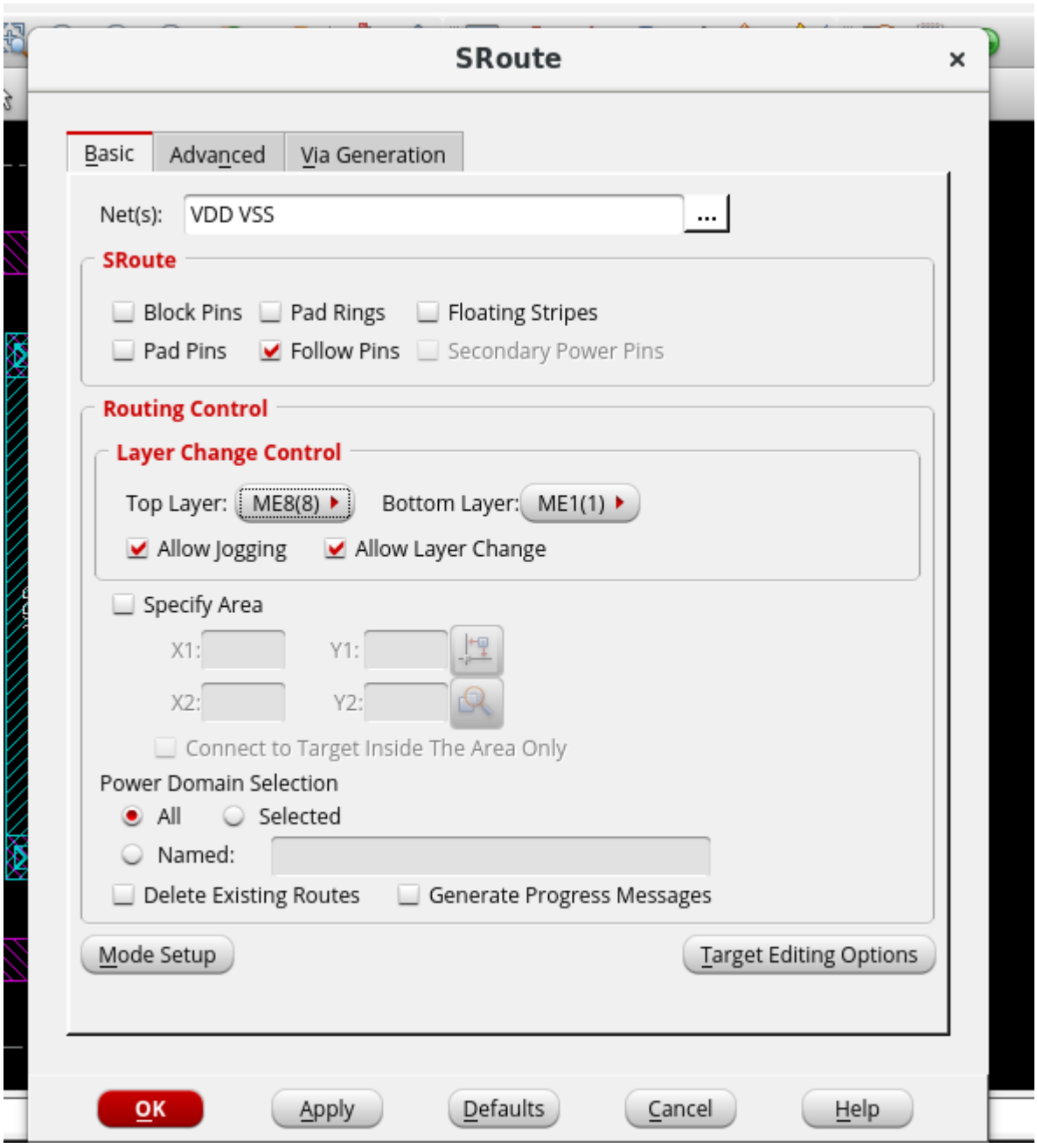
File Edit View Search Terminal Help

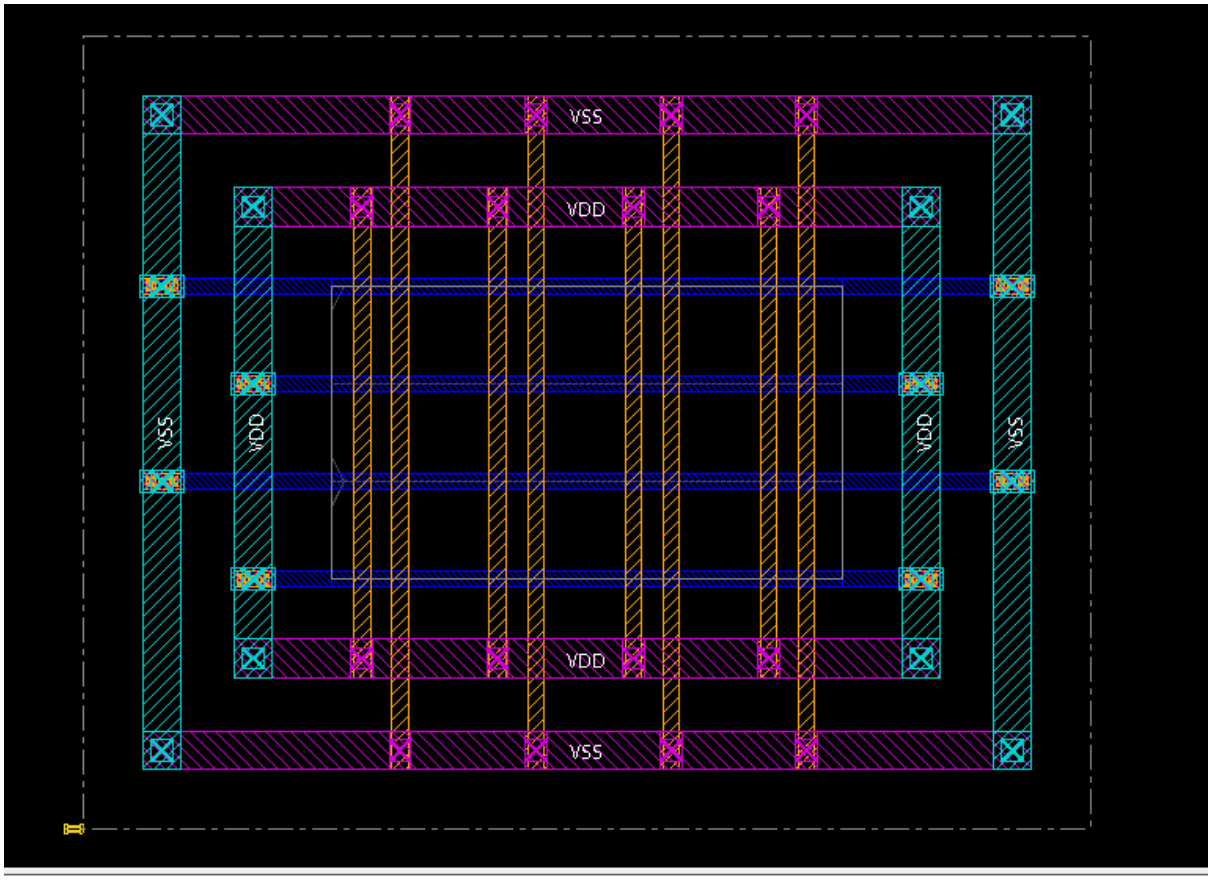
```
addRing created 8 wires.
ViaGen created 8 vias, deleted 0 via to avoid violation.
+--------+----------------+----------------+
|  Layer |     Created    |     Deleted    |
+--------+----------------+----------------+
|   ME7  |        4       |       NA       |
|   VI7  |        8       |        0       |
|   ME8  |        4       |       NA       |
+--------+----------------+----------------+
innovus 1> addStripe will allow jog to connect padcore ring and block ring.
Stripes will stop at the boundary of the specified area.
When breaking rings, the power planner will consider the existence of blocks.
Stripes will not extend to closest target.
The power planner will set stripe antenna targets to none (no trimming allowed).
Stripes will not be created over regions without power planning wires.
The entire stripe set will break at the domain if one of the nets is not in the domain.
addStripe will break automatically at non-default domains when generating global stripes over
AddStripe segment minimum length set to 1
Offset for stripe breaking is set to 0.

**WARN: (IMPPP-193):    The currently specified  spacing 0.4000 in -spacing option might crea
```

Creating Power rails with special route

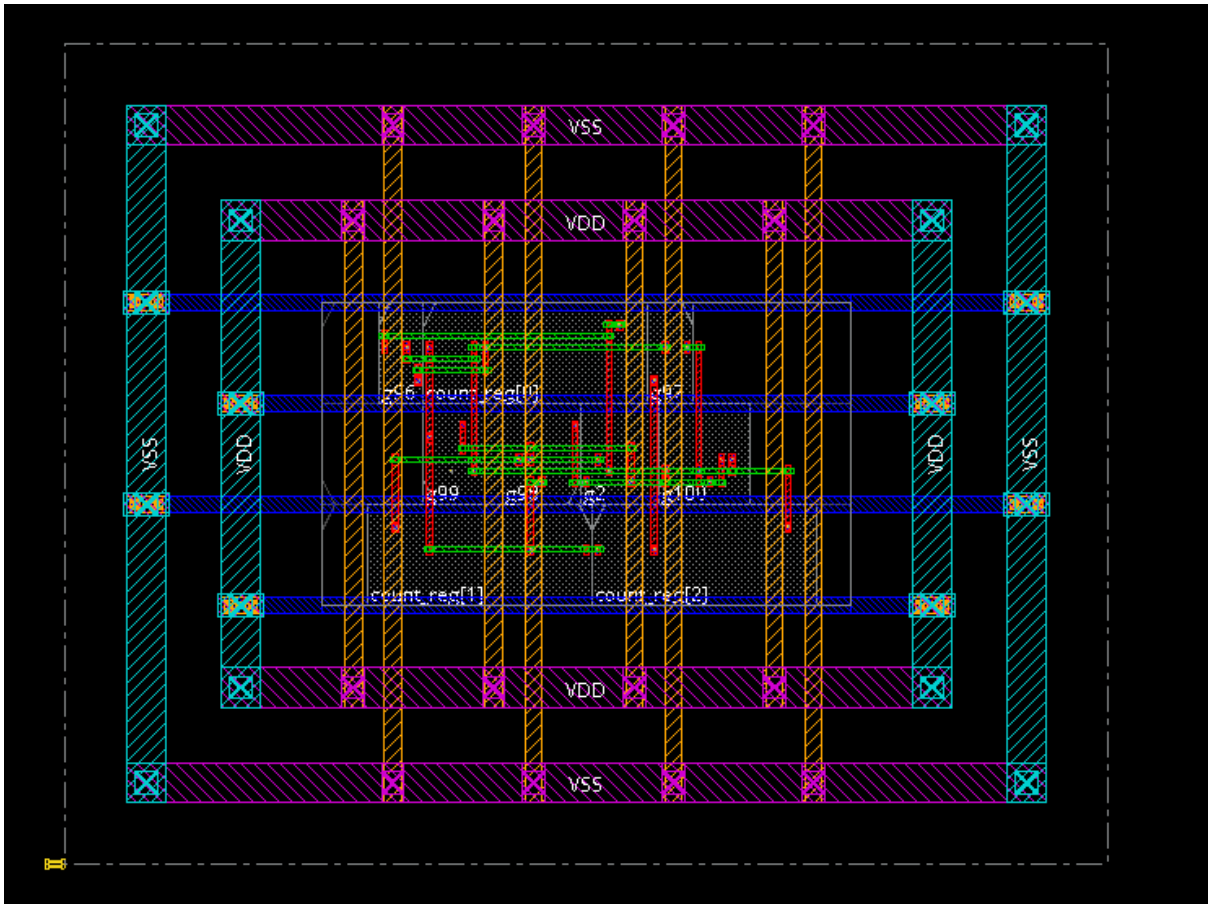
```
globalNetConnect VDD -type pgpin -pin VDD -instanceBasename *
globalNetConnect VSS -type pgpin -pin VSS -instanceBasename *
```

Special Route

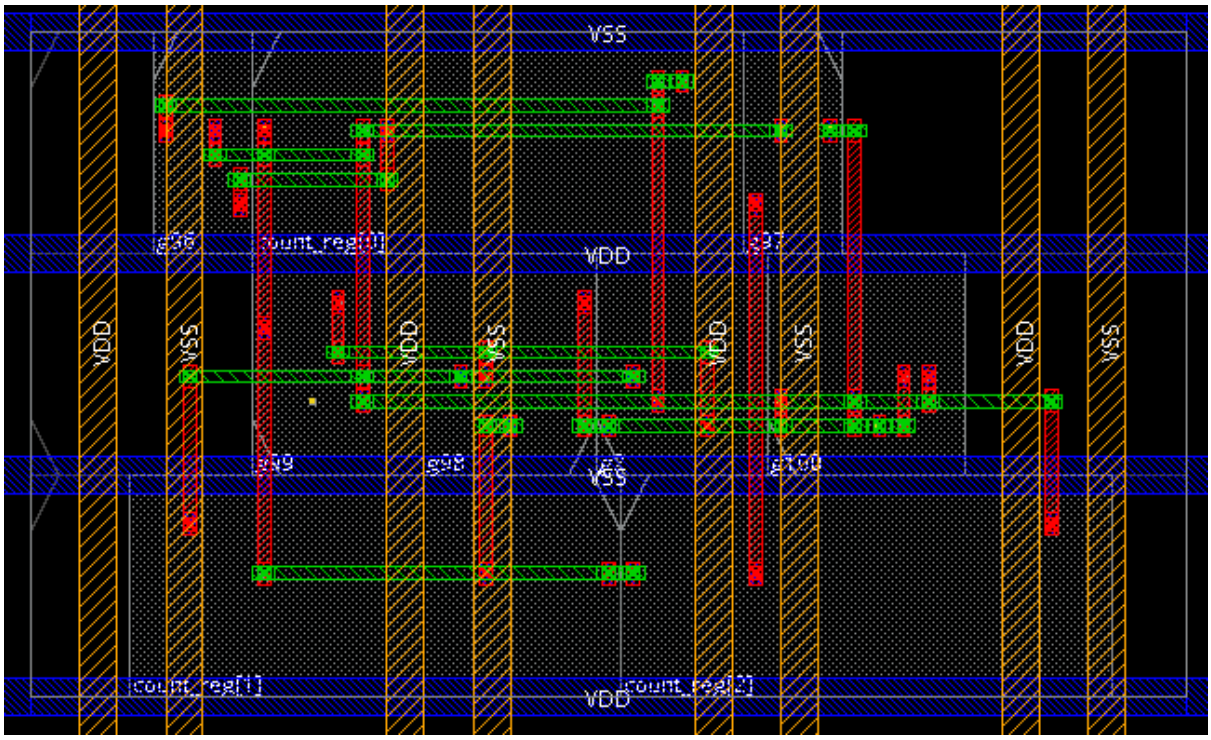




Standard Cell



Zoomed view of the core



Pre-CTS Timing Report

Setup Time

```
Activities  Terminal                                   Sat 23:28
                                                      Terminal
File  Edit  View  Search  Terminal  Help
*** Done Building Timing Graph (cpu=0:00:00.2 real=0:00:01.0 totSessionCpu=0:04:15 mem=2110.7M)

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 worst_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  3.583  |  9.216  |  3.583  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    6    |    3    |    6    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 68.794%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.33 sec
Total Real time: 1.0 sec
Total Memory Usage: 2055.429688 Mbytes
innovus 3>
```

Hold Time

Terminal

File Edit View Search Terminal Help

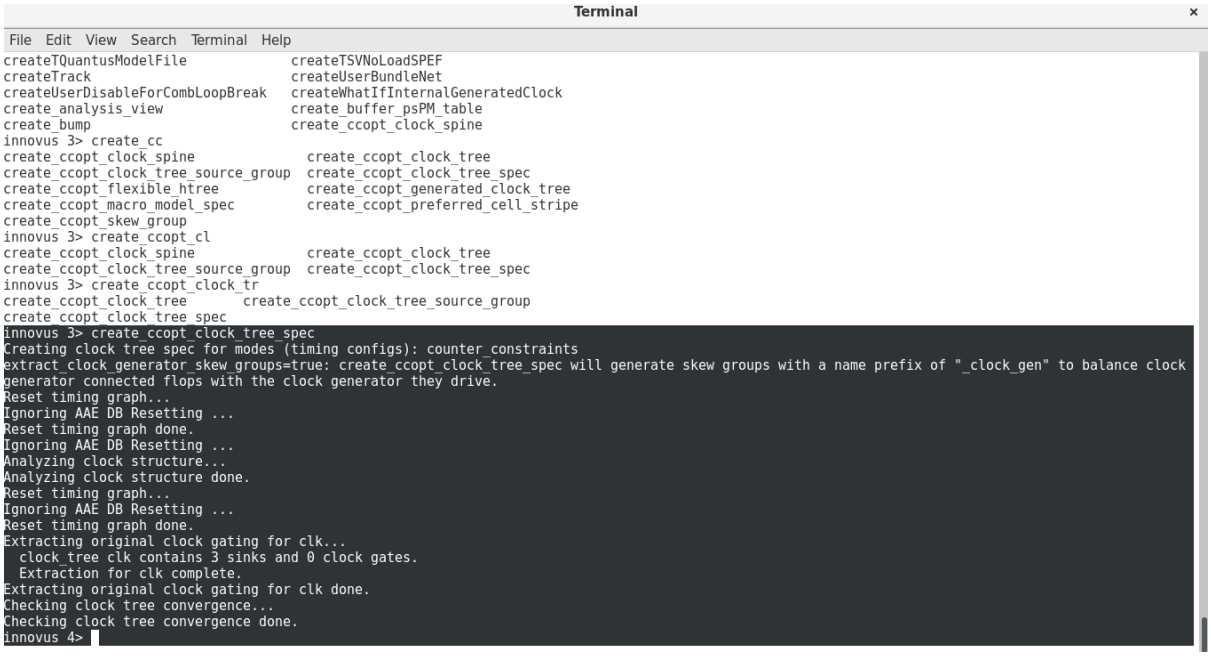
```
# Design Mode: 90nm
# Analysis Mode: MMMC Non-OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#################################################################################
AAE_INFO: 1 threads acquired from CTE.
Calculate delays in BcWc mode...
*** Calculating scaling factor for min_timing_library libraries using the default operating condition of each library.
Total number of fetched objects 12
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2111.16 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.2 real=0:00:01.0 totSessionCpu=0:04:24 mem=2111.2M)

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 best_case

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.102  |  0.102  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    3    |    3    |    0    |
+--------------------+---------+---------+---------+

Density: 68.794%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.42 sec
Total Real time: 1.0 sec
Total Memory Usage: 2029.234375 Mbytes
innovus 3>
```

Note: No violating path in Pre-CTS timing report for setup and hold time

Clock Tree Synthesis

```
Create_ccopt_clock_tree_spec
Ccopt_design
```

Terminal output of above commands



Post-CTS Timing Report

Setup Time

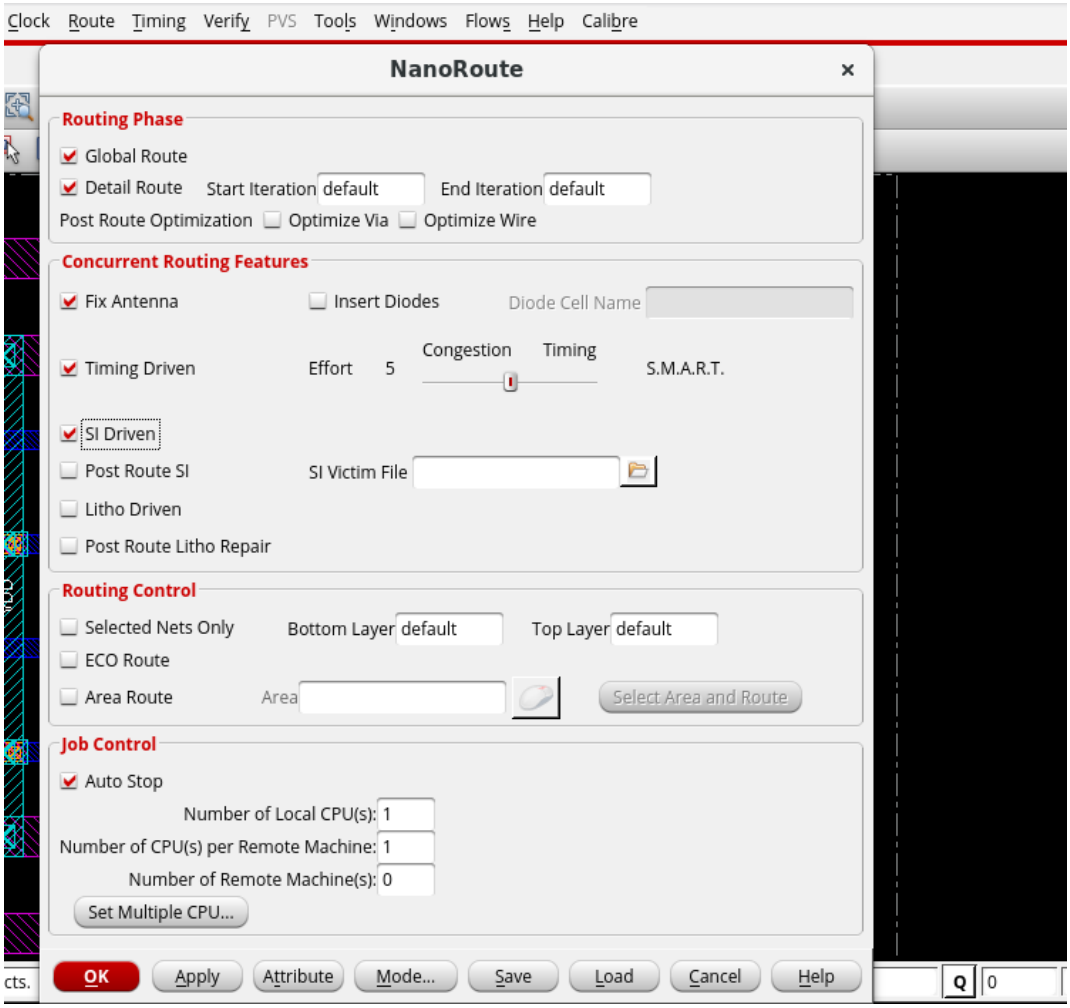
```
File  Edit  View  Search  Terminal  Help
*** Done Building Timing Graph (cpu=0:00:00.2 real=0:00:01.0 totSessionCpu=0:05:08 mem=2230.9M)
Reported timing to dir ./timingReports
**optDesign ... cpu = 0:00:09, real = 0:00:10, mem = 2175.7M, totSessionCpu=0:05:08 **

------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

Setup views included:
 worst_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  3.628  |  9.216  |  3.628  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    6    |    3    |    6    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 68.794%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
**optDesign ... cpu = 0:00:09, real = 0:00:10, mem = 2173.7M, totSessionCpu=0:05:08 **
*** Finished optDesign ***
External::optDesign done. (took cpu=0:00:14.0 real=0:00:14.2)
Runtime done. (took cpu=0:00:25.8 real=0:00:25.8)
```

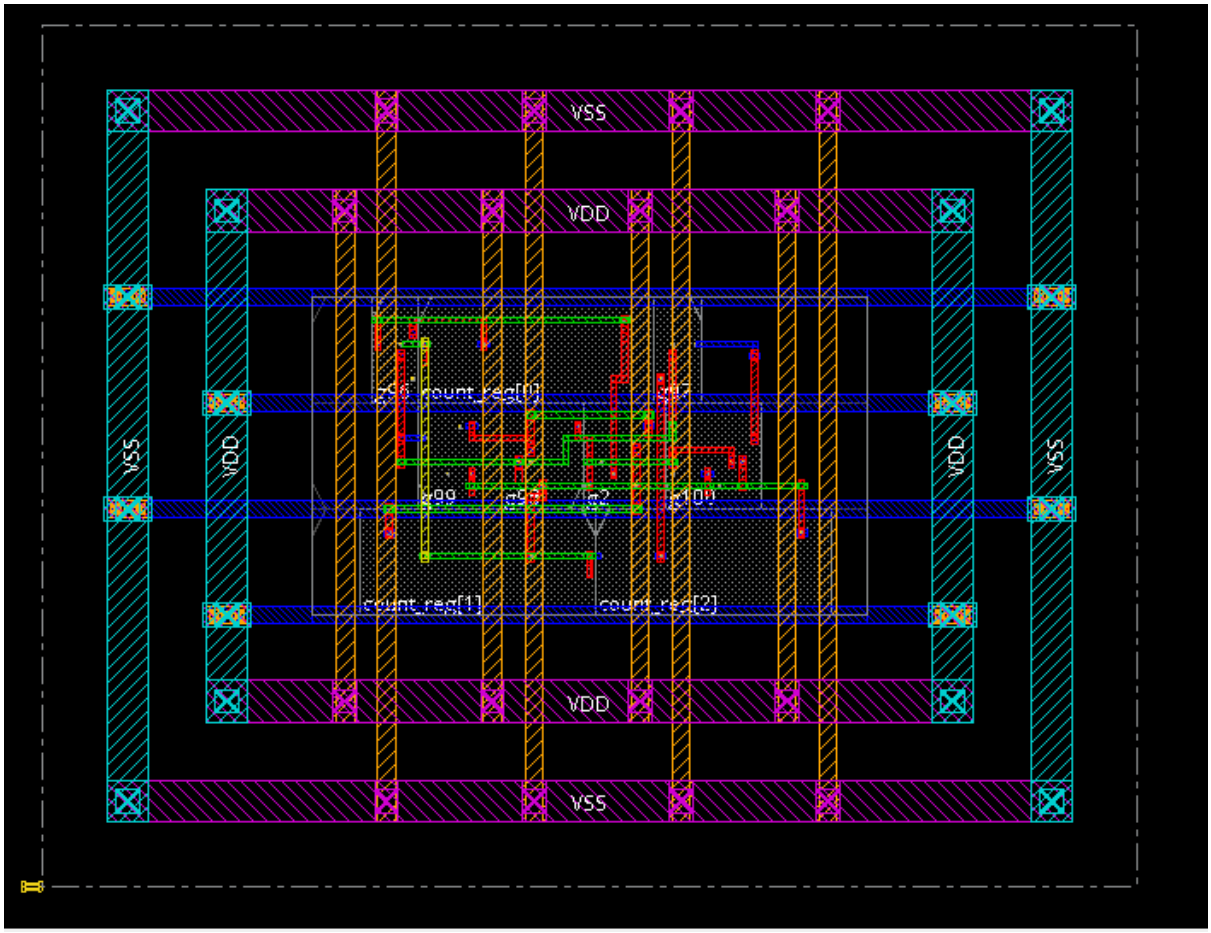
Hold Time

```
Terminal
File  Edit  View  Search  Terminal  Help
# Design Mode: 90nm
# Analysis Mode: MMMC Non-OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#################################################################################
AAE_INFO: 1 threads acquired from CTE.
Calculate delays in BcWc mode...
*** Calculating scaling factor for min_timing_library libraries using the default operating condition of each library.
Total number of fetched objects 12
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2164.24 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.2 real=0:00:00.0 totSessionCpu=0:05:38 mem=2164.2M)

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 best_case

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.099  |  0.099  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    3    |    3    |    0    |
+--------------------+---------+---------+---------+

Density: 68.794%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.35 sec
Total Real time: 1.0 sec
Total Memory Usage: 2084.859375 Mbytes
innovus 5>
```

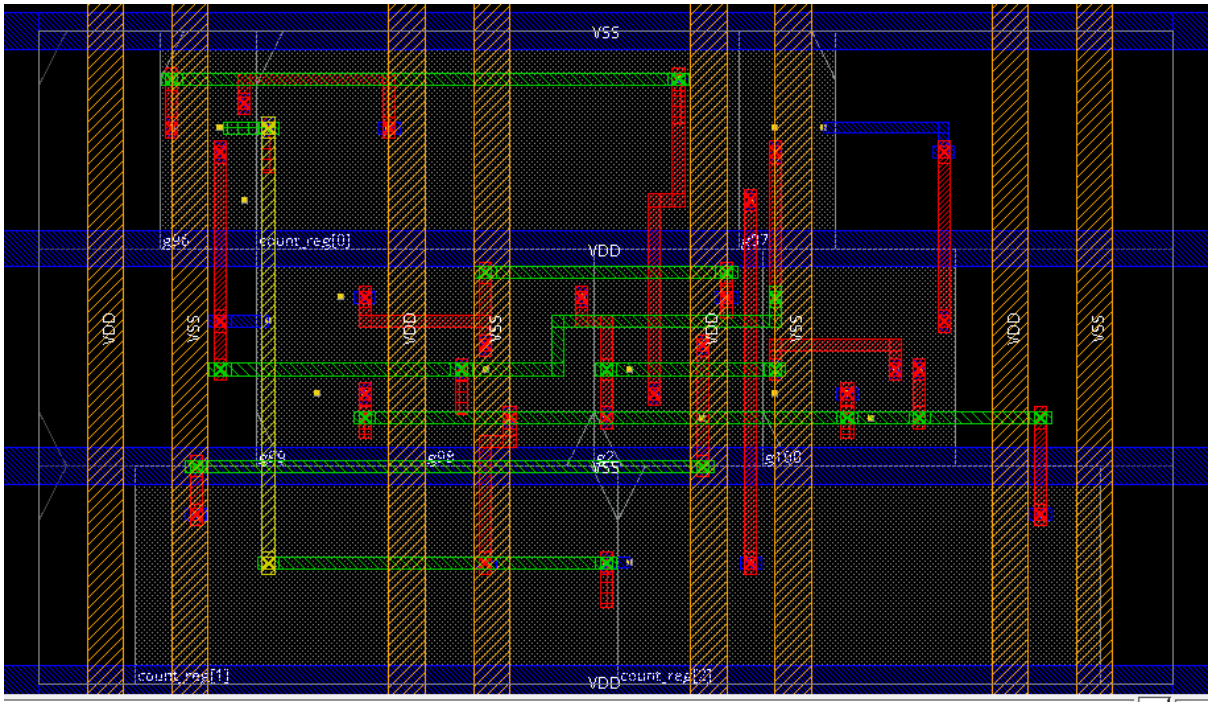
Note: No violating path in Post-CTS timing report of setup time and hold time.

Nano Route





Zoomed view of the core



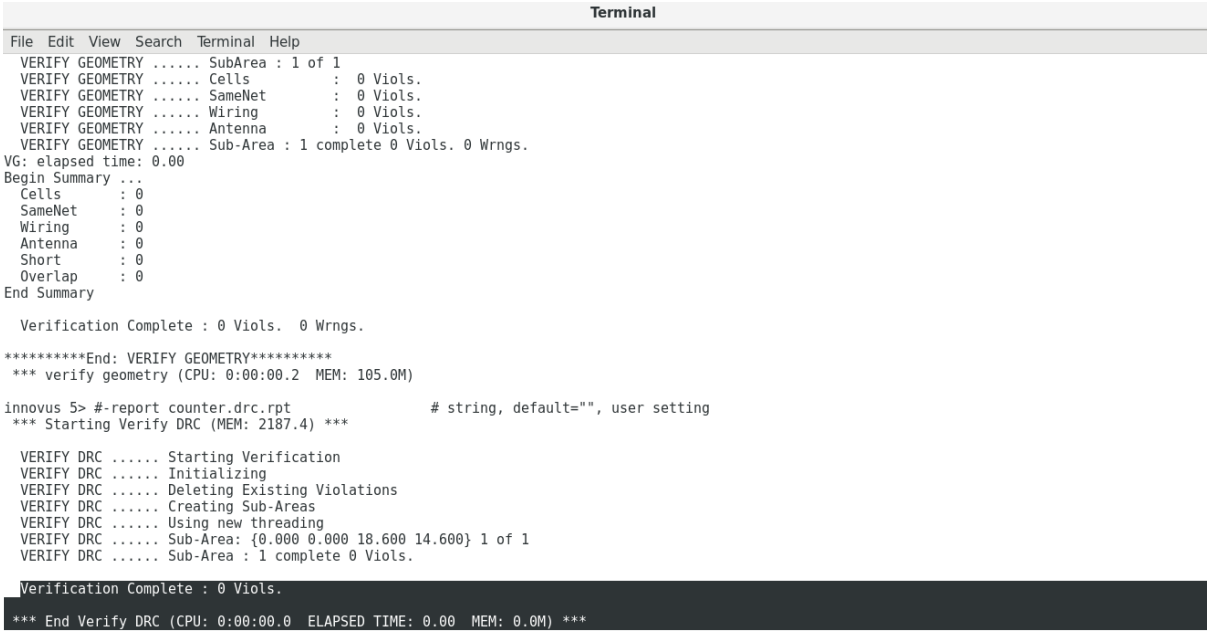
Terminal output after nano routing

```
Terminal
File  Edit  View  Search  Terminal  Help
#
#-----------------------
#  Metal 1           30
#  Metal 2           17
#  Metal 3            2
#-----------------------
#                    49
#
#detailRoute Statistics:
#Cpu time = 00:00:02
#Elapsed time = 00:00:02
#Increased memory = 2.38 (MB)
#Total memory = 1193.67 (MB)
#Peak memory = 1537.38 (MB)
#
#globalDetailRoute statistics:
#Cpu time = 00:00:07
#Elapsed time = 00:00:07
#Increased memory = 5.71 (MB)
#Total memory = 1193.19 (MB)
#Peak memory = 1537.38 (MB)
#Number of warnings = 7
#Total number of warnings = 55
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Sat Oct 16 23:37:28 2021
#
#routeDesign: cpu time = 00:00:07, elapsed time = 00:00:07, memory = 1193.19 (MB), peak = 1537.38 (MB)

*** Summary of all messages that are not suppressed in this session:
Severity  ID               Count  Summary
WARNING   IMPEXT-3493          1  The design extraction status has been re...
WARNING   IMPEXT-3530          1  The process node is not set. Use the com...
WARNING   TCLCMD-1403          1  '%s'
*** Message Summary: 3 warning(s), 0 error(s)

innovus 5>
```

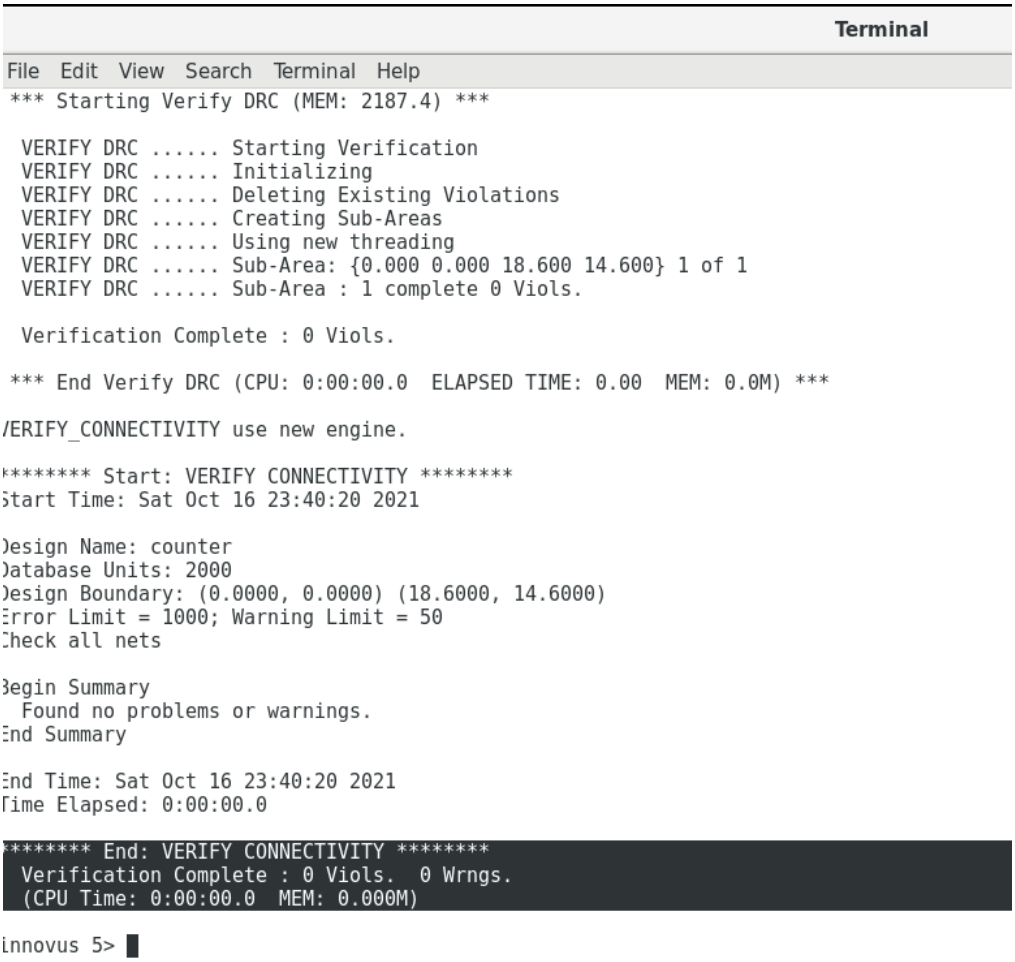
Verify Geometry

```
Terminal
File  Edit  View  Search  Terminal  Help
Severity  ID               Count  Summary
WARNING   IMPEXT-3493          1  The design extraction status has been re...
WARNING   IMPEXT-3530          1  The process node is not set. Use the com...
WARNING   TCLCMD-1403          1  '%s'
*** Message Summary: 3 warning(s), 0 error(s)

innovus 5>  *** Starting Verify Geometry (MEM: 2082.4) ***

**WARN: (IMPVFG-257):   verifyGeometry command is replaced by verify_drc command. It still works in this release but will be removed in future releas
e. Please update your script to use the new command.
  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                        ..... bin size: 2880
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:00.2  MEM: 105.0M)

innovus 5>
```

Verify DRC

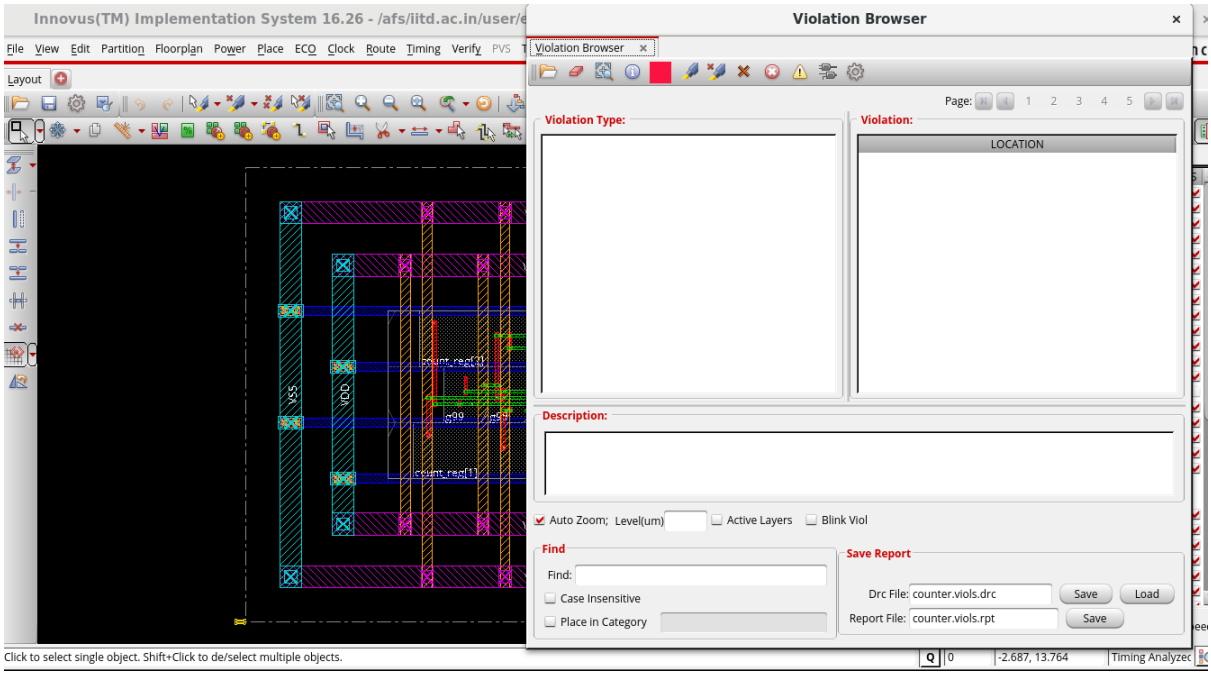


Verify Connectivity

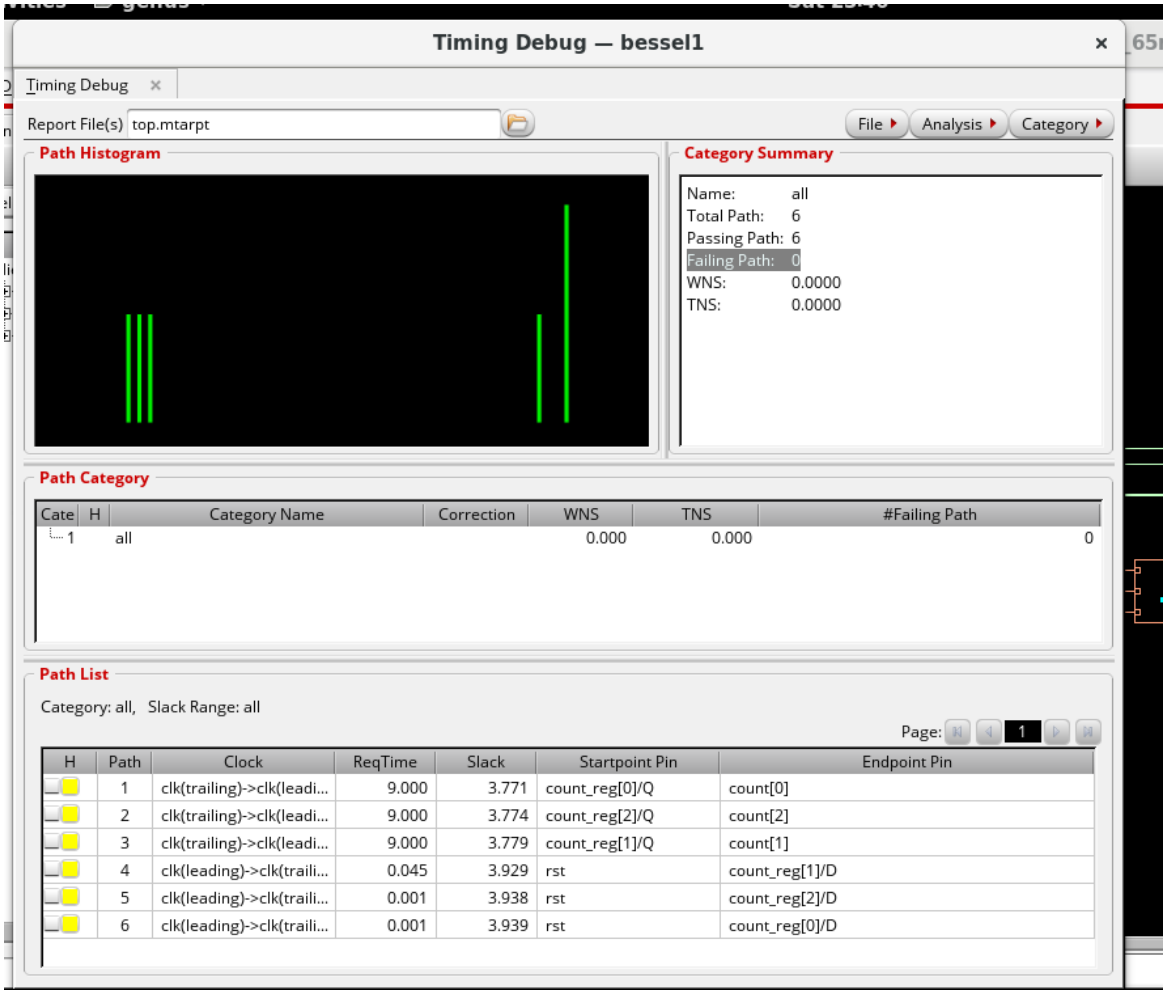


Note: No violations or errors in Geometry, DRC, and Connectivity

Violation Brower



Timing Debug



Note: All the paths are passing.

Targets Achieved

- RTL to GDSII flow of mod 5 counter has been done without any timing violations
- Detailed timing report files are located in counter -> physical_design -> timingReports folder
- Power analysis output is shown in this report