# EXPERIMENT NO. 1

# COMMON EMITTER AMPLIFIER

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**Aim:** To study the performance of a common emitter amplifier.

**Equipment & Components**: Analog Electronics Trainer kit, DSO, Function Generator, (Analog Discovery kit), Digital multimeter, Transistor, Resistors, Capacitors, Connecting wires.

## Theory:

CE Amplifier circuit with potential divider biasing arrangement is shown in Fig. 1.1. Here $C_C$ is called the coupling capacitor and $C_E$ the bypass capacitor.

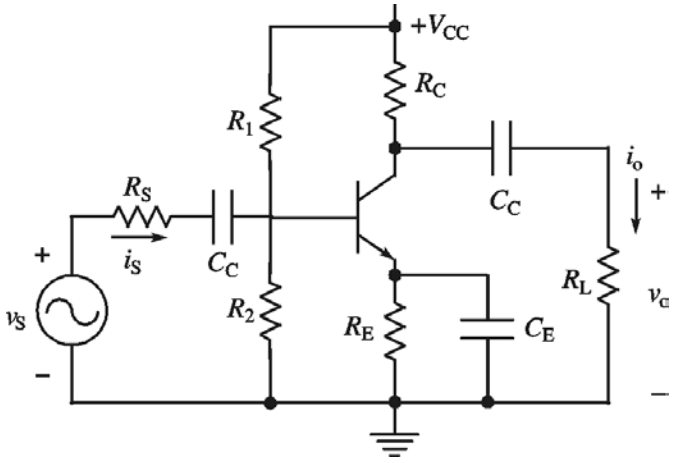



**Figure 1.1: CE Amplifier**

The dc-biasing is used to fix the Q-point of the transistor. Using the equivalent circuit as shown in Fig. 1.2, the Q-point ($I_{CEQ}$, $V_{CEQ}$) of the transistor can be obtained.

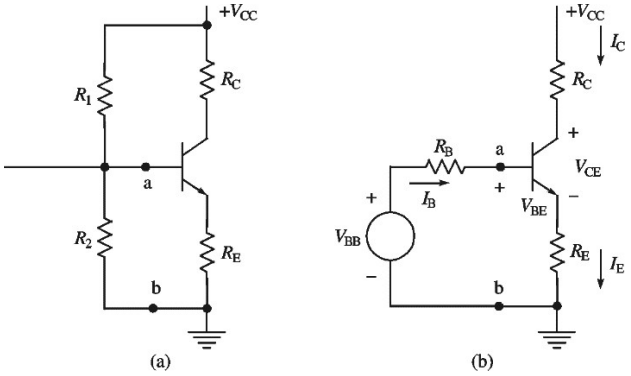



**Figure 1.2 (a) Voltage divider bias for CE Amplifier (b) Thevenin Equivalent circuit**

Thevenin voltage is given by, $V_{Th} = \frac{R_2}{R_1+R_2} V_{CC} = V_{BB}$ and Thevenin resistance is given by, $R_{TH} = \frac{R_1 R_2}{R_1+R_2} = R_B$

At the Q-point, $I_{BQ} = \frac{V_{BB}-V_{BE}}{R_B+(1+\beta)R_E}$ and $I_{CQ} = \beta I_{BQ}$ ; $V_{CEQ} = V_c - I_C R_C - (I_B + I_C) R_E$

For the ac analysis, use the equivalent circuit as shown in Fig.1.3 assuming all capacitors as short at the given signal frequency. The $r_\pi$ - $g_m$ model of BJT is used in the ac analysis.

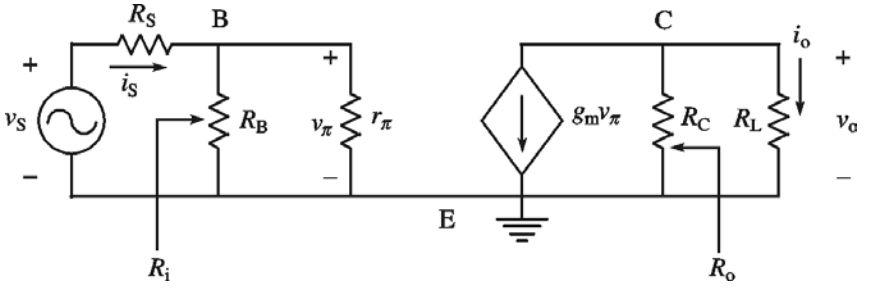



**Figure 1.3 Small signal ac equivalent for CE Amplifier**

$r_\pi$ = Base-Emitter resistance = $V_T / I_B$, where $V_T = KT/q \equiv 26$ mV at room temperature and $I_B$ is the dc Q-point base current.

$g_m$ = Transconductance = $I_C/V_T$, where $I_C$ is the dc Q-point collector current.

β= Short-circuit current gain= $r_\pi g_m$

$v_\pi = v_{be}$ = ac base – emitter voltage

$r_o$= Output resistance =$[\partial v_c / \partial i_c]\, v_{be=\text{ constant}}$ and $V_{BE} = 0.6\,V$

## Voltage Gain, $A_{vs}$ :

The output voltage $v_o = -g_m v_\pi (R_C \parallel R_L)$ where $v_\pi = \frac{R_B \parallel r_\pi}{R_S+(R_B \parallel r_\pi)} v_s$

Hence, the voltage gain is,

$$A_{vs} = \frac{v_o}{v_s} = -\frac{v_\pi}{v_s} g_m (R_C \parallel R_L) = -g_m (R_C \parallel R_L) \frac{R_B \parallel r_\pi}{R_S + R_B \parallel r_\pi}$$

The voltage gain is negative indicating $180^0$ phase reversal between the input and output voltages.

## Current Gain, $A_{is}$:

Since, $i_s = \frac{v_s}{R_S+(R_B \parallel r_\pi)}$ and $i_o = \frac{v_o}{R_L}$, current gain $A_{is} = \frac{i_o}{i_s} = A_{vs} \frac{R_S+(R_B \parallel r_\pi)}{R_L}$

## Input Resistance, $R_i$:

The input resistance is given by $R_i = R_B \parallel r_\pi$, where, $R_B = R_{TH} = \frac{R_1 R_2}{R_1+R_2}$

## Output Resistance, $R_o$:

To find the output resistance, we short circuit the input voltage source and remove the load, $R_L$. Now, we connect an external voltage source at the output terminals and find the current delivered by this source. The ratio of the external voltage and the current drawn by the amplifier gives the output resistance .Thus, $R_o = R_c$

**Frequency Response**:

Due to the presence of coupling and bypass capacitors, at low frequencies, the gain of the amplifier is reduced. The internal transistor capacitors lower the voltage gain and input impedance at high frequencies. At high frequencies the coupling, bypass and transistor parasitic capacitors provide very low impedance. The low impedance due to parasitic capacitors reduces the gain at high frequencies. Thus, the gain of the amplifier reduces both at low and high frequencies. The low frequency 3 dB cutoff occurs due to the bypass capacitor $C_E$ (sufficiently large), and is given by

$$f_L = \frac{1}{2\pi R C_E} \qquad \text{where,} \quad R = R_E \parallel \frac{r_\pi}{\beta+1}$$

The high frequency modeling is carried out using hybrid-π model as shown in Fig. 1.4.

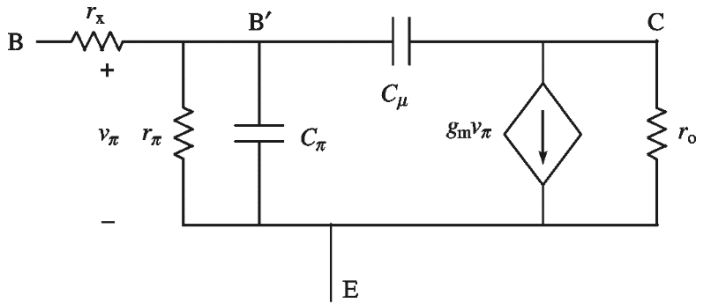



**Figure 1.4: High frequency hybrid- π model of BJT**

For high frequency -3 dB cutoff of the amplifier is given by,

$$f_H = \frac{1}{2\pi RC} \quad \text{where,} \quad C = C_\pi + A_v \times C_\mu \quad \text{and} \quad R = r_\pi \parallel (R_s \parallel R_B),$$

$C_\pi = base - emitter$ Capacitance obtained from data sheet or can be calculated from the relation, $C_\pi = \frac{g_m}{2\pi f_T}$, where $f_T$ is unity common–emitter short–circuit current gain frequency.

$C_\mu$ = Collector – base junction capacitance obtained from data sheet

$|A_v| = g_m \times R_{ac}$ , where $R_{ac}$ = the net ac load. The Bandwidth of the Amplifier, BW = ( $f_{H-} f_L$ ).

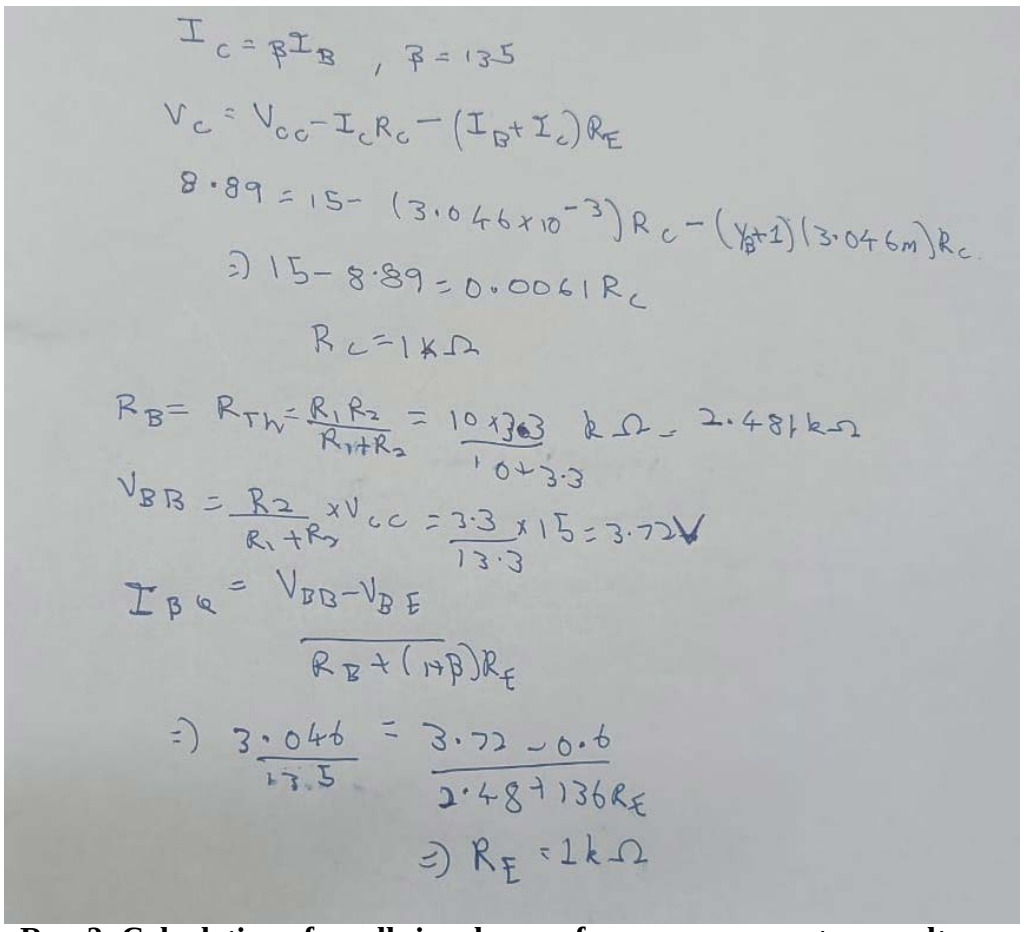
## Observations:

### Run1: Design

Determine the values of $R_E$ and $R_C$ of the CE amplifier circuit shown in Fig.1.1, using the following data.

$R_1$=10 KΩ, $R_2$= 3.3 KΩ, $R_L$= ∞ (open), $R_S$ =1 KΩ, $V_{CC}$ =15V, $I_{CQ}$ = 3.046 mA, $V_{CEQ}$ = 8.89 V, $V_{BE}$=0.6 V and

**β=135 (measure using DMM)**. Neglect $I_{CBO}$. Use the Transistor 2N2222, $C_{C1}$=$C_{C2}$=10μF, $C_E$=100μF.




**Run 2: Calculation of small signal ac performance parameters : voltage gain, current gain :**

Feed the 50mv (p-p) sinusoidal signal at 1 KHz frequency as the input signal $v_s$, and measure the output voltage $v_o$, and the voltage between base and the common terminal,$v_b$.The source current $i_s$ is then given by $(v_s - v_b)/ R_s$.

**Voltage gain**, $A_{vs} = \frac{v_o}{v_s}$ .

**Current gain**, $A_{is} = \frac{i_o}{i_s}$, where $i_o = \frac{v_b}{R_L}$ ; & $R_L$=1KΩ

**Tabular Column for $A_{vs}$ & $A_{is}$ :**

| S. No. | $V_{s(p-p)}$ (mV) | $V_{o(p-p)}$(V) | $i_o$ ( mA) | $V_{b(p-p)}$(mV) | $i_s$ ( mA) | $A_{vs}$ | $A_{is}$ |
|---|---|---|---|---|---|---|---|
| 1 | 50 | 1.372 | 1.372 | 26.23 | 0.0236 | 27.44 | 58.135 |
| 2 | 60 | 1.630 | 1.630 | 31.62 | 0.0282 | 27.16 | 57.801 |
| 3 | 70 | 1.87 | 1.87 | 37.08 | 0.0327 | 2671 | 57.18 |
| 4 | 80 | 2.12 | 2.12 | 42.6 | 0.0373 | 26.5 | 56.836 |
| 5 | 100 | 2.57 | 2.57 | 53.79 | 0.0461 | 25.7 | 55.74 |

Theoretical value: Practical value:

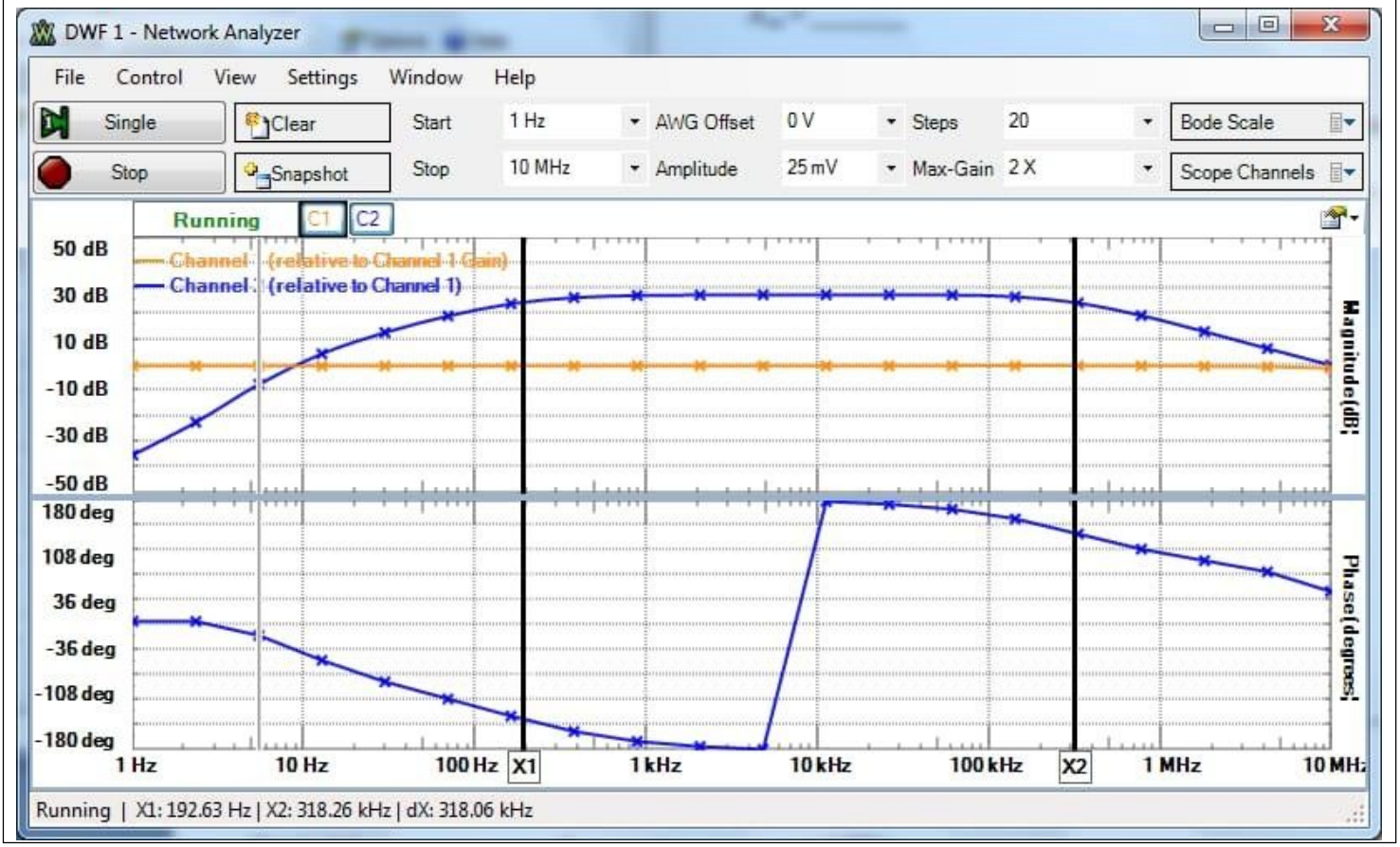
$A_{vs}$ = 25.75 $A_{vs}$ = 26.702

**Run3: Frequency response of CE amplifier using potential divider biasing.**

Feed sinusoidal input of amplitude $V_{s(p-p)}$= 50 mV. Sweep the input frequency from 1 Hz to 1 MHz and obtain the

magnitude and phase response of the filter. The voltage gain of the CE amplifier practically =27.5dB .

**Frequency response**




Theoretical: $f_L$ =198.36Hz , $f_H$= 314.26Khz , and BW= 314.07Khz

Practical: $f_L$ =192.63 HZ , $f_H$ = 318.26Khz , and BW=318.06KHz

## Run 4 : Calculation of small signal input and output resistance:

**Input resistance**, $R_i = \frac{v_b}{i_s}$, Theoretical $R_i$ =0.788k ohm and Practical $R_i$ =1.113k ohm

**Output resistance**, $R_o$ : To measure the output resistance $R_o$, short the input terminals , i.e. remove the input ac source, connect an ac source through a resistor across the output terminals as shown in Fig. 1.5. Choose $v_s'$ equal to 500 mVp-p at 1 kHz frequency and $R'$= 1 kΩ. Measure $v_o'$. The output resistance is then given by the following equation.

$$R_o = \frac{v_o'}{(v_s' - v_o')/R'}$$

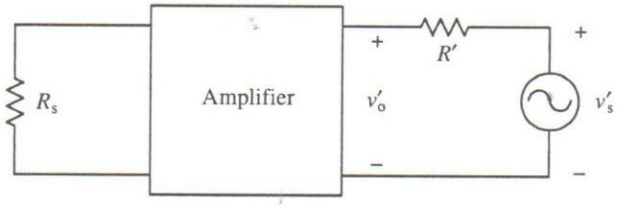


**Figure1.5: Setup for the measurement of output resistance.**

Theoretical $R_0$ = 1000ohm and Practical $R_0$ = 971.14ohm

Observe the input and output voltages simultaneously on a DSO, The phase difference ($\phi$) between the two voltages is 180 degrees.

## Conclusions:

In this lab experiment the performance of a CE Amplifier circuit was studied using the potential divider method. In run 1 I found the values of Re and Rc. After that using a small signal analysis, the values of voltage gains and current gains were found. There was a small deviation between the theoretical and practical values. Then in run3, the frequency response of the amplifier and found the bandwidth was observed. In the last run the input and output resistances were found.