**CMOS VLSI CIRCUITS**

OPEN ENDED PROJECT

**TEAM DETAILS**

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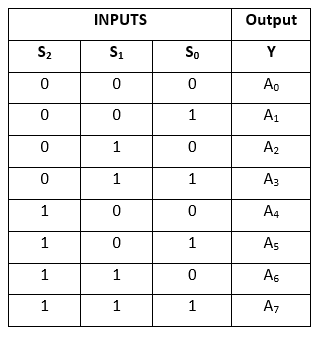
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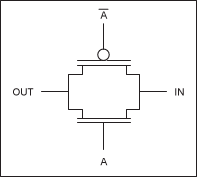
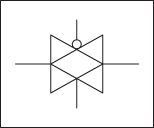
DR. SAROJA V SIDDAMAL

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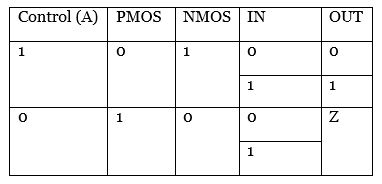
8:1 MUX Using Transmission Gate Logic

Truth Table for 8:1 MUX

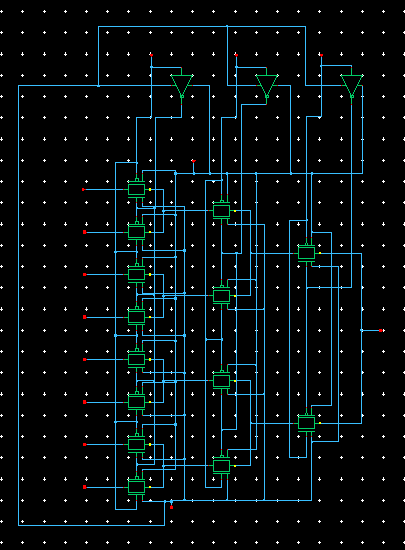


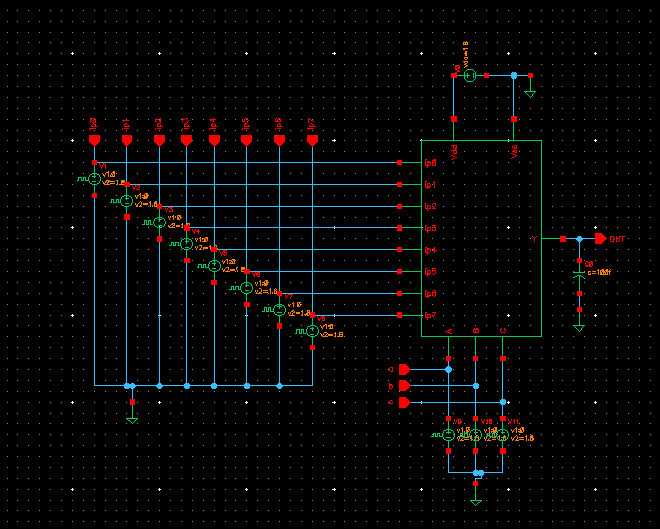
 

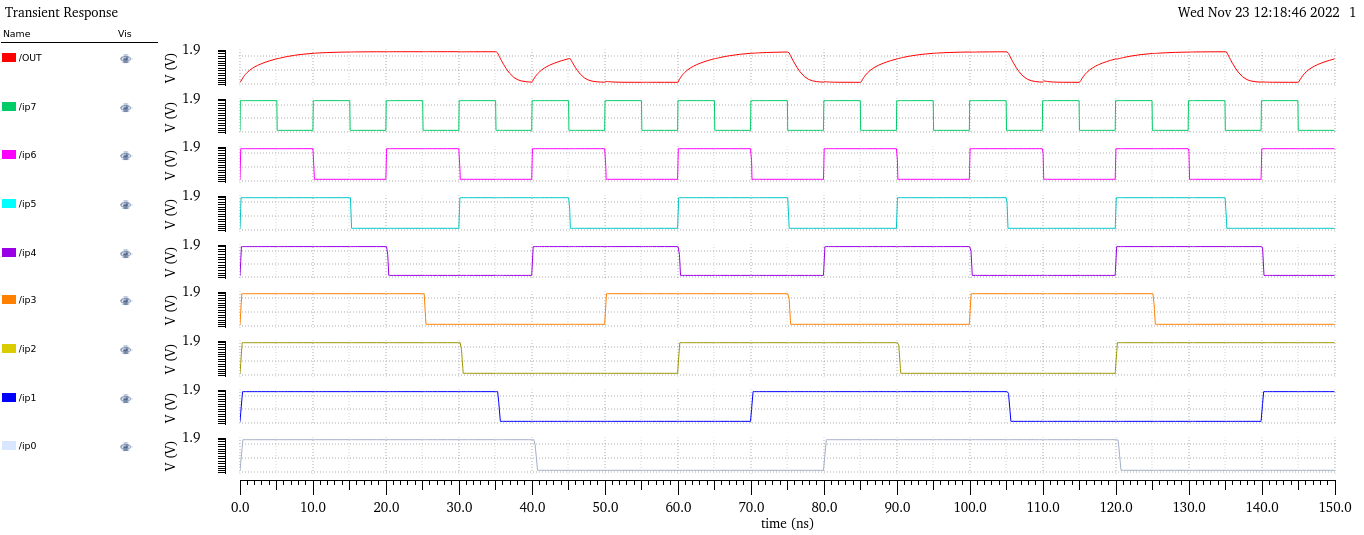
Schematic and Circuit Symbol of Transmission Gate



Logic of Transmission Gate



8:1 MUX Using Transmission Gate Test Circuit :



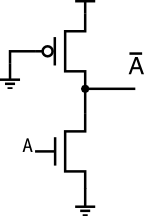
Analysis and Observations:

**For 8:1 MUX using Transmission Gate**

|  |  |
| --- | --- |
| Rise Time (tr) | 7.81 ns |
| Fall Time (tf) | 2.534 ns |
| Delay Time(td) | 1.792 ns |
| Power | 1.117 W |

Pseudo NMOS Logic:

In a Pseudo NMOS Logic,the gate of PMOS(Pull Up Transistor) is always connected to Ground potential,Hence the PMOS is always ON.The Below N-Tree gets evaluated corresponding to the inputs provided in the N-Tree.



A Pseudo Inverter

Equation for 8:1 MUX

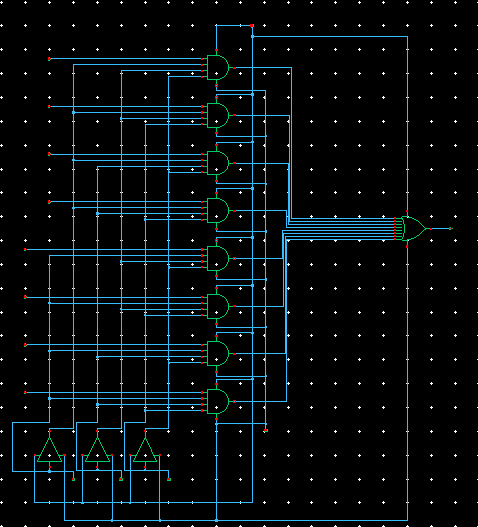
Y = A'.B'.C'.I0 + A’.B'.C.I1 + A'.B.C'.I2 + A’.B.C.I3 + A.B’.C’ I4 + A.B’.C I5 + A.B.C’ .I6 + A.B.S3.I7

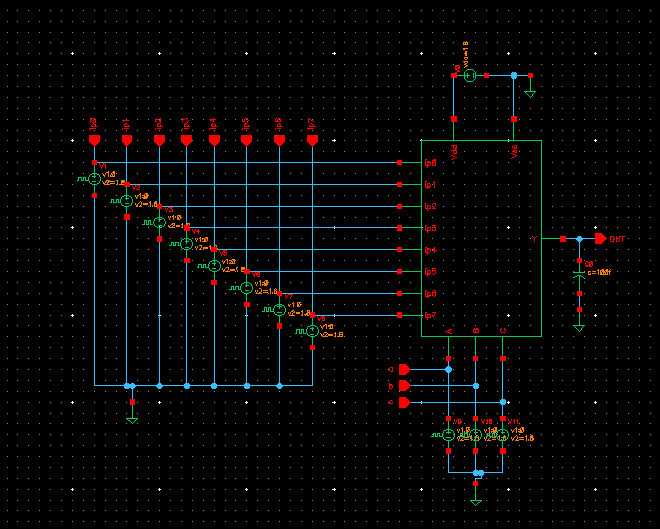
Here we need

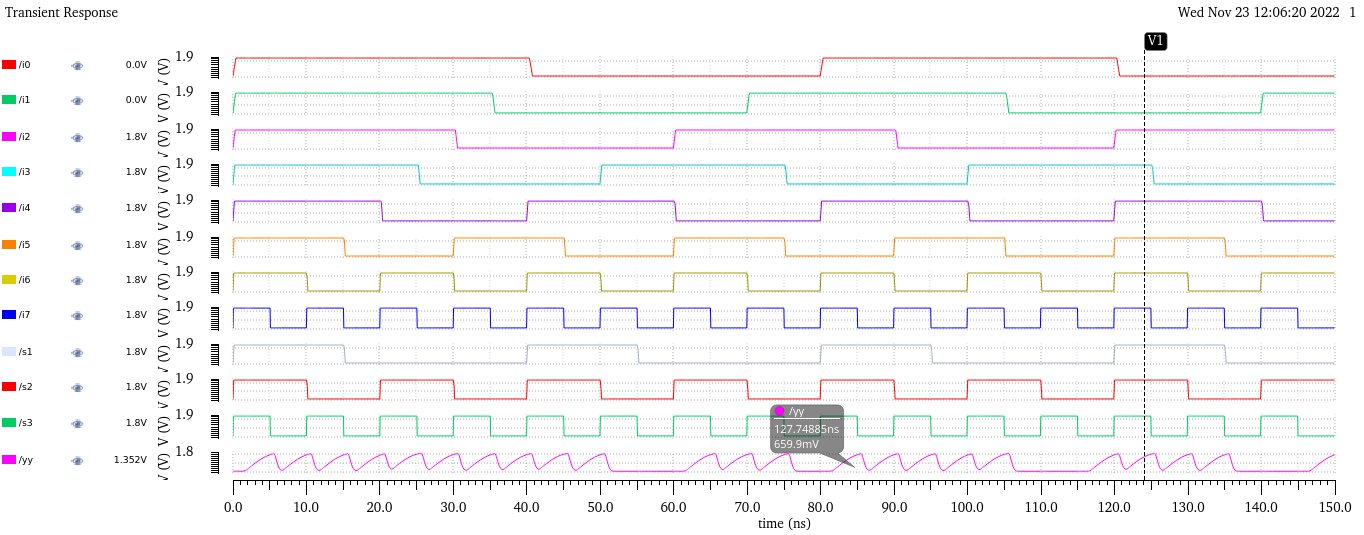
->8 no.s of 4-input AND gate designed with the Pseudo NMOS Logic.

->1 no.s of 8-input OR gate designed with the Pseudo NMOS Logic.

->Inverters as required.



8:1 MUX Using Pseudo NMOS Logic Test Circuit :



Analysis and Observations:

**For 8:1 MUX using Pseudo NMOS**

|  |  |
| --- | --- |
| Rise Time (tr) | 3.561 ns |
| Fall Time (tf) | 935.1ps |
| Delay Time(td) | 3.027 ns |
| Power | 749.5 mW |

RESULTS AND CONCLUSIONS:

|  |  |  |  |
| --- | --- | --- | --- |
|  | Pseudo NMOS Logic | Transmission Gate Logic | Comparisons |
| Rise Time(tr) | 3.561 ns | 7.81 ns | P.N |
| Fall Time(tf) | 935.1 ps | 2.534 ns | P.N |
| Delay Time(td) | 3.027 ns | 1.792 ns | T.G |
| Power | 749.5 mW | 1.117 W | P.N |

As observed from the analysis done for both the logic families for the circuit of 8 : 1 MUX,we observe that rise time of the Pseudo NMOS logic used is less compared to Transmission Gate Logic,Also Fall time for the Pseudo NMOS logic used is less compared to Transmission Gate Logic.Power for Pseudo NMOS logic is also less when compared to the Transmission Gate logic.

Hence Pseudo NMOS Logic used for 8:1 MUX is much faster and reliable as

the rise time and fall time is less,also Power consumed is less.