

Recognition of digital logic circuit diagrams

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PROPOSAL

When designing digital logic circuits, it is frequently necessary to draw the circuits by hand before implementing the design in RTL. If there are some issues faced during simulation or synthesis of the design, the design process has to be repeated. To speed up the design cycle, it would be beneficial to have an environment that can capture hand-drawn digital circuit diagrams and generate the RTL code for the logic. The Verilog RTL code generated by the environment can be used directly in simulation and synthesis environments.

After review of existing research in the subject, there were papers found in the topic of recognizing transistor-level circuit diagrams. This project aims to focus on the area of digital logic circuit diagrams (involving AND gates, OR gates, flip-flops, etc.) and deliver a solution that is different from existing research work.

The project would use morphological image processing techniques to detect the wire connections and the logic gate types in the drawing. The signal names in the diagram would be identified as well and used in the RTL code. The auto-generated RTL code would be compared with manual creation of RTL code to verify the accuracy of the project environment.

Future enhancements of the project would include creating timing diagrams of the circuit so that it can serve as an initial check of the circuit design.

REFERENCES

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- [3] S. Zesheng, "Symbol recognition in electronic diagrams using decision tree," Proceedings of the IEEE International Conference on Industrial Technology, pp. 719-723, 1994.
- [4] B. Edwards, "Machine recognition of hand-drawn circuit diagrams," IEEE International Conference on Acoustics, Speech, and Signal Processing, vol. 6, pp. 3618-3621, 2000.

PHONE USE

A personal Android phone will be used for testing the project.