Comparision between Vedic and Array multipliers

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Comparison of Vedic Multiplier with Conventional Array Multiplier

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***Abstract*—In the current developing world, demand for high speed multipliers has increased. To satisfy the need of fast multipliers we have to use high Throughput Arithmetic operations. One of the most important Arithmetic operations is Multiplication. In general, we define the performance of any DSP system based on the performance of a multiplier, as in general multiplier is slow. So the speed and area of multiplier became very important in real time applications. while designing a fast multiplier it consumed large area, so designing a multiplier which is efficient in both speed and area became a big challenge. So in designing a system in Verilog approach low power multipliers are required to make our system more efficient. Our Report mainly deals with the comparison of both conventional array multiplier and a Vedic multiplier. Here, we compare our design mainly on area, number of LUT's used, delay, memory and hardware complexity**

***Index Terms*— Array Multiplier, Vedic Multiplier, Multipliers Urdhva Tiryagbhayam.**

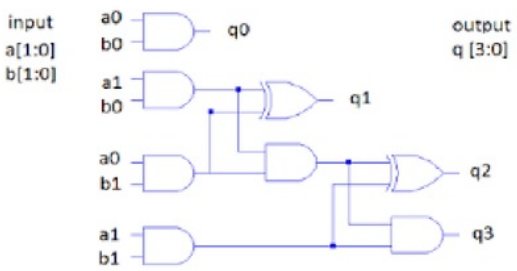
I. Introduction

In many DSP systems performing Arithmetic operations is a basic operation performed, in the Arithmetic Operations like Multiplication plays a major part. In designing ALU's the major requirement is an effective multiplication algorithm. In Fast Fourier transform and convolution also the basic block is multiplication, so as the execution time is our first priority, fast multipliers are required. For the fabrication of many complex circuits fast and efficient multiplier is really an important thing as a designer. One of the basic algorithm used is Array multiplication algorithm, this algorithm is associated with high hardware complexity. So a fast multiplication process is developed by Vedic mathematics. This multiplication uses Urdhva Tiryagbhayam sutra. In the rest of the report we will be dealing with Vedic multiplier, Array multiplier, comparison and finally with a conclusion.

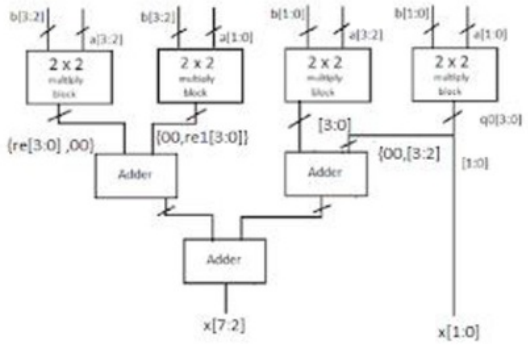
II. Vedic Multiplier

This algorithm is mainly basically on vertical and crosswise multiplication. The following circuit & block diagrams depict the process of Vedic multiplication.

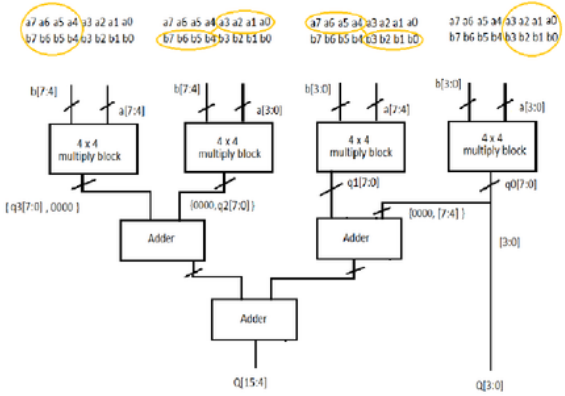
A. 2x2 bit Vedic Multiplier:



B. 4X4 Multiplier Block:

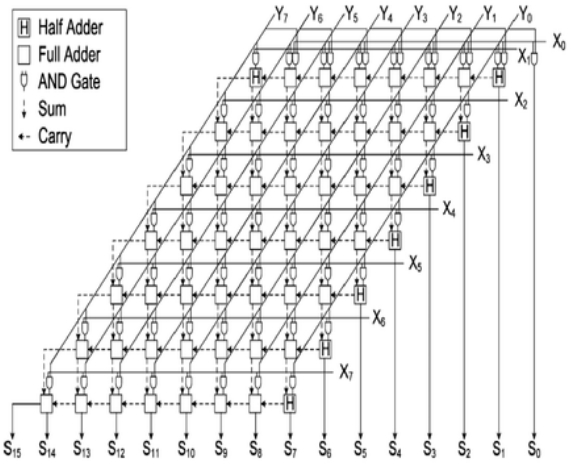


C. 8X8 Multiplier Block



III. ARRAY MULTIPLICATION:

Array multiplier is a layout of a combinational logic. It utilizes short wires that run from one full adder to the next full adder horizontally, vertically or diagonally. The following diagram depicts the process of array multiplication. The array multiplier is one of the basic multipliers and hence is highly inefficient.



The conventional array multiplier utilizes carry save addition to add the products. In this method, we first generate the product terms through AND gates. The first row can comprise either HA's or FA's (i.e. half adders or full adders respectively), If we use FA's in the first row then the cin to the block must be zero. Then the carry generated in each FA is transferred to the forward progressing diagonal block in the next row. Since we add carries in the next stage it is carry save method of addition. Continuing this process, we get the sum of all the product terms. The output of the final row is the required product of the two operands.

IV. COMPARISONS OF BOTH MULTIPLIERS:

Parameters	Array multiplier	Vedic multiplier
Area	more	less
Hardware Complexity	High	low
Memory	more	less
Delay	more	less
No of LUT's	more	less
Power consumption	High	low

V. CONCLUSION

As we see from the above comparisons we found that Vedic Multiplier consumes less area, memory than conventional array multiplier. In terms of Hardware complexity also Array Multiplier is more complex with respect to hardware due to many full and half adders. Hence Vedic Multiplier is better than Array Multiplier.

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