PCI Express - MSI Interrupt Reception using the AXI Bridge

Contents

Chapter 1. PCI Express Overview

- Peripheral Component Interconnect (PCI) is a connection interface standard.
- The PCI Express is an upgrade over the previous PCI, where it offers more bandwidth and is compatible with existing operating systems.
- Unlike the PCI's parallel connection, the PCI handles several point-to-point serial connections with a switch (like a network).

Chapter 2. Interrupts Overview

- Interrupts are a method of creating a break in the flow of function.
- The PCI Express feature three main methods of interrupt handling: Legacy Interrupt, Message Signaled Interrupts (MSI), and MSI-X.

Chapter 3. AXI Bridge Overview

- The AXI Bridge Module acts as a bridge between the standard AXI interfaces and the Synopsys DesignWare PCIe core native interfaces.
- The bridge interconnects the AXI interfaces within an AMBA-embedded system with a remote PCIe link, as either a root complex port, or as an endpoint port.

Chapter 4. MSI Reception when using the AXI Bridge

The MSI are memory write (MWr) TLPs. The core automatically builds the MSI packet whenever requested by your application logic and a simple handshake is all that is required. The AXI bridge receives MSI requests in the same manner as a MWr. The termination of an MSI request must be done by your application or by using the optional MSI controller.

AXI MSI Controller (RC Mode):

1. The bridge provides an optional MSI controller to detect and terminate incoming MSI requests by enabling the `CX_MSI_CTRL_ENABLE =1`
2. The MSI packets are captured and terminated in the AXI bridge, and an interrupt is signaled locally.
3. The MSI Controller is programmed with the similar system MSI address.
4. The MSI interrupt is detected when the received MWr request matches specified MSI address, along with the MSI memory write request conditions.
5. The MSI Controller that decodes the MSI MWr data payload that determines the Endpoint device (EP) and the interrupt vector corresponding to the MSI.
6. `msi_ctrl_int output`is asserted when as valid interrupt is decoded.
7. De-assertion takes place when there is no MSI interrupt pending.

Chapter 5. Features

- MSI interrupt controller is only enabled in RC mode when device type is 0x4. It is inactive in EP mode.
- Up to eight EPs are supported by the MSI interrupt controller.
- Each supported EP has a set of interrupt enable, mask, and status registers.
- Guarantees correct AXI ordering with respect to other inbound posted writes by generating the MSI interrupt only after your application AXI slave acknowledges responses of previous posted TLPs.
- A maximum of 32 interrupts are supported per EP.
- Optional 32-bit register driven general purpose outputs `(msi_ctrl_io[31:0])`

Chapter 6. MSI Request Detection Criteria:

- Header attributes bits are zero. No snoop (NS) and relaxed ordering (RO) must be zero.
- Length field is 0x01 to indicate a payload of one DWORD.
- First byte enable (FBE) is 4'bxx11 (enabling the first two bytes of the payload.)
- Last byte enable (LBE) is 4'b0000.
- TLP address corresponds to system's chosen MSI address as programmed in the "MSI Controller Address Register" `(MSI_CTRL_ADDR_REG and MSI_CTRL_UPPER_ADDR_REG)`. This register is not the "MSI Lower 32 Bits Address Register" which is part of the PCI Express MSI capability register structure.

Chapter 7. DM Core Block Diagram (with AHB/AXI Bridge Module)