Logic Gates using CMOS Technology

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***Abstract*—To study the design and functionality of NAND and AND gate that includes how Tphl and Tplh is affected in various cases of input.**

I. Introduction

- NAND and NOR gates are basic building block of digital circuits because any type of circuit can be made from these two that's why are called as Universal Gates.
- The Pull Down Network is constructed using NMOS transistor, while PMOS transistors are used in the Pull Up Network. The primary reason for this choice is that NMOS transistors produce "strong zeros," and PMOS devices generate "strong ones".
- Their are certain Rules that can be derived to construct logic functions.NMOS devices connected in series Results to an AND function becuase When all the inputs high,all the series combination conducts and the value at one end of the chain is transferred to the other end. Similarly, NMOS transistors connected in parallel result in OR function because if the conducting path between the output and input terminal is at least one then the value at one end will be transferred to other end. Using similar concepts, Rules for PMOS networks can be derived. A series connection of PMOS conducts if all inputs are low, depicting a NOR gate,Vice Versa PMOS transistors in parallel implement a NAND gate.
- A Complimentary gate is naturally inverting that means we can derive NAND , NOR , XNOR gates directly but for AND , OR , XOR gate we need to connect one extra Inverter.

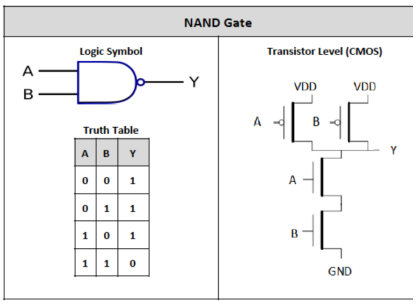

Fig:1-Figure Showing transistor level diagram and truth table of nand gate

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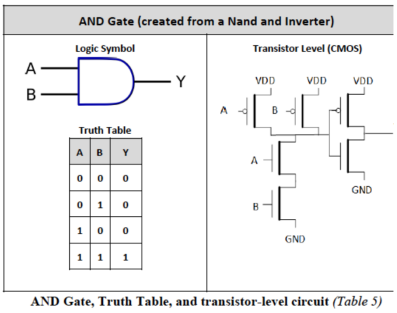


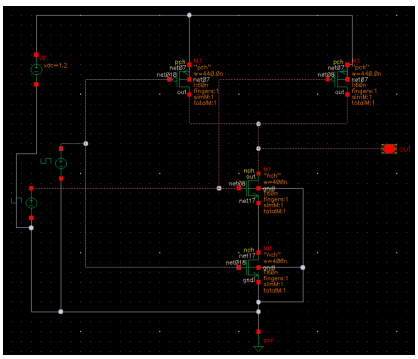
Fig:2-Figure Showing transistor level diagram and truth table of and gate

II. Static Properties of CMOS Gates:

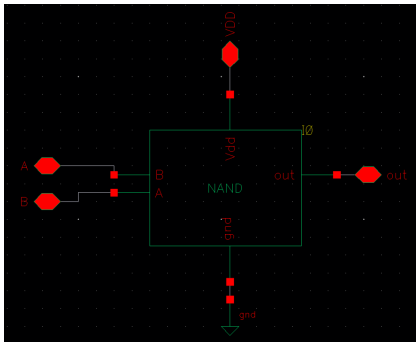
- Similar to cmos inverter the Steady-state power dissipation of CMOS gates is negligible only a little power dissipation due to leakage currents.
  Width of PMOS and NMOS in Combinational gates will be adjusted in such a way that it's propagation delay is same as that of CMOS Inverter (Wp/Wn = 2.3).
  Tplh and Tphl will be different in different Input transitions in combinational gates.

III. Results and Inferences

A. Schematic of NAND Gate drawn:

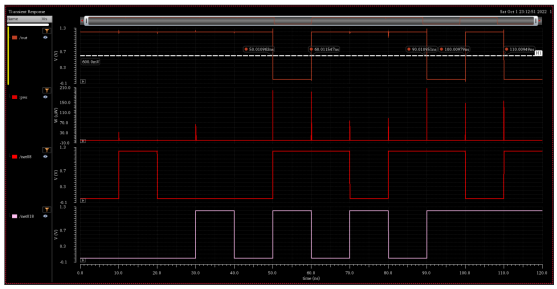


B. Symbolic View of NAND gate drawn:



In the above Schematic of NAND Gate the width of NMOS and PMOS is equals to 440nm and 400nm this is because to obtain similar response as of an inverter.

C. Transient analysis and power analysis of nand gate

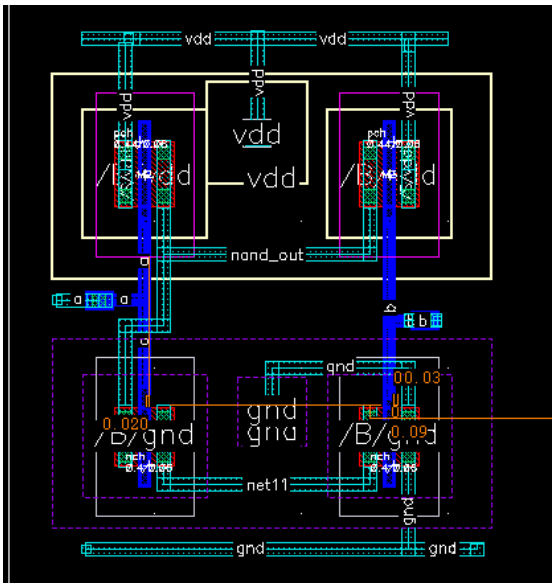


Transient Analysis

Inferences

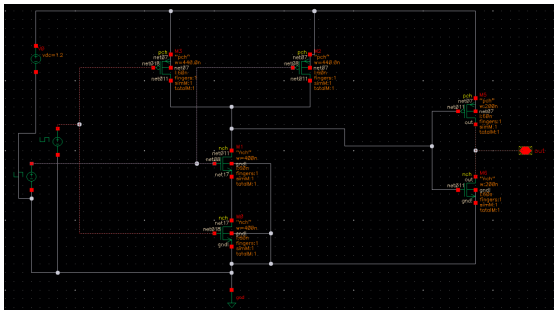
- For case 1:
  Rise Time is 0.011547ns when A=1 and B =1→0
  For case 2 :
  Rise Time is 0.00979ns when A=1 and B=1→0
  For case 3:
  Rise time even lesser than these two.
- Justification For Inference 1 :
  We Know Tplh equals to .69*Rp*Cl so When Both PMOS are than Net resistance is equals to Rp/2 whereas in other two cases it is equal to Rp so the cases 3 will have the lesser delay wrt to other two. The difference between case 23 is depending on which nmos is ON in PDN if the nmos which is closer to out is ON than Vdd has to charge Cl as well as Ca so ultimately we will get a delay wrt to other case.
- Fall time(Tphl) in the above diagram is equals to 0.010963ns(50.010963-20.005)ns for input transition A=B=0 →1 and it is equal to 0.10951ns for A=1 , B=0 →1 and for the last case(B=1 , A=0 →1) it is approximately equal to case 2.
- Justification for inference 3 :- For case we were having a strong pull up network because both PMOS devices are ON initially whereas in other two cases only one PMOS is ON resulting in lesser delay. The little difference between case 2 3 is due to the body effect.
- The Static power consumption for these logic is also approximate to Zero same as an inverter because at a time either Pull Up is ON or Pll Down is ON so there is direct Connection between VDD and GND.
- Dynamic Power consumption is still there that is because for a small duration of time Both PUN and PDN transistors are in saturation region so there is a direct connection between Vdd and Ground.

D. Layout For NAND gate



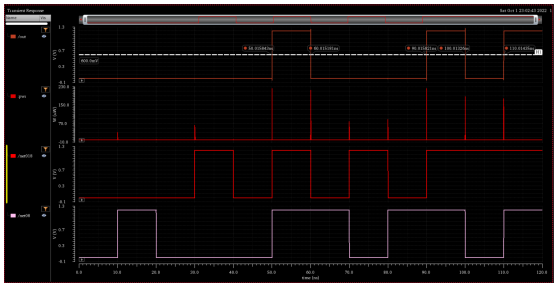
- Area for this gate is approximately equals to 2*(440*60 + 400*60)→100.8 micro meter (Sum of area of all the transistors).
- In layout We need to arrange the transistor parallely in PUN and PDN this is because when we will be using them in larger network than there we are having two straing parallel Wire for VDD and GND So we need to maintain a required height for net layout design as well as we have to keep them in parallel fashion.

1) Schematic for AND gate:



- Just Connected One Inverter in Front of nand gate.

E. Transient analysis for AND gate



- Here in AND gate one extra invetrter is connected in front of NAND so just extra Tplh and Tphl of inverter is being added to NAND gate's delay values and the sequance of all the cases is exaclty same as that of NAND gate.

CONCLUSION

- Tplh and Tphl in cases of NAND and AND gate depends on the type of input transition taking place (tp=0.69*R*Cl). So, for design of these gates the Worst Case Scenario of the respective transition should be considered otherwise Resultant gate may get into Meta stable state.
- For Tplh Worst case scenario is A=1, B=1$\rightarrow$0 (here A is input to the upper transistor and B is input to lower transistor in PDN) because in this case net resistance in PUN is Rp only and since upper transistor in PDN is ON so we need to charge its internal capacitance.
  And the best Case for Tplh is A = B = 1 $\rightarrow$ 0.
- For Tphl the worst case scenario is A = B = 0 $\rightarrow$ 1 because in this case both transistor are switching ON.
  And the best case for Tphl is A= 1, B = 0 $\rightarrow$ 1.
- For AND Gate analysis will be exactly similar just extra delay for inverter will be added.

IV. REFERENCE

http://www.verilogcode.com/2015/05/draw-digital-logic-gates-truth-tables.html

Jan Rabaey - Digital Integrated Circuits