Logic Gates using CMOS Technology

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***Abstract*—To study the design and functionality of NOR, XOR and XNOR gate that includes transient analysis , power analysis and Layout.**

I. Introduction

- NAND and NOR gates are basic building block of digital circuits because any type of circuit can be made from these two that's why are called as Universal Gates.
- The Pull Down Network is constructed using NMOS transistor, while PMOS transistors are used in the Pull Up Network. The primary reason for this choice is that NMOS transistors produce "strong zeros," and PMOS devices generate "strong ones".
- Their are certain Rules that can be derived to construct logic functions.NMOS devices connected in series Results to an AND function becuase When all the inputs high,all the series combination conducts and the value at one end of the chain is transferred to the other end. Similarly, NMOS transistors connected in parallel result in OR function because if the conducting path between the output and input terminal is at least one then the value at one end will be transferred to other end. Using similar concepts, Rules for PMOS networks can be derived. A series connection of PMOS conducts if all inputs are low, depicting a NOR gate,Vice Versa PMOS transistors in parallel implement a NAND gate.
- A Complimentary gate is naturally inverting that means we can derive NAND , NOR , XNOR gates directly but for AND , OR , XOR gate we need to connect one extra Inverter.

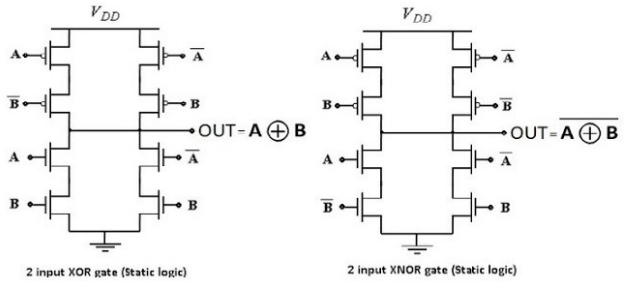

Fig:1-Figure Showing transistor level diagram of XOR and XNOR gate

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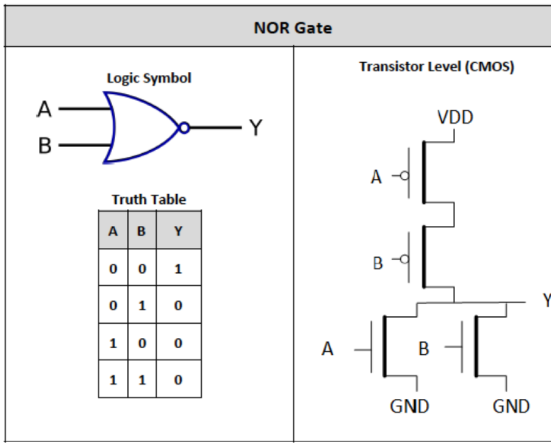


Fig:2-Figure Showing transistor level diagram and truth table of NOR gate

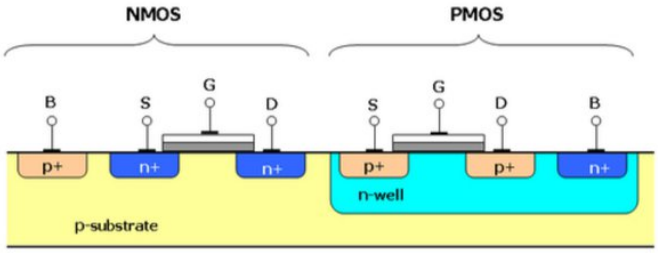


Fig:3 - Design on P type wafer

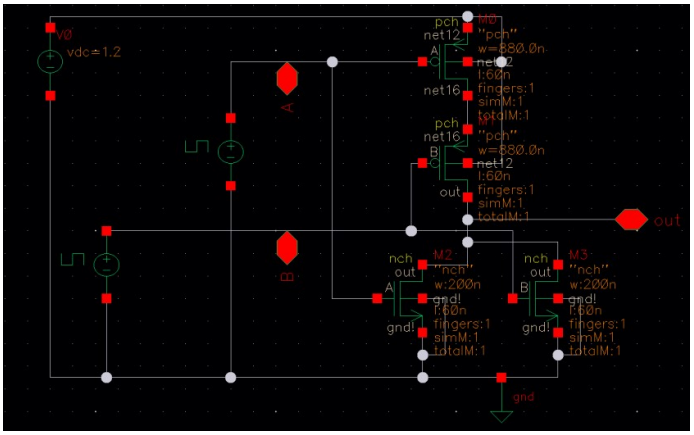
- To design Circuits we can either use a p-type wafer or n-type wafer. So here in this lab we have implemented the designs on P type wafer so to implement the PUN we need to dig N-well inside it. So that both PUN and PDN both can be implemented on a single Silicon Wafer.

II. Static Properties of CMOS Gates:

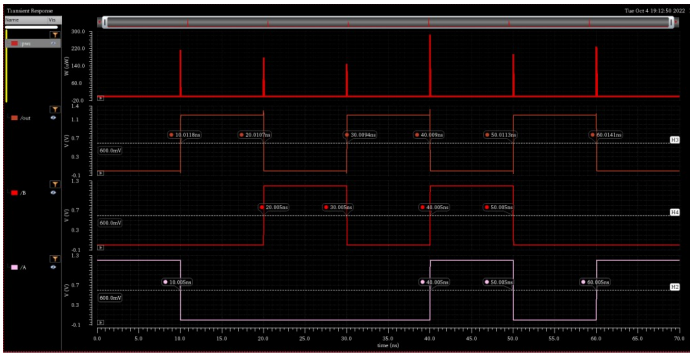
- Similar to cmos inverter the Steady-state power dissipation of CMOS gates is negligible only a little power dissipation due to leakage currents.
  Width of PMOS and NMOS in Combinational gates will be adjusted in such a way that it's propagation delay is same as that of CMOS Inverter (Wp/Wn = 2.3). Tplh and Tphl will be different in different Input transitions in combinational gates.

III. Results and Inferences

A. Schematic of NOR Gate:



B. Transient analysis and power analysis of NOR gate

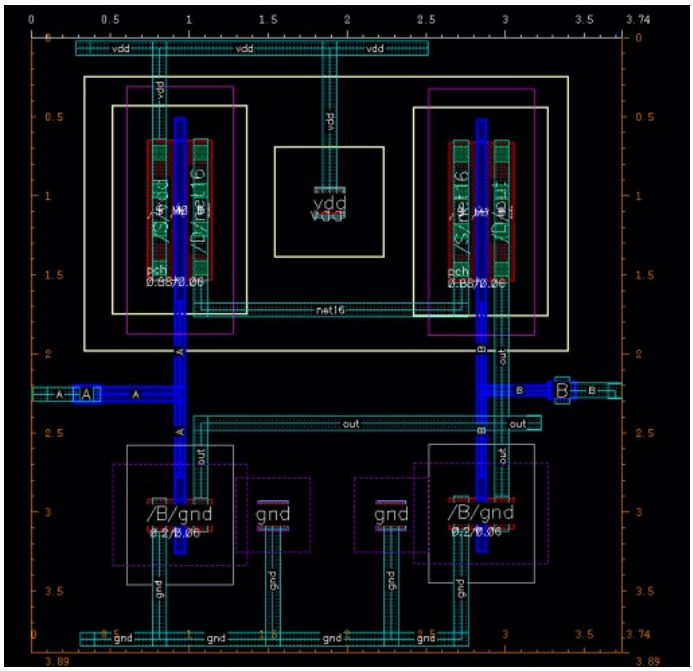


Transient Analysis

Inferences

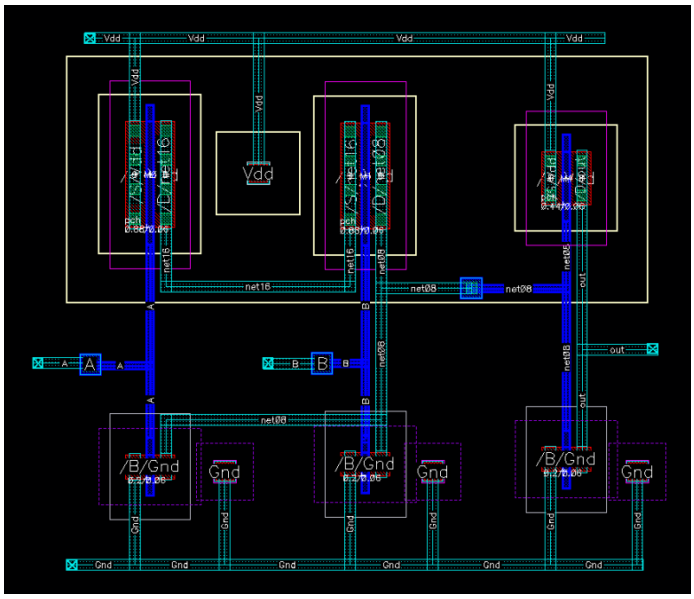
- For case 1:
  Rise Time is 0.0068ns (10.0118-10.005) when B=0 and A =1→0
  For case 2 :
  Rise Time is 0.0044ns when A=0 and B=1→0
  For case 3:
  Rise Time is 0.0063ns when A=B=1→0
- Justification For Inference 1 :
  Case 2 is best Case because upper transistor in PUN is ON from start itself so its total capacitance is charged already before switching that's why delay is minimum in this case.
  Case 3 and 1 is having little difference that is because of body effect and they are having significant difference with case 1 because of in these two case total capacitance of both the transistor of PUN needs to be charged.
- For case 1:
  Fall Time is 0.0091ns (60.0141-60.005) when B=0 and A =0→1
  For case 2 :
  Fall Time is 0.0057ns when A=0 and B=0→1
  For case 3:
  Fall Time is 0.004ns when A=B=0→1
- Justification for inference 3 :- Case 3 is the best case because in this case both NMOS in PDN are turning on so collectively they will take lesser time to discharge the capacitance. Time Difference between Case 1 and Case 2 is because in case 1 upper transistor in PUN is turning OFF but lower transistor is still ON so we need to discharge its total capacitance that's why case 1 is worst case scenario.
- The Static power consumption for these logic is also approximate to Zero same as an inverter because at a time either PUN is ON or PDN is ON so there isn't any direct Connection between VDD and GND.
- Dynamic Power consumption is still there that is because for a small duration of time Both PUN and PDN transistors are in saturation region so there is a direct connection between Vdd and Ground.

C. Layout For NOR gate



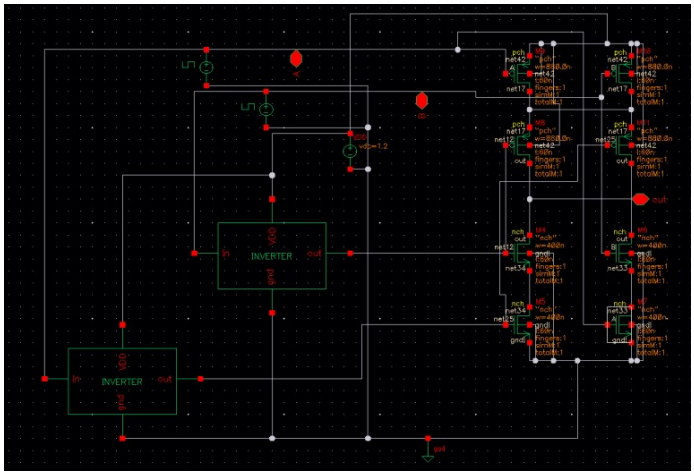
- Here we have used P-type wafer so to implement the PUN we Dig N well inside it.
- Area for this gate is approximately equals to 2*(440*60 + 400*60)→100.8 micro meter (Sum of area of all the transistors).
- In layout We need to arrange the transistor parallely in PUN and PDN this is because when we will be using them in larger network than there we are having two straight parallel Wire for VDD and GND So we need to maintain a required height for net layout design as well as we have to keep them in parallel fashion.

D. Layout For OR gate

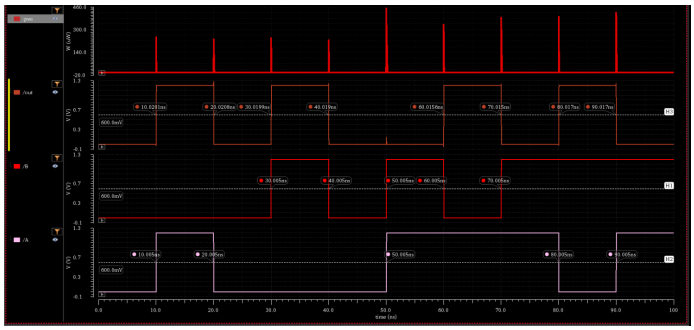


Just one extra inverter is connected here so just two extra mosfet(pmos and nmos) area will be added in the previous case.

E. Schematic of XOR Gate:



F. Transient analysis and Power analysis of XOR gate

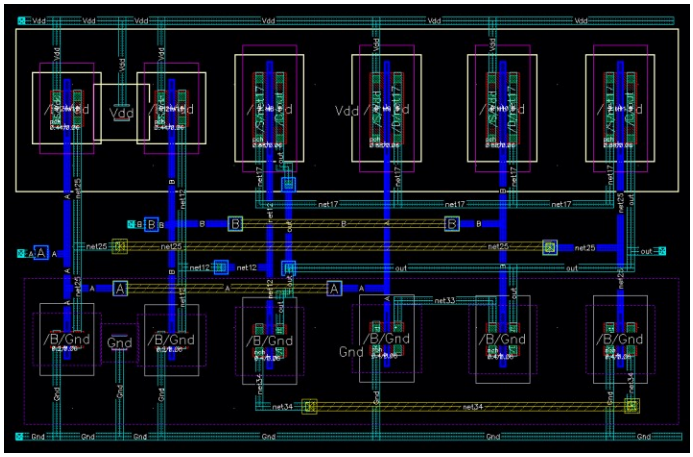


Inferences

- For Rise Time

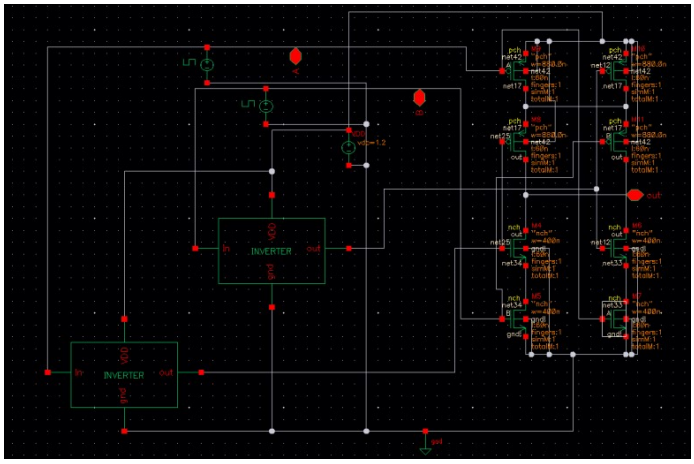
  Case 1 : 0.0151ns(10.0201-10.005) for B=0 , A=0→1.
  Case 2 : 0.0149ns for A=0 , B=0→1.
  Case 3 : 0.0106ns for A=1 , B=1→0.
  Case 4 : 0.012ns for B=1 , A=1→0.
- Worst case is in Case 1 where B=0 , A=0→1 because here in PUN upper transistor is already ON so after switching it will not take time to charge it's total capacitance.
  Case 2 has little smaller delay with that off Case 1 that's because body effect. Best Case is in Case 3 where A=1 , B=1→0 because here we need to charge both transistor in PUN because transistor which is directly connected to VDD was switched off initially.
  Case 4 has little smaller delay with that off Case 3 that's because body effect.
- For Fall Time
  Case 1 : 0.0158ns(20.0208-20.005) for B=0 , A=1→0.
  Case 2 : 0.014ns for A=0 , B=1→0.
  Case 3 : 0.01ns for A=1 , B=0→1.
  Case 4 : 0.012ns for B=1 , A=0→1.
- Best case is Case 3 when A=1 , B=0→1.
  worst Case is Case 1 when B=0 , A=1→0.

G. Layout of XOR Gate:

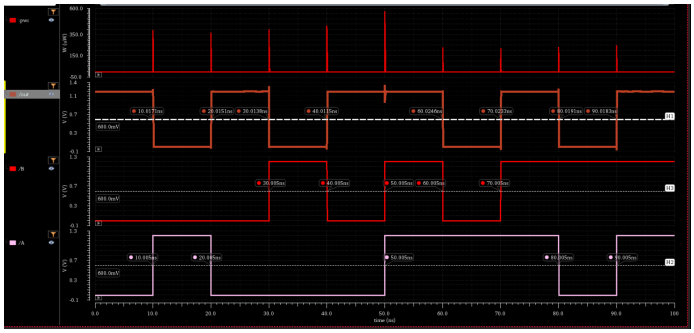


Inferences :-
Inference is exactly same as that of NOR gate just area has increased because number of transistor are also increased.

H. Schematic of XNOR Gate:

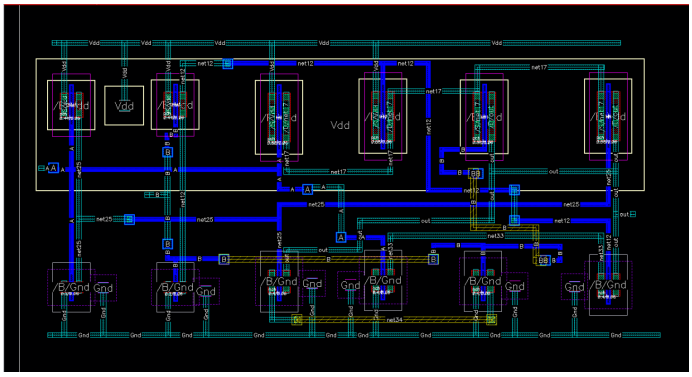


I. Transient analysis and Power analysis of XNOR gate



- For Rise Time
  Case 1 : 0.0101ns(20.0151-20.005) for B=0 , A=1→0.
  Case 2 : 0.0065ns for A=0 , B=1→0.
  Case 3 : 0.0183ns for A=1 , B=0→1.
  Case 4 : 0.0133ns for B=1 , A=0→1.
    - Best Case occurs when A=0 , B=1→0.
      Worst case occurs when A=1 , B=0→1.
- For Fall Time
  Case 1 : 0.0121ns(10.0171-10.005) for B=0 , A=0→1.
  Case 2 : 0.0088ns for A=0 , B=0→1.
  Case 3 : 0.0196ns for A=1 , B=1→0.
  Case 4 : 0.0141ns for B=1 , A=1→0.
    - Best Case occurs when A=0 , B=0→1.
      Worst case occurs when A=1 , B=1→0.

J. Layout For XNOR gate



Conclusion

- Rise Time(Tlh) and Fall time(Tphl) can vary between different cases that depends on transistor switching.
- Whenever designing circuit we needs to take worst case scenarios into consideration so that our chip doesn't fail.
- Power(dynamic) Dissipation also depends on the input patterns if both inputs change their logic level simultaneously than it will be relatively higher than the other cases.

IV. References

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Jan Rabaey - Digital Integrated Circuits
https://www.quora.com/Why-do-we-need-to-use-P-substrate-for-NMOS-and-N-substrate-for-PMOS