Rahul Yadav, B20059, Assignment , EE-623P , Problem-8

Control of buck Converter

❖ Objective :-

Parameter set of a digital voltage mode-controlled synchronous buck converter is given below:

L (uH) = 7, C (uF)=200, R(Ohm) = 3, Switching Freq. (fsw) =300Khz, Input voltage (V) =12, Output Voltage (V) =7 Capacitor ESR (mOhm) =30

Derive a small-signal model and design a suitable voltage loop controller to achieve compensated loop bandwidth fsw/10 (roughly) and phase margin >45 deg. Choose proper quantization level for the error voltage and DPWM to ensure stable operation. Assume ripple voltage is less than 1% of the output voltage. Show the load transient performance using a MATLAB Simulink model. Assume the modulator delay and control loop delay are present in the control loop and the total delay is equal to 0.7 µs. Now add the total delay in the control loop and do the simulation. Note down the difference with the previous simulation and explain the reason.

❖ Small Signal Model :-

⇨ $\hat{x}$=$A\hat{x} + B\hat{u} + f\hat{d}$

⇨ $\hat{x}$=$A\hat{x} + f\hat{d}$ $\quad \therefore u = 0$

Taking Laplace transform

⇨ sX$(s) = AX(s) + fD(s)$

⇨ $(sI - A)X(s) = fD(s)$

⇨ X$(s) = (sI - A)^{-1} fD(s)$

⇨ Vo(s)= $CX(s)$

⇨ Vo$(s) = C\ (sI - A)^{-1} fD(s)$

⇨ $\frac{Vo(s)}{D(s)} = \left((\boldsymbol{\alpha} * rc * s) + \frac{\boldsymbol{\alpha}^2 * rc}{R*C} + \left(\frac{\boldsymbol{\alpha}^2}{C}\right)\right) * \frac{\left(\frac{Vin}{L}\right)}{\left(s+\left(\boldsymbol{\alpha}*\frac{rc}{L}\right)\right)*\left(s+\frac{\boldsymbol{\alpha}}{R*C}\right)*\left(\frac{\boldsymbol{\alpha}^2}{L*C}\right)}$

⇨ $\frac{Vo\ (s)}{D\ (s)} = \frac{5.092e04\ s + 8.487e09}{7.002e08\ s\text{^}2 + 4.127e12\ s + 4.903e15}$

Here ,

⇨ $A1 = A2 = \begin{bmatrix} \frac{-\boldsymbol{\alpha} rc}{L} & \frac{-\boldsymbol{\alpha}}{L} \\ \frac{\boldsymbol{\alpha}}{C} & \frac{-\boldsymbol{\alpha}}{RC} \end{bmatrix}$

⇨ $B1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$, $B2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$

⇨ $C1 = C2 = [\boldsymbol{\alpha} rc \quad \boldsymbol{\alpha}]$

❖ MATLAB CODE :-

```
clc;
clear all;
s=tf('s');
Vin=12;
Vout=7;
R=3;
L=7*10^-6;
C=200*10^-6;
rc=0.03;
alpha = R/(R+rc);
Gvd=((alpha*rc*s)+((alpha*alpha*rc)/(R*C))+(a
lpha*alpha/C))*(Vin/L)/((s+(alpha*rc/L))*(s+(
alpha/(R*C)))*(alpha*alpha/(L*C)))
bode(Gvd);
pzmap(Gvd);
margin( Gvd )
hold on
wa=13.2e3;
wb=132e3;
k1=200000000;
C1 = k1*(1+s/wa)/(1+s/wb);
resultant = Gvd*C1;
margin(resultant);
```

❖ Equation of compensator c1:-

⇨ $C1 = k1 * \frac{\left(1+\frac{s}{wa}\right)}{\left(1+\frac{s}{wb}\right)}$

⇨ $200000000 * \frac{\left(1+\frac{s}{13200}\right)}{\left(1+\frac{s}{132000}\right)}$

❖ Resultant Equation

⇨ $C1 * Gvd$

⇨ $\frac{1.344e18\ s^2 + 2.418e23\ s + 2.957e27}{9.243e12\ s\text{^}3 + 1.275e18\ s\text{^}2 + 7.255e21\ s + 8.543e24}$

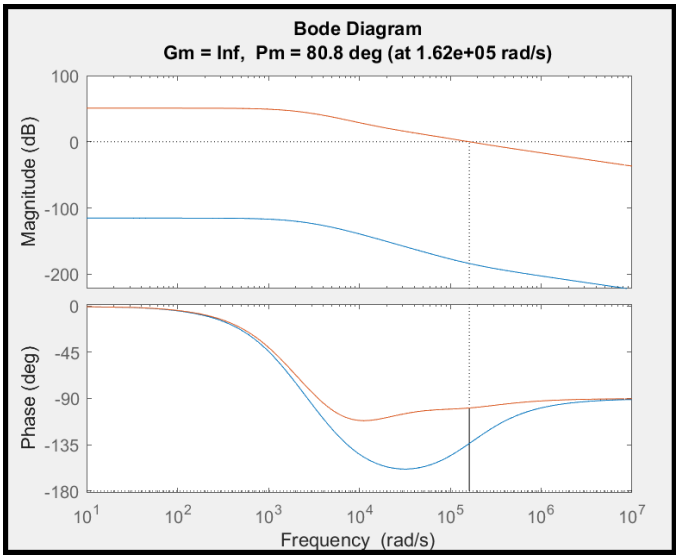
We do not need to work with C2 as we have already got the desired results with C1.

Rahul Yadav, B20059, Assignment , EE-623P , Problem-8

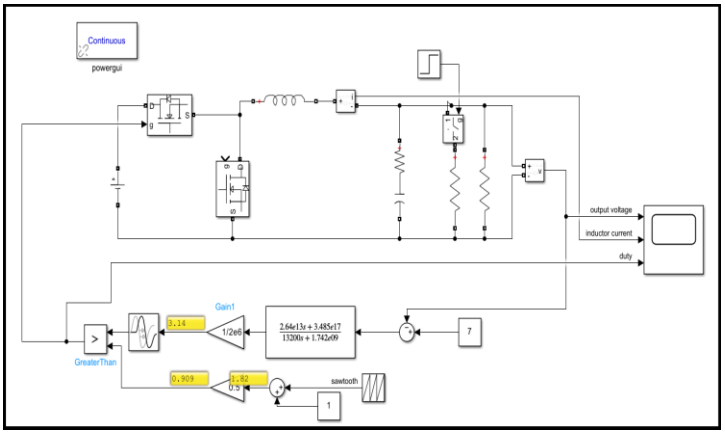
Control of buck Converter

❖ Bode Plot

Orange waveform is uncompensated plot whereas blue waveform is compensated plot.
As we can see we have a bandwidth of 1.62e5 rad/s which is almost equal to $\frac{300}{10} = 30Khz$.
Phase Margin we have is greater than 45degree.



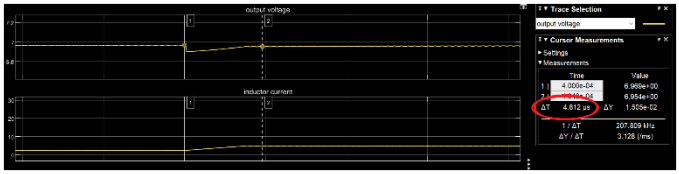
Simulink Model:-



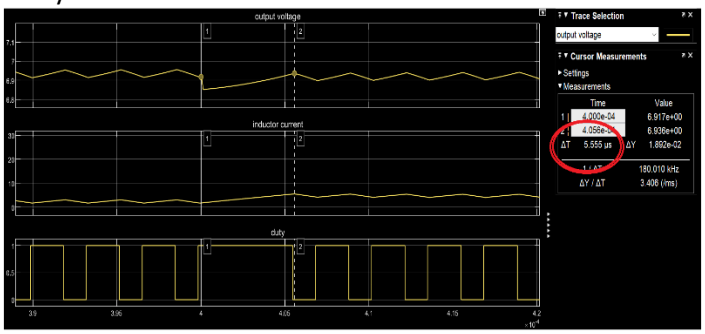
Simulink Results:-

Transient Results :-

Here when load is switched from 3 ohm to 1.5ohm at 0.0004sec output voltage takes a dip and rises to 6.95v in 4.891us.



After introducing the modulator delay and control loop delay of 0.7us :-



As we can see from the above plot that it is taking 5.55us to recover that is almost equal to the additional 0.7us to the previous case.

So, the addition of delay introduces the delay in the output response.

CONCLUSION:-

We have successfully done the control of Buck converter with the tuning of compensator. Also, we have successfully verified the transient performance of the system with variable load.