# Sense Amplifier

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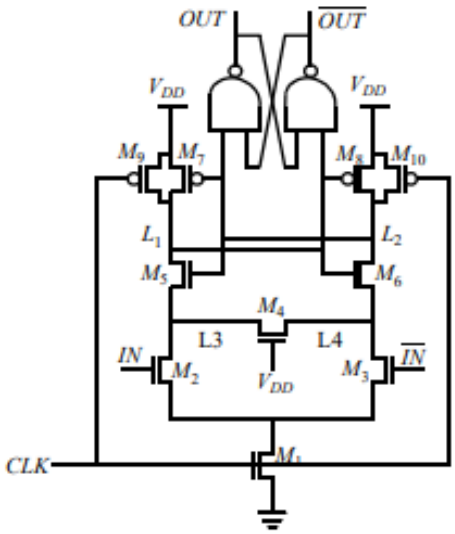
***Abstract*—In this assignment, we have designed a sense amplifier-based register with appropriate transistor sizing in Cadence Virtuoso 60nm technology. We ran a functional simulation of the design to determine setup time, hold time, and Tcq delay.Aside from that, the design layout is created.**

## I. Introduction



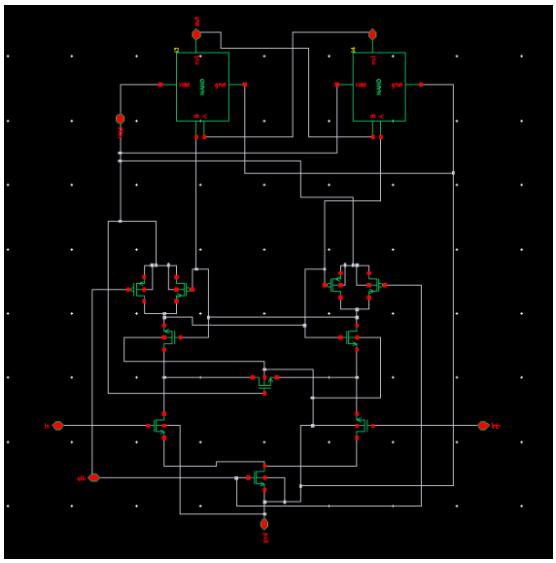

Master-slave idea and the glitch technique are two essential methods for creating edge-triggered registers. Another method is shown in Fig1, which employs a sensing amplifier arrangement to create an edge-triggered register.
Small input signals are amplified by sense-amplifier circuits to produce rail-to-rail swings. We shall see that sense amplifier circuits are often used in low swing bus drivers and memory cores to magnify small voltage swings occurring in densely loaded wires.

### A. Working of Sense Amplifier :

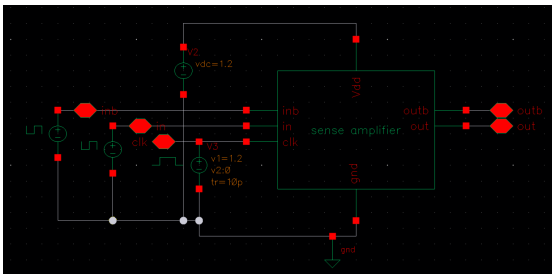
In the circuit showed in Fig1, the differential input signal is sampled by a precharged front-end amplifier at the rising edge of the clock signal. A NAND cross-coupled SR FF that keeps the data and ensures that the differential outputs switch only once every clock cycle receives the outputs from the front-end. The circuit has a front-end consisting of a cross-coupled inverter (M5 -M8), whose outputs (L1 and L2) are precharged using devices M9 and M10 during the low phase of the clock. Transistor M1 is similar to an evaluate switch in dynamic circuits and is turned off ensuring that the differential inputs don't affect the output. On the rising edge, the evaluate transistor turns on and the differential input pair (M2 and M3) is enabled, enabling the use of low-swing signaling on the input wires..

## II. Result And Inferences

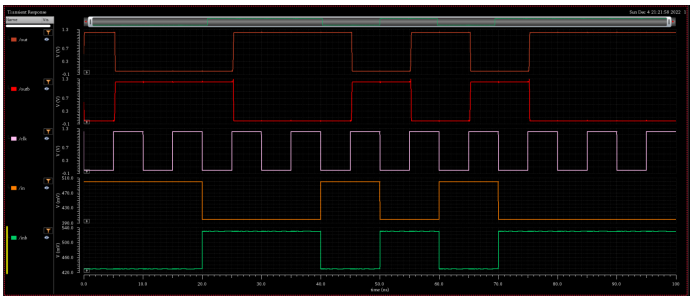
### A. Schematic of Sense Amplifier



### B. Symbol of Sense Amplifier



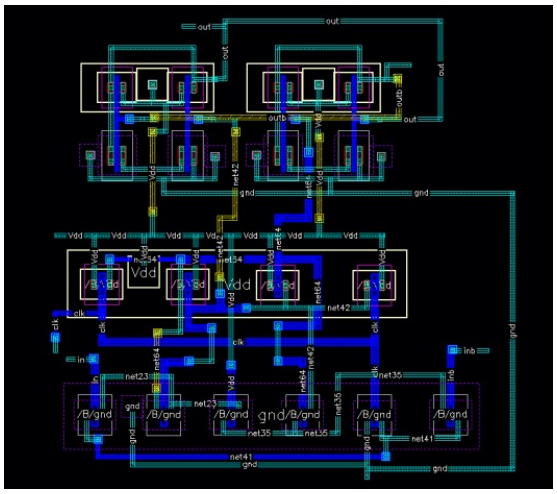
### C. Input/Output waveform of Sense Amplifier



**Inferences :**

- Total total number of transistors used in the sense amplifier is 10 + 8(NAND Gate) = 18 transistors.
- Input Signal volatage given in this design is 400mV for logic 0 and 500mV for logic 1.
- Input Compliment Signal voltage given in this design is 430mV for logic 0 and 530mV for logic 1.
- We can see from this plot that, despite the low voltage difference between IN and INbar, the rail-to-rail swing at the output is around 1.2V (1.199V - 49uV).

### D. Layout of Sense Amplifier




**Inferences :**

- Area for this gate is approximately equals to (100.8 + 260) = (360.8) fermi meter (Sum of area of all the transistors).
- In layout We need to arrange the transistor parallely in PUN and PDN this is because when we will be using them in larger network than there we are having two straing parallel Wire for VDD and GND So we need to maintain a required height for net layout design as well as we have to keep them in parallel fashion.

## Conclusion

In this assignment we have broadly discussed about the sense Amplifier. There is always a trade off between size, performance, power consumption and the cost of the device. Depending on the application, the emphasis will be on different metrics.And approx all the big circuits like processors and so on consists of thousands of registers. So, we need the register to be high speed, power efficient, and made of less hardware as possible. Sense amplifier based register gives better performance and a good way of designing an edge triggered register but as we have seen it takes more no[umber of transistor as compared to that of the master-slave technique.

## III. References

Digital Integrated Circuits (2nd Edition) by Jan M. Rabaey CMOS Invertor and STA concept