****
** (C) Copyright 2013 Xilinx, Inc. All rights reserved.
** This file contains confidential and proprietary information of Xilinx, Inc. and
** is protected under U.S. and international copyright and other intellectual property laws.
****
** ___ ___
** / /\/ /
** /__/ \ /   Vendor: Xilinx
** \ \ \/
** \ \   readme.txt Version: 1.0
** / /   Date Last Modified:
** /__/ /\   Date Created: November 19, 2014
** \ \ / \   Associated Filename:
** __\/__\
**
** Device: N/A
** Purpose: Design Files for Zynq IP Integrator Example Design
** Revision History: 1.0
**
****
**
** Disclaimer:
**
**   This disclaimer is not a license and does not grant any rights to the materials
**   distributed herewith. Except as otherwise provided in a valid license issued to you
**   by Xilinx, and to the maximum extent permitted by applicable law:
**   (1) THESE MATERIALS ARE MADE AVAILABLE "AS IS" AND WITH ALL FAULTS,
**   AND XILINX HEREBY DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS,
**   IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF
**   MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR
**   PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including
**   negligence, or under any other theory of liability) for any loss or damage of any kind or
**   nature related to, arising under or in connection with these materials, including for any
**   direct, or any indirect, special, incidental, or consequential loss or damage (including loss
**   of data, profits, goodwill, or any type of loss or damage suffered as a result of any action
**   brought by a third party) even if such damage or loss was reasonably foreseeable or
**   Xilinx had been advised of the possibility of the same.

** Critical Applications:
**
**   Xilinx products are not designed or intended to be fail-safe, or for use in any application
**   requiring fail-safe performance, such as life-support or safety devices or systems,
**   Class III medical devices, nuclear facilities, applications related to the deployment of

** airbags, or any other applications that could lead to death, personal injury, or severe
** property or environmental damage (individually and collectively, "Critical Applications").
** Customer assumes the sole risk and liability of any use of Xilinx products in Critical
** Applications, subject only to applicable laws and regulations governing limitations on
** product liability.

** THIS COPYRIGHT NOTICE AND DISCLAIMER MUST BE RETAINED AS PART OF THIS FILE AT
** ALL TIMES.

****

This is a simple IP Integrator based Zynq design. A Bus Functional Model Simulation can be run on this design.

This Zynq design can be targeted for the Zed , the ZC702 and the ZC706 evaluation boards.

To implement the design execute the following steps:

1. From the Flow Navigator pane in Vivado, click on **Generate Bitstream** under Program and Debug.
2. Export hardware to SDK clicking **File => Export => Export Hardware**.
3. After the hardware has been exported launch SDK by selecting **File => Launch SDK.**
4. Run the test code on a Zynq board, by following the steps outlined below:
   a. In SDK, which should have launched in a separate window, create a new software application by clicking **File** => **New** => **Application project**. Specify a name of the project. Click Next. Select **Peripheral Tests** from the **Available Templates** box. Click **Finish**. This should compile the peripheral tests source code and all the associated files along with it.
   b. Then program FPGA by clicking **Xilinx Tools** => **Program FPGA**. Make sure that the path to the bit file is correct and click **Program** in the Program FPGA dialog box. The **DONE LED** will turn green, if everything goes smoothly.
   c. Select the Zynq_Design application in the Project Explorer, right click on it and select **Debug As** => **Launch on Hardware (System Debugger)**. In the Confirm Perspective Switch dialog box, click **Yes**.
   d. Set up the terminal from the Terminal Tab in SDK with the following settings:
      i. Connection Type: Serial
      ii. Port: COMXX (where XX is the port number)
      iii. Baud Rate: 115200
      iv. Data Bits: 8
      v. Stop Bits: 1

XILINX INTERNAL

vi. Parity : None

vii. Flow Control: None

viii. Timeout (sec): 5

e. Expand the Debug tab and select the processor core on which your software will run (ARM Cortex - A9 MPCore #0).

f. Press **Resume (F8)**.

g. You should be able to see the output of the peripherals test that the code executes on the terminal.

A simple testbench is included to show BFM simulation of the Zynq processor. The testbench writes to the GPIO and also writes and reads back from the Block Memory through the GP0 port of the Zynq processor.

To simulate the example design, follow the following steps:

1. From the Flow Navigator in Vivado, click on **Run Simulation => Run Behavioral Simulation**.
2. Select **Run => Restart** from the menu. Once simulation starts, type "**run 2500 ns**" in the tcl console and look at the transaction in the waveform window.

Note that you can only run behavioral simulation on the example design.

XILINX INTERNAL