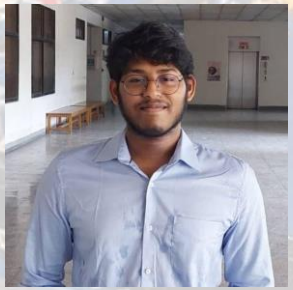
EEE 466-Analog Integrated Circuit Laboratory
July 2023 Level-4 Term-1 Section G2
Final Project Presentation

Designing A Phase Shifter Circuit

SUBMITTED BY – GROUP 07



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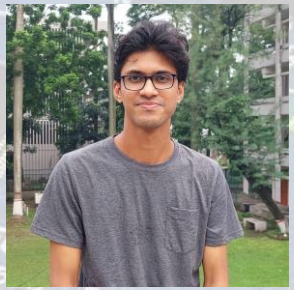

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Outline

1. Summary
2. Introduction
3. Design
4. Implementation
5. Analysis and Evaluation
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Summary / Abstract

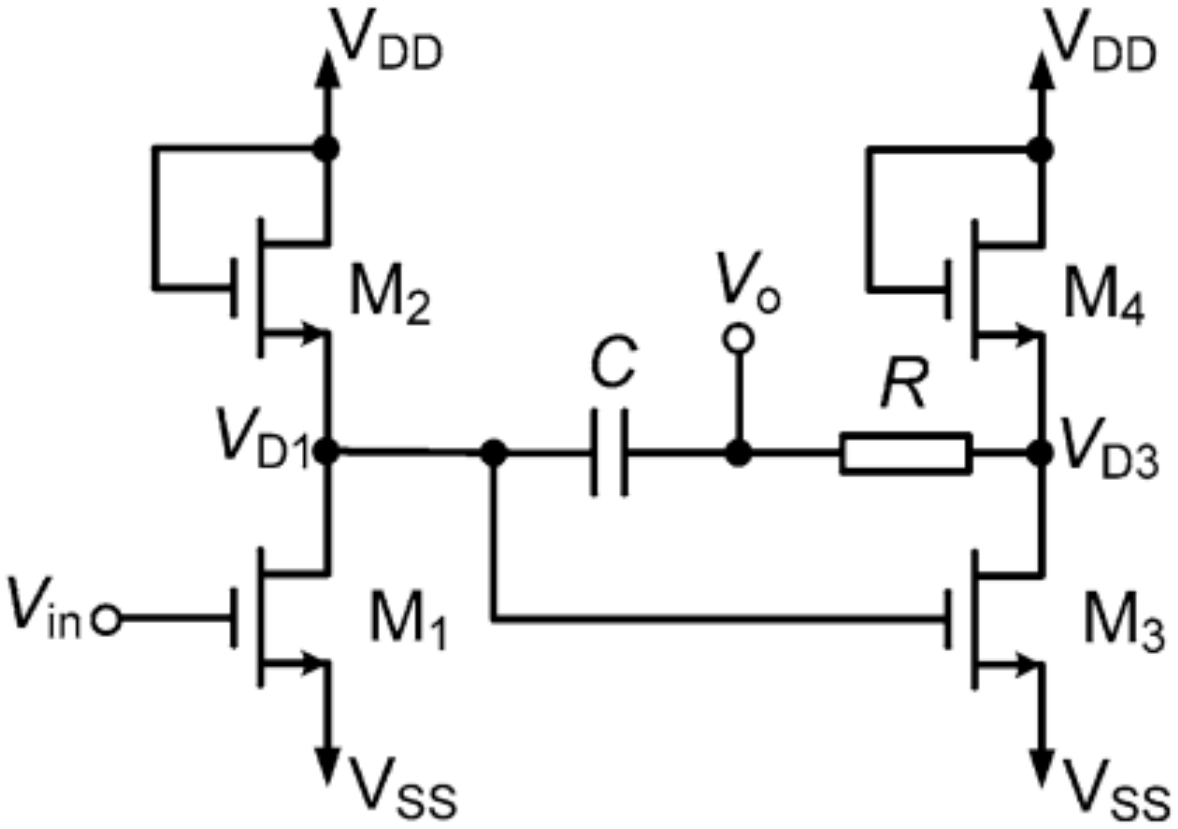
In this presentation, we introduce a voltage-mode (VM) first-order phase shifter, also known as an all-pass filter, which employs only six NMOS and one PMOS transistors. Electronic tunability can be effortlessly achieved by substituting the resistor with an NMOS transistor operating in the triode region. We present simulation results based on gpdk045 CMOS parameters with 2V to 5V supply voltages to showcase the exceptional performance of this proposed phase shifter.

Problem Statement

We have to design a phase shifter circuit with the following specifications:

Specifications	Desired
Frequency Range	1 kHz - 100 kHz
Phase Shift Range	0 - 90 degree
Control Voltage	0 - 1 V
Supply Voltage	2-5 V

Design Methods: Circuit 1



$$V_{D1} = -V_{in}$$

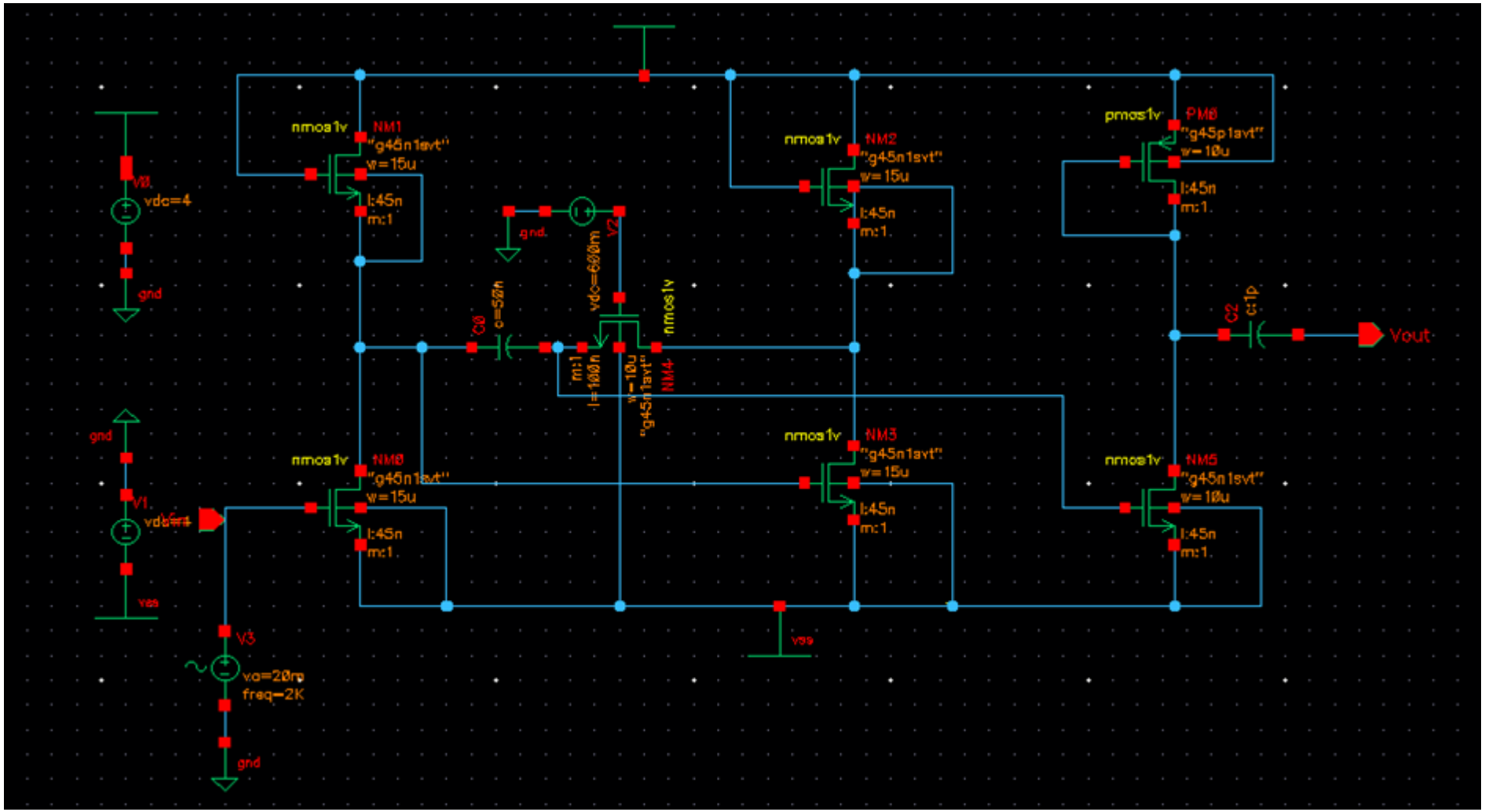
$$V_{D3} = V_{in}$$

$$(V_{D1} - V_o)sC = \frac{V_o - V_{D3}}{R}$$

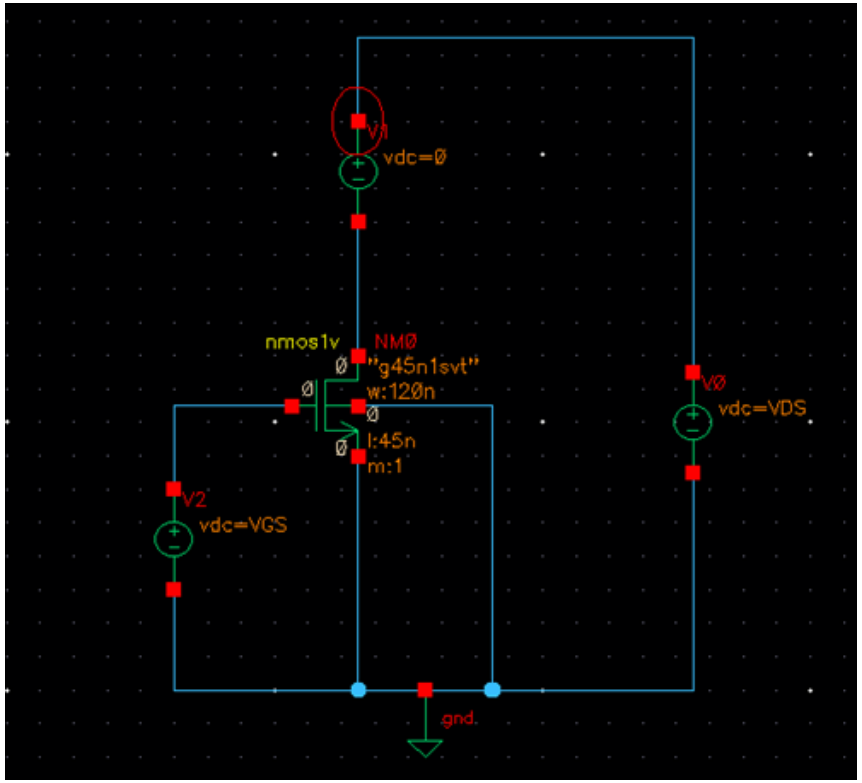
$$\frac{V_o}{V_{in}} = \frac{1 - sCR}{1 + sCR}$$

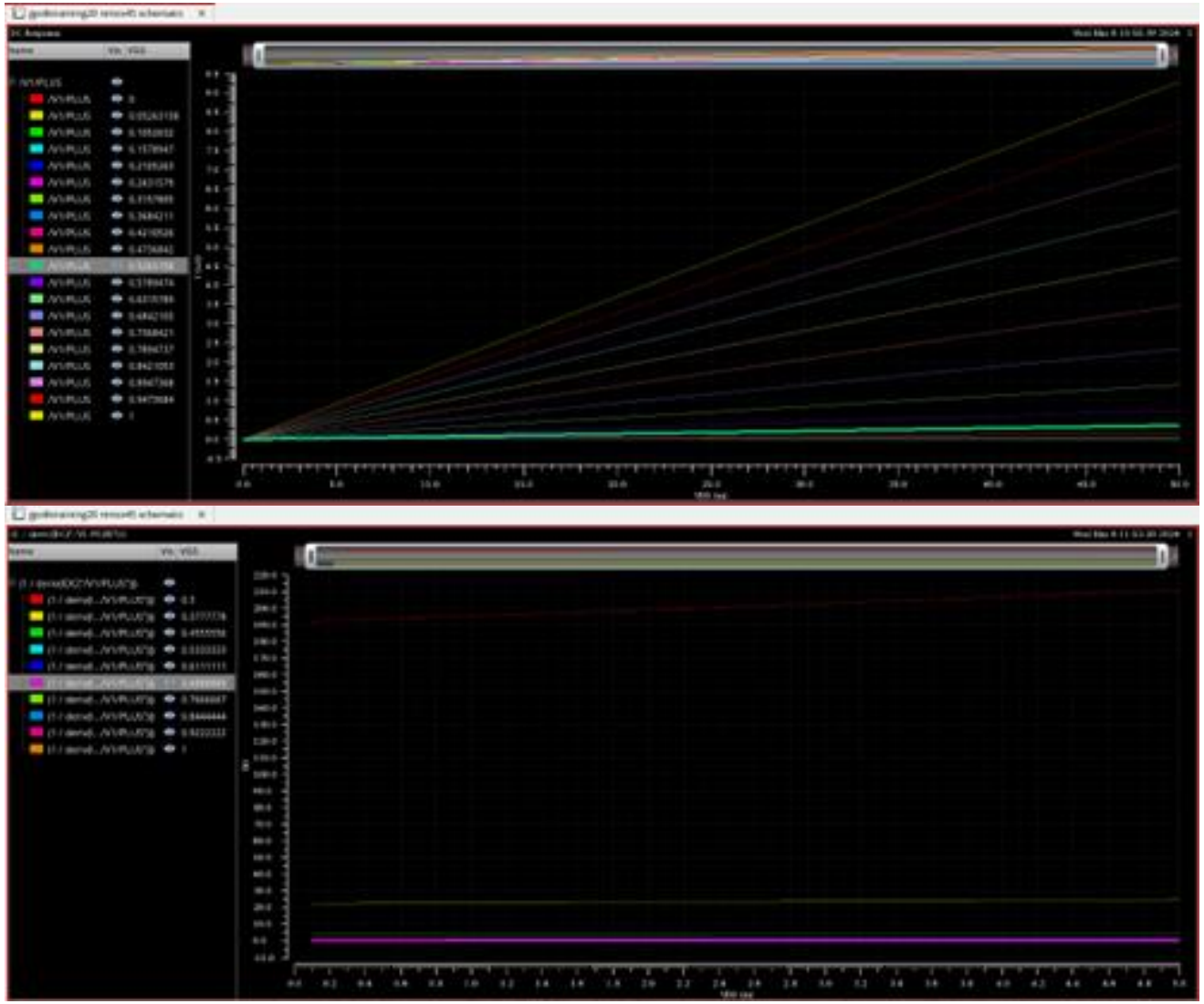
$$\varphi(\omega) = -2\tan^{-1}(\omega CR)$$

Design: Circuit Diagram

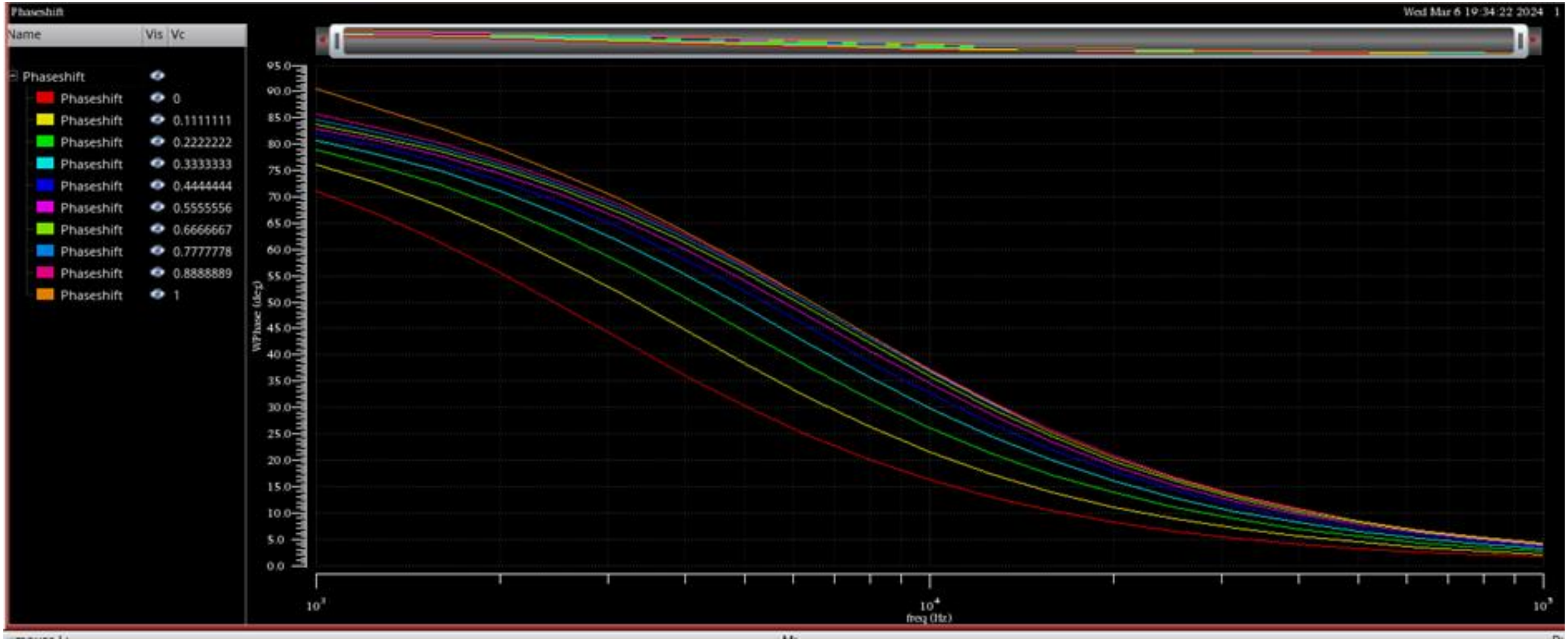


Design: Simulation of NMOS(45 nm)





Design: Phase vs Control Voltage



Output for CV = 0.2 V, f= 2 kHz

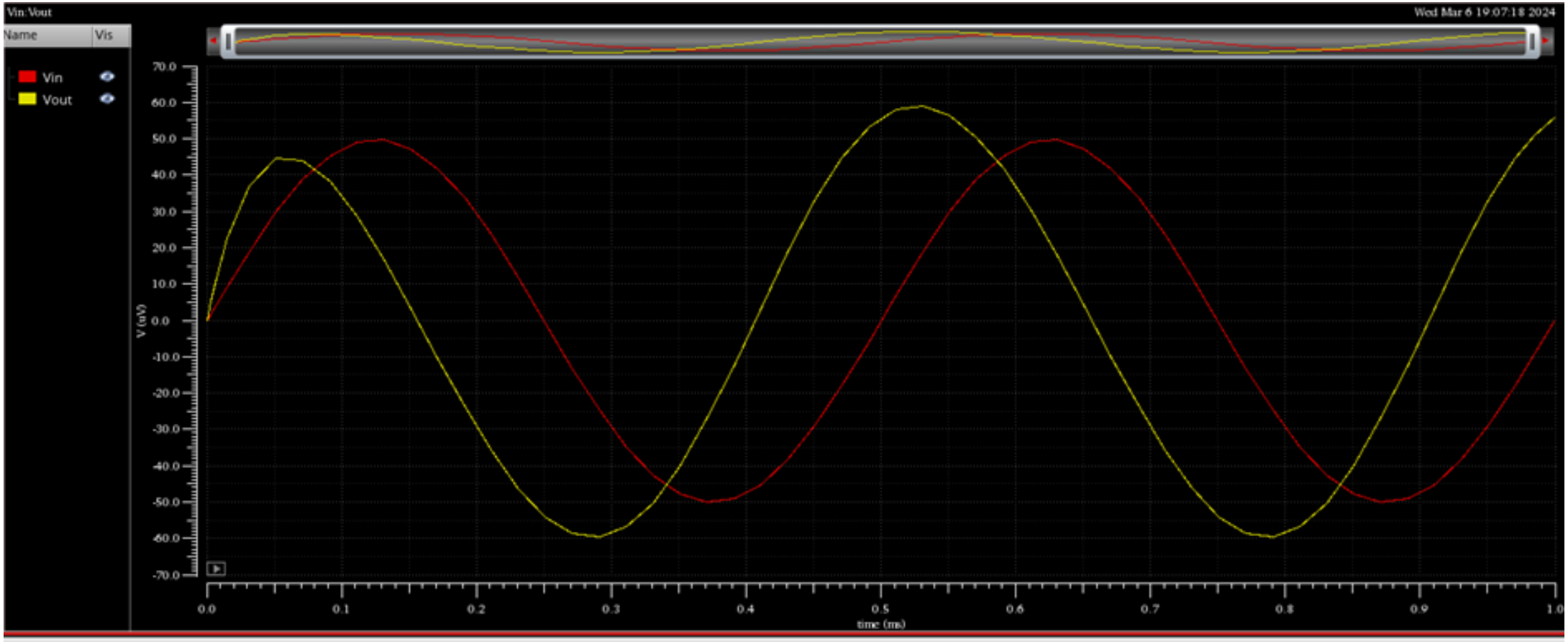
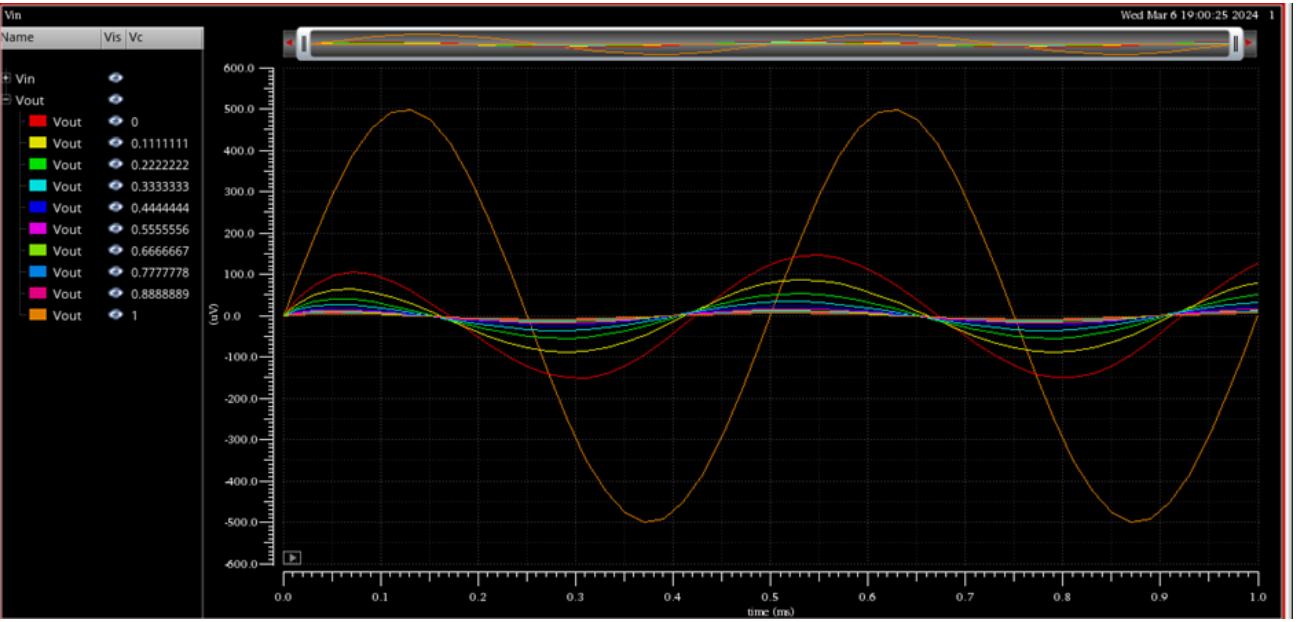
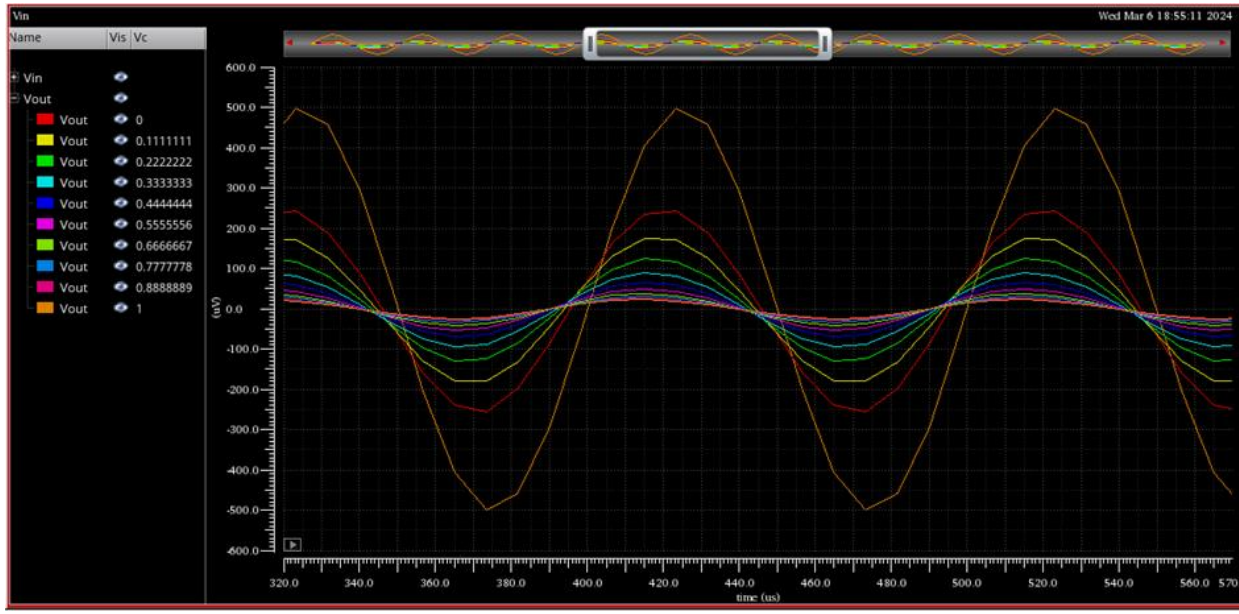
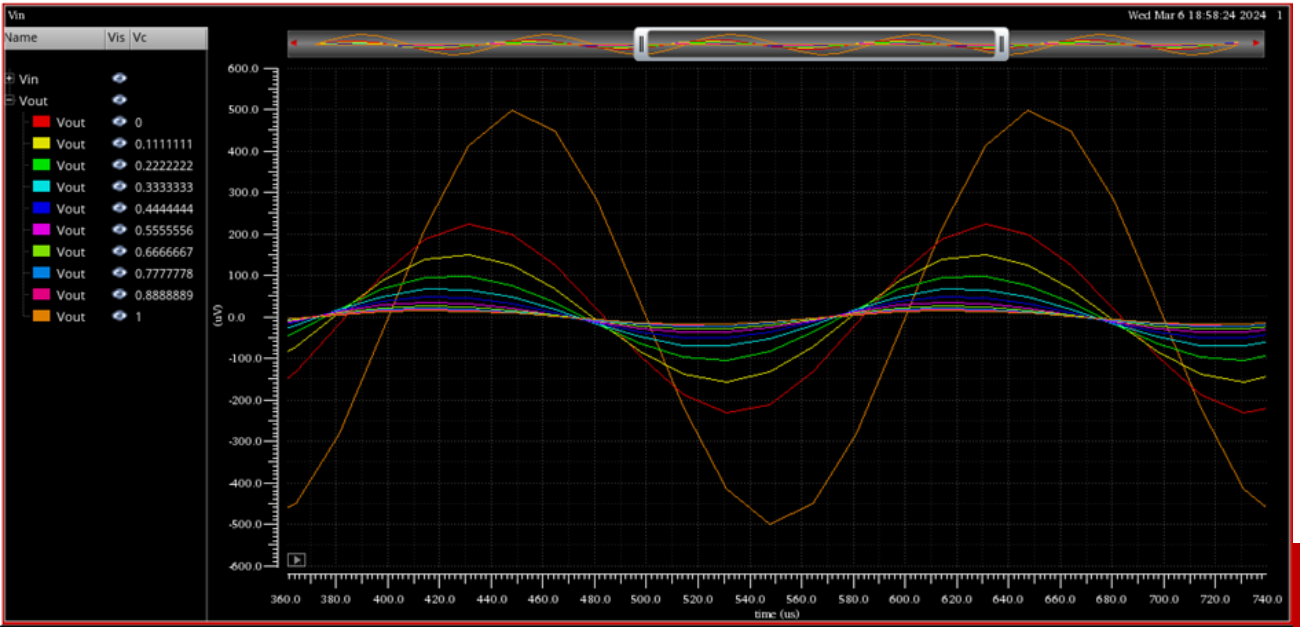
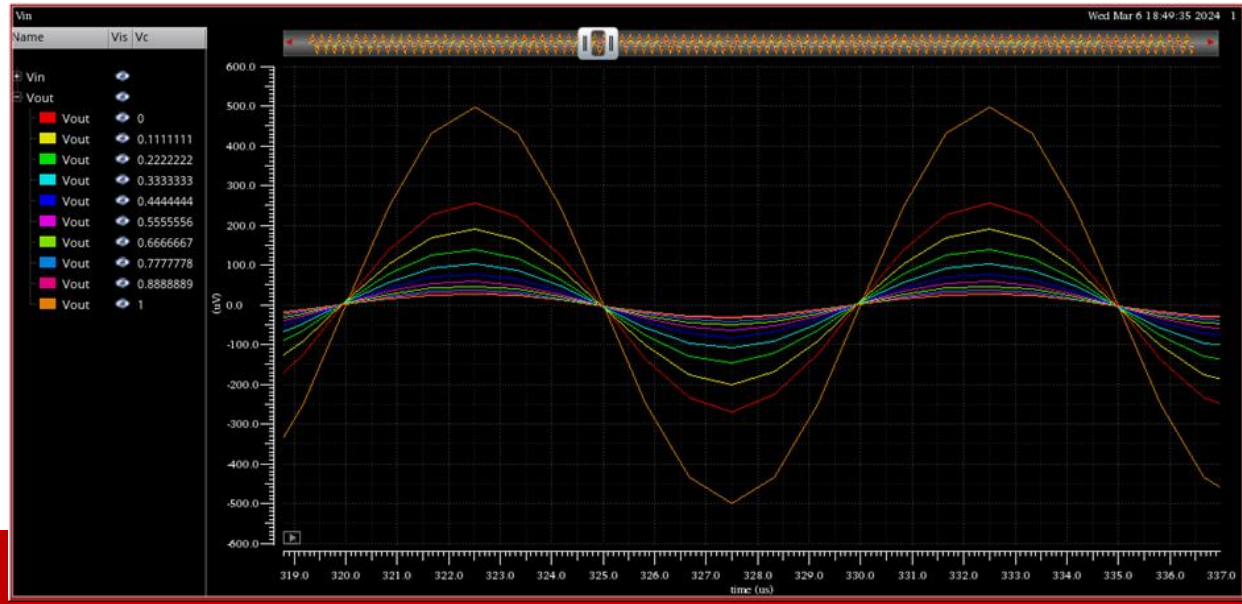


Photo Gallery: Output for f= 2 , 5, 10 & 100 kHz









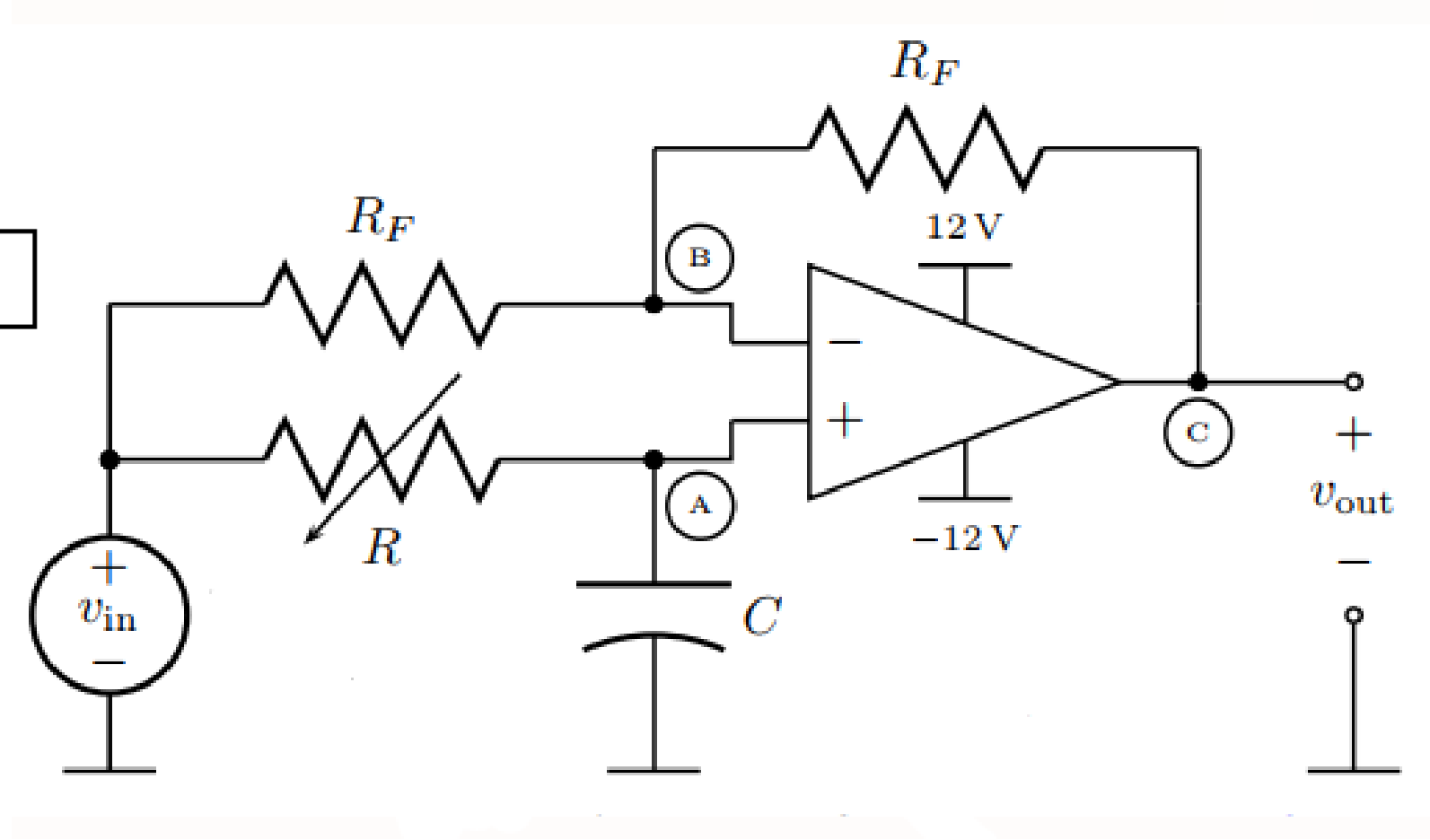
Result

Specifications	Desired	Achieved
Frequency Range	1 kHz - 100 kHz	1 kHz - 100 kHz
Phase Shift Range	0 - 90 degree	0 - 90 degree
Control Voltage	0 - 1 V	0 - 1 V
Supply Voltage	2-5 V	4 V

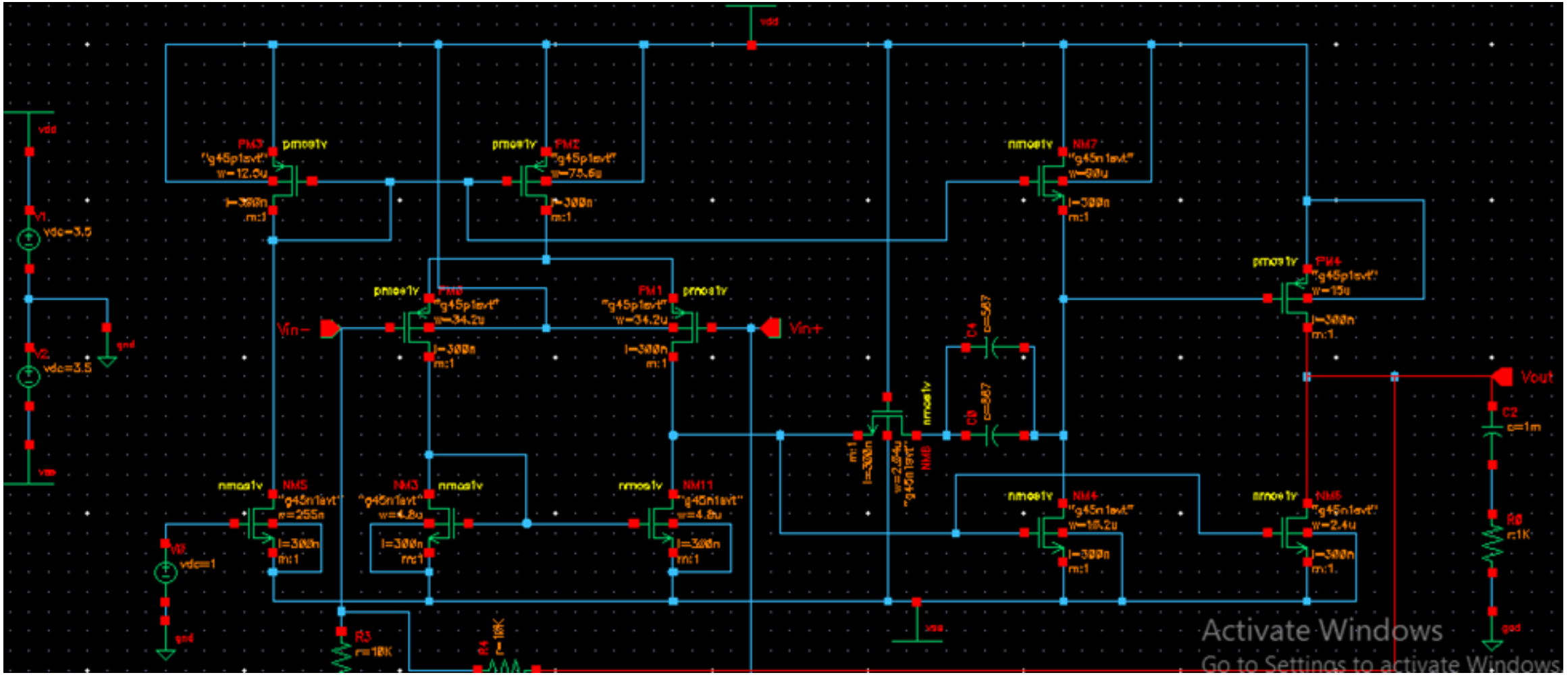
Design Methods: Circuit 2

$$\boxed{\angle H(j\omega)} = \boxed{-2\arctan(\omega RC)}$$

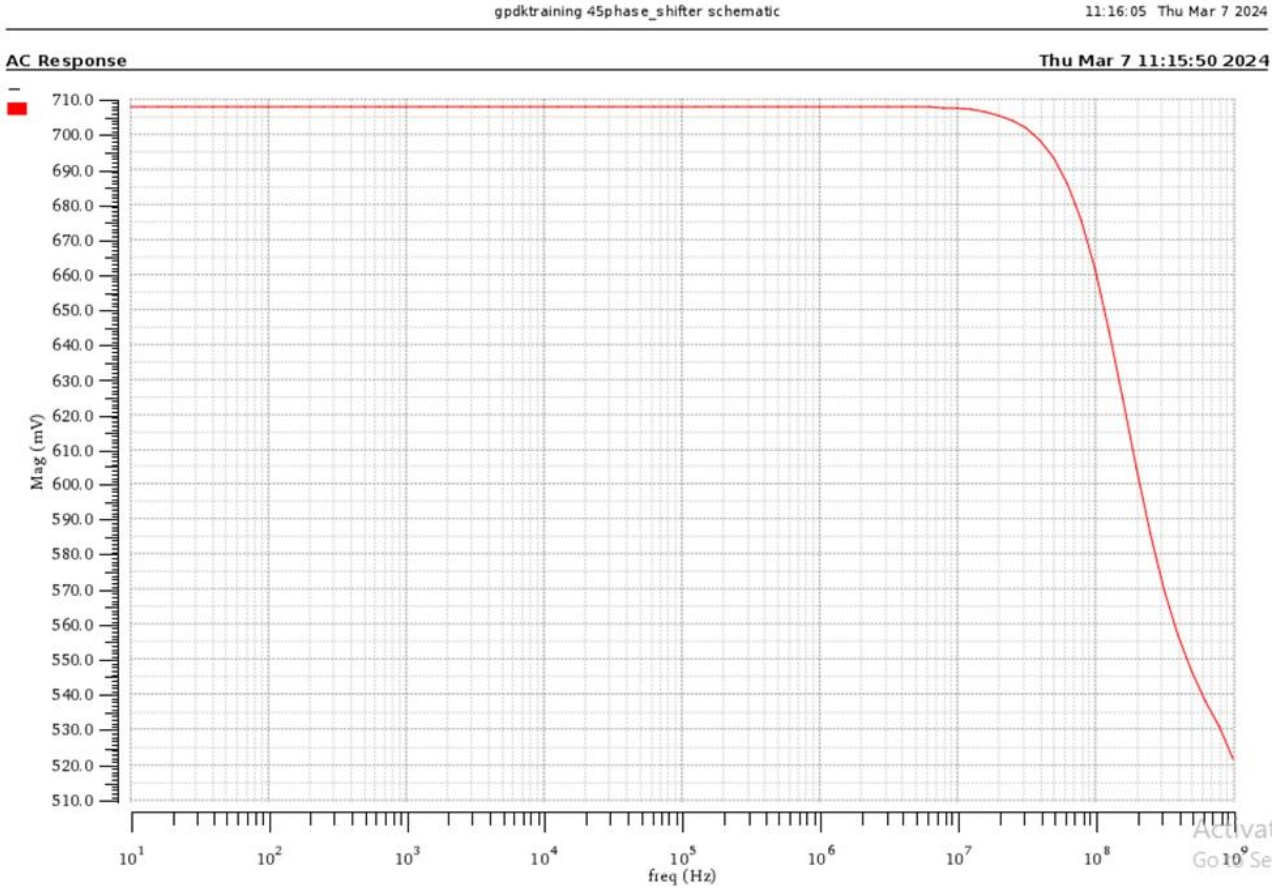
phase: 0 ~ -180 degree

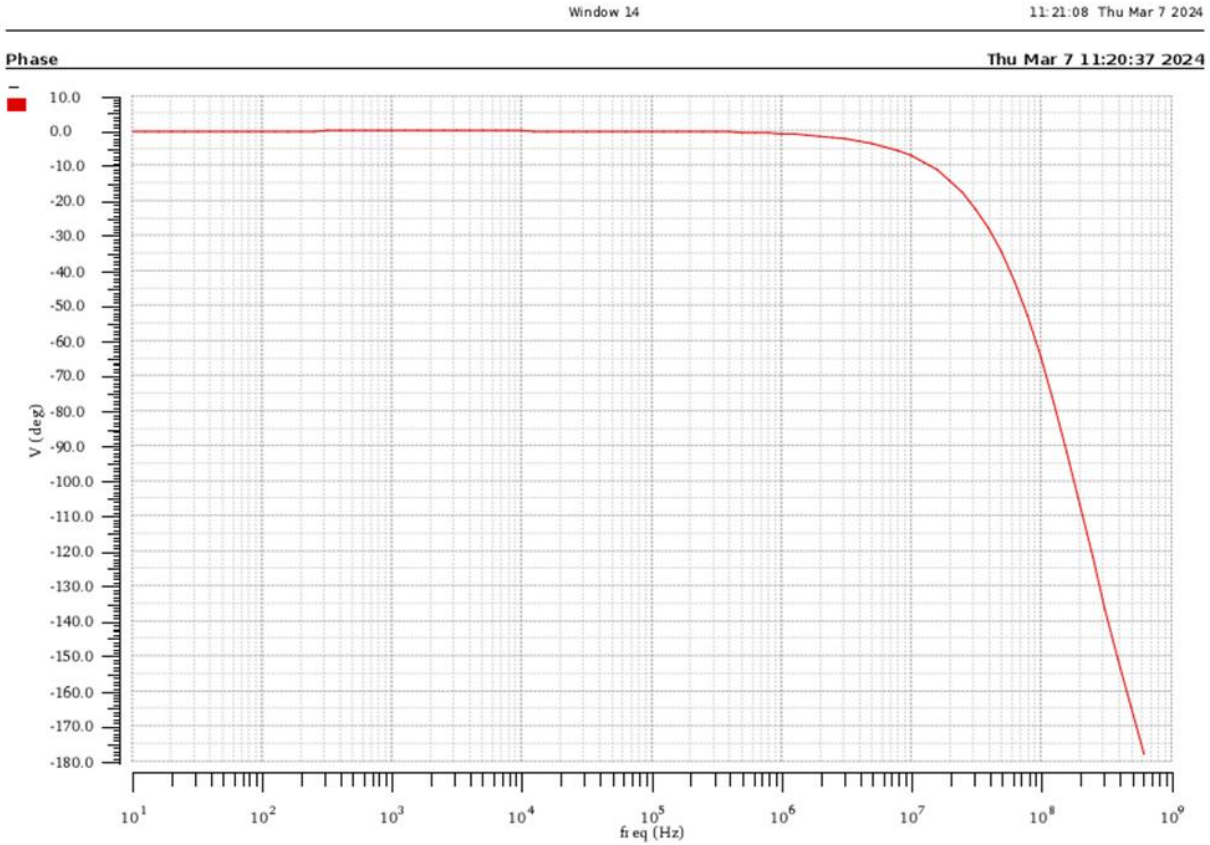


Design Methods: Circuit 2

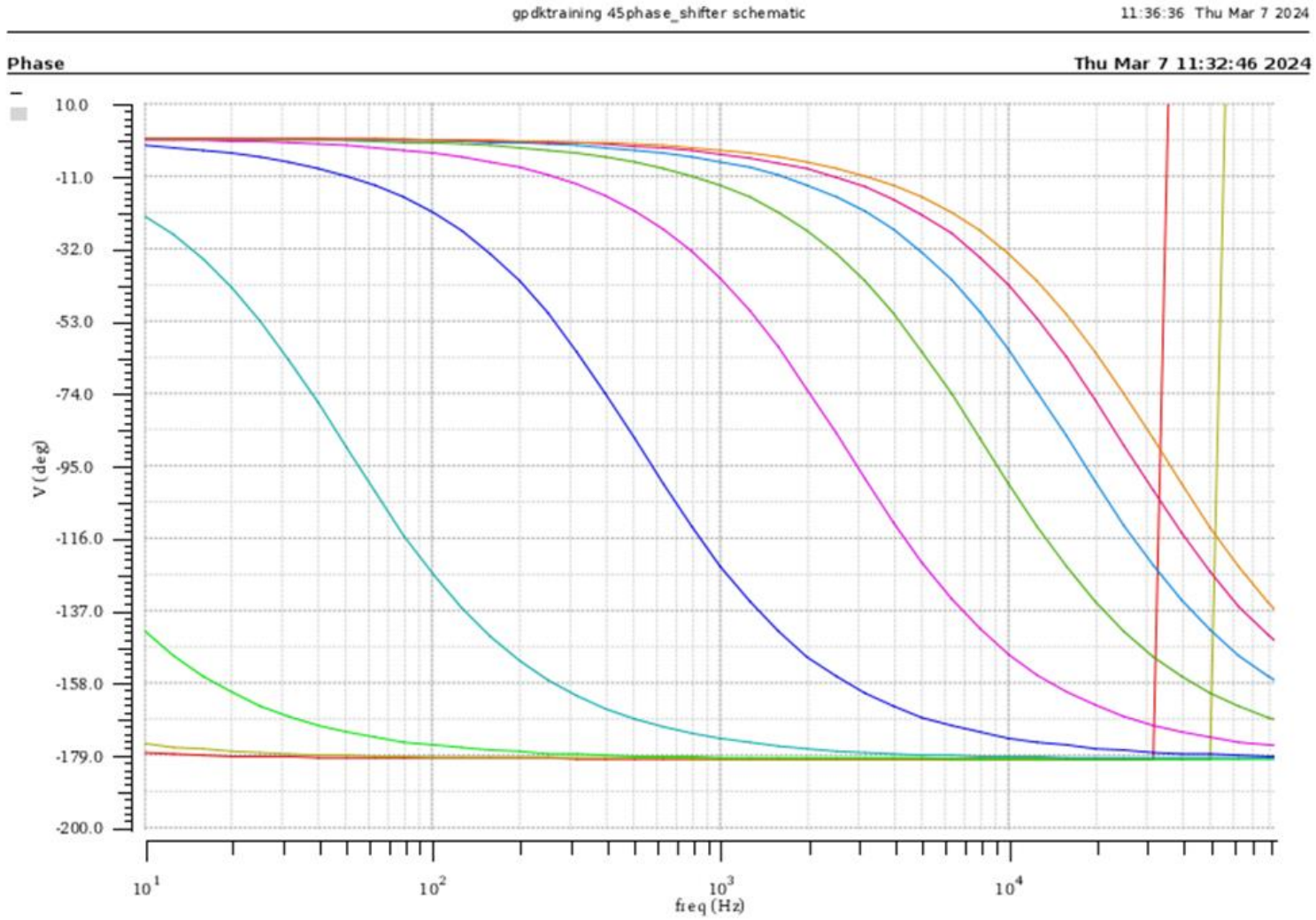


Design: Op -Amp Characteristics

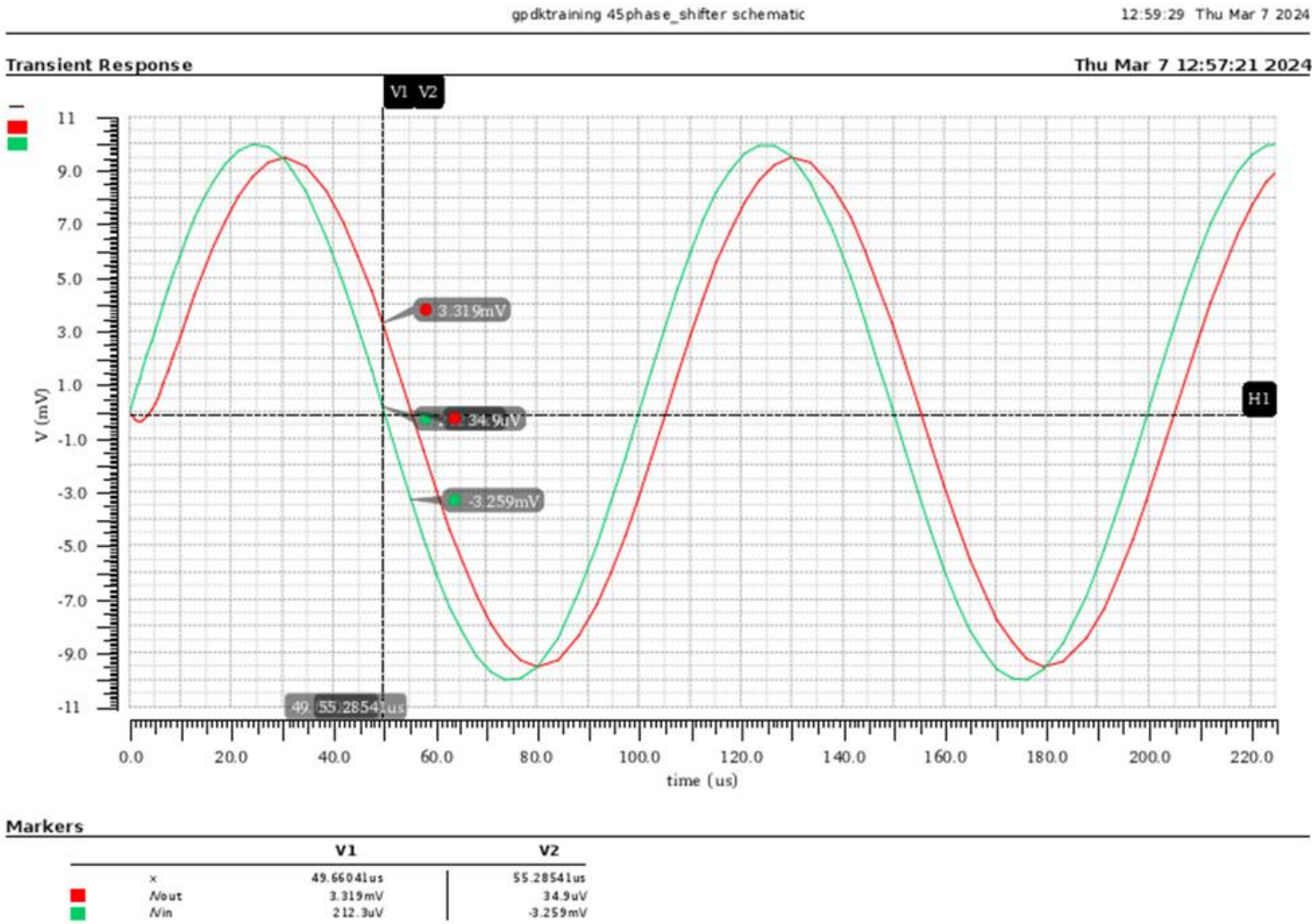




Implementation Demonstration
Phase vs Control Voltage



Transient for CV = 700 mV, f= 10 kHz



Analysis and Evaluation

Specifications	Desired	Achieved (4 MOS based)	Achieved (Op-Amp based)
Frequency Range	1 kHz - 100 kHz	**1 kHz - 100 kHz**	1 kHz - 50 kHz
Phase Shift Range	0 - 90 degree	**0 - 90 degree**	0 - 180 degree
Control Voltage	0 - 1 V	**0 - 1 V**	**0 - 1 V**
Supply Voltage	2-5 V	4 V	**2- 5 V**

Novelty

- Customized Design for Application
- Iterative Optimization
- Advancing Analog IC Design

Practical Considerations of the Design

- Antenna Arrays and Beamforming
- Frequency Synthesis
- RF and Microwave Systems
- Audio and Acoustic Systems
- Communication Systems

References

1. Minaei, Shahram, and Erkan Yuce. "High input impedance NMOS based phase shifter with minimum number of passive elements." Circuits, Systems, and Signal Processing 31 (2012): 51-60.
2. Allen, Phillip E., Robert Dobkin, and Douglas R. Holberg. CMOS analog circuit design. Elsevier, 2011
3. Razavi, Behzad. Design of analog CMOS integrated circuits