Name: Md Raihanul Islam Bhuiyan

Id : 2020239

Section: 12

Course : CSE 340

Assignment: 3

Ans to the Q: N: 1

lw and sw instructions need memory access.

Given that,

lw = 25% and sw = 10%

∴ Fraction of all cycles that the data memory used is = (25 + 10)%

= 35% (Ans)

Ans to the Q.N:2

addi, beq, lw and sw instructions will need the input of the sign extender.

Given that,

addi = 20%, beq = 25%, lw = 25%, sw = 10%

∴ fraction of all cycles where the input of sign extend circuit needed is = (20+25+25+10)%

= 80%

(Ans)

Ans to the Q.N.: 3

Datapath showing the pipeline stages using stall is given below:

lw $f0, 36($f1)

lw $f2, 40($f0)

lw $f3, 44($f2)

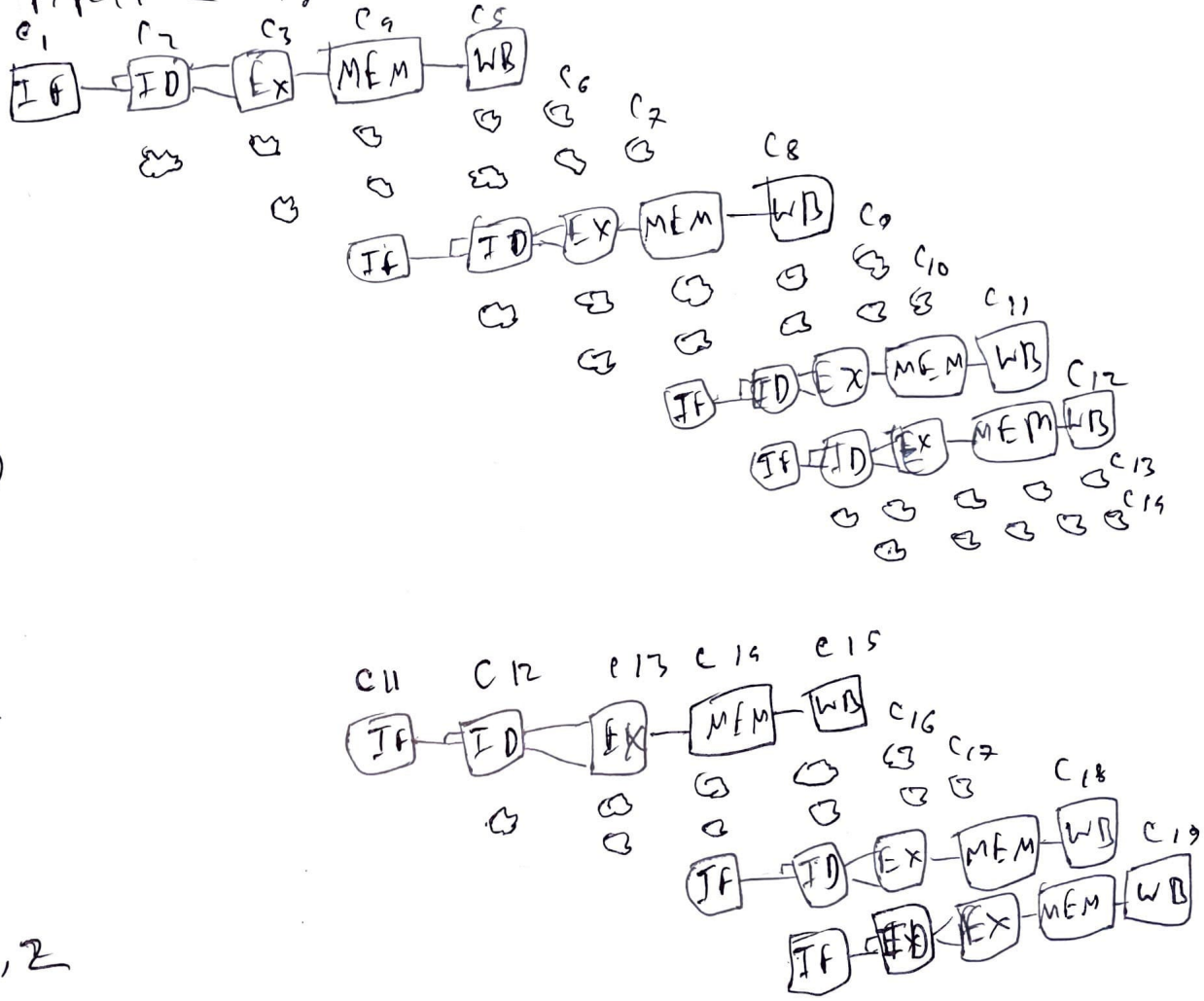
sll $f3, $f2, 2

sub $f0, $f3, $f2

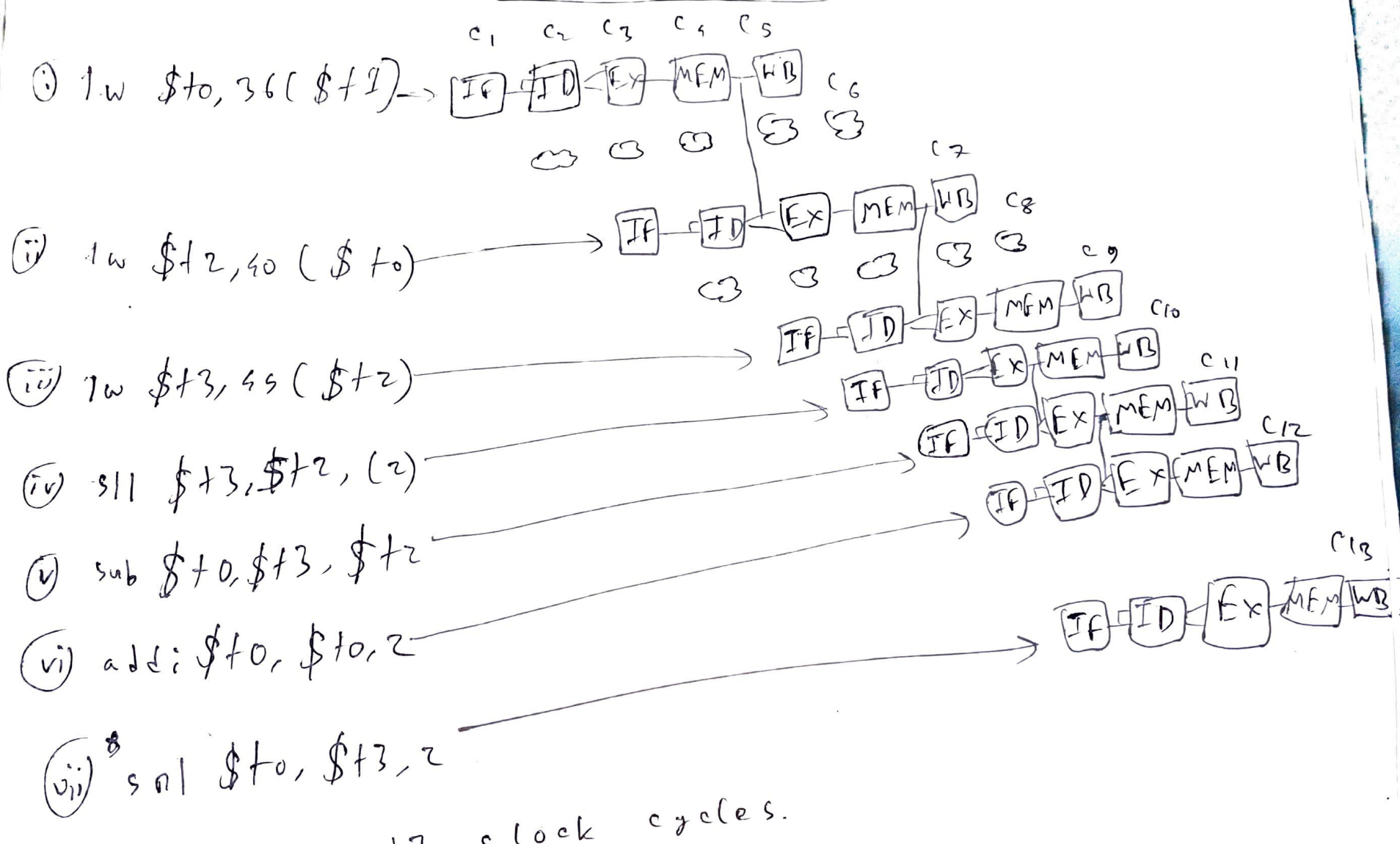
addi $f0, $f0, 2

sal $f0, $f3, 2

$\therefore$ CPI = $\frac{19}{9}$ = 2.714 (Ans)



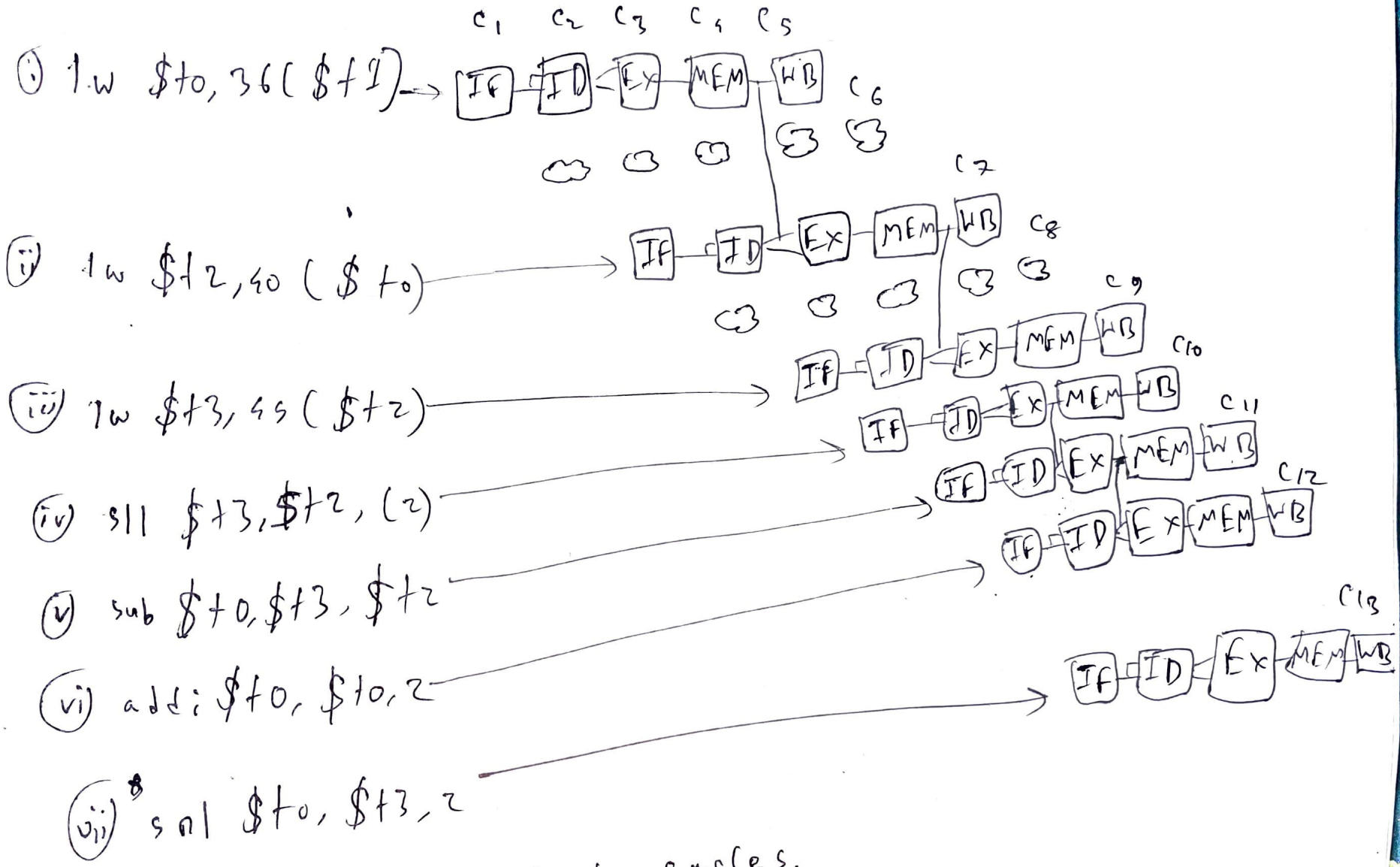
Ans to the Q: N: 4



∴ There are 13 clock cycles.

∴ CPI = $\frac{13}{7}$ = 1.8571 (Ans)

Ans to the Q: N: 5



∴ There are 13 clock cycles.

∴ CPI = $\frac{13}{7}$ = 1.8571

We cannot do scheduling here. Because, it will change the sequence of the code. and will cause error.

So, for the seven lines of MIPS instaction there will be 13 clock cycles.