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For exclusive use of adopters of the book *Digital Design Principles and Practices*, Fourth Edition, by John F. Wakerly,  
ISBN 0-13-186389-4.

1.1 How about a picture of John *not* in a tuxedo?

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**1.2** Three definitions of “bit”:

- (1) A binary digit (pp. 1, 4, 18, 20, 22).
- (2) Past tense of “bite” (p. 1).
- (3) A small amount (pp. 6, 10).

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### 1.3

- ASIC Application-Specific Integrated Circuit
- CAD Computer-Aided Design
- CD Compact Disc
- CO Central Office
- CPLD Complex Programmable Logic Device
- DIP Dual In-line Pin
- DVD Digital Versatile Disc
- FPGA Field-Programmable Gate Array
- HDL Hardware Description Language
- IC Integrated Circuit
- IP Internet Protocol
- LSI Large-Scale Integration
- MCM Multichip Module
- MSI Medium-Scale Integration
- NRE Nonrecurring Engineering
- PBX Private Branch Exchange
- PCB Printed-Circuit Board
- PLD Programmable Logic Device
- PWB Printed-Wiring Board
- SMT Surface-Mount Technology
- SSI Small-Scale Integration
- VHDL VHSIC Hardware Description Language
- VLSI Very Large-Scale Integration

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#### 1.4

ABEL Advanced Boolean Equation Language

CMOS Complementary Metal-Oxide Semiconductor

DDPP Digital Design Principles and Practices

JPEG Joint Photographic Experts Group

MPEG Moving Picture Experts Group

OK Although we use this word hundreds of times a week whether things are OK or not, we have probably rarely wondered about its history. That history is in fact a brief one, the word being first recorded in 1839, though it was no doubt in circulation before then. Much scholarship has been expended on the origins of OK, but Allen Walker Read has conclusively proved that OK is based on a sort of joke. Someone pronounced the phrase “all correct” as “oll (or orl) correct,” and the same person or someone else spelled it “oll korrect,” which abbreviated gives us OK. This term gained wide currency by being used as a political slogan by the 1840 Democratic candidate Martin Van Buren, who was nicknamed Old Kinderhook because he was born in Kinderhook, New York. An editorial of the same year, referring to the receipt of a pin with the slogan O.K., had this comment: “frightful letters . . . significant of the birth-place of Martin Van Buren, old Kinderhook, as also the rallying word of the Democracy of the late election, ‘all correct’ .... Those who wear them should bear in mind that it will require their most strenuous exertions ... to make all things O.K.” [From the *American Heritage Electronic Dictionary (AHED)*, copyright 1992 by Houghton Mifflin Company]

PERL According to some, it’s “Practical Extraction and Report Language.” But the relevant Perl FAQ entry, in perlfaq1.pod, says “never write ‘PERL’, because perl isn’t really an acronym, apocryphal folklore and post-facto expansions notwithstanding.” (Thanks to Anno Siegel for enlightening me on this.)

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### 1.5

- Wrist watches and alarm clocks.
- Cash registers? No, they were never really analog. Rather, they were electro-mechanical digital systems.
- Gasoline pumps.
- Bathroom scales.
- Thermometers and blood-pressure gauges.
- Speedometers.
- Sketches “drawn” by police artists.
- Musical greeting cards.

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- 1.6 The same function is performed by a single 2-input OR gate.

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### 1.7 Never.

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- 1.8 In my book, “dice” is the plural of “die.”

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- 3e2.1    2.1    (a)  $1101011_2 = 6B_{16}$     (b)  $174003_8 = 111110000000011_2$   
(c)  $10110111_2 = B7_{16}$     (d)  $67.24_8 = 110111.0101_2$   
(e)  $10100.1101_2 = 14.D_{16}$     (f)  $F3A5_{16} = 1111001110100101_2$   
(g)  $11011001_2 = 331_8$     (h)  $AB3D_{16} = 1010101100111101_2$   
(i)  $101111.0111_2 = 57.34_8$     (j)  $15C.38_{16} = 101011100.00111_2$

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- 4e2.2    2.2 (a)  $1234_8 = 1010011100_2 = 29C_{16}$   
(b)  $174637_8 = 111110011001111_2 = F99F_{16}$   
(c)  $365517_8 = 11110101101001111_2 = 1EB4F_{16}$   
(d)  $2535321_8 = 10101011101011010001_2 = ABAD1_{16}$   
(e)  $7436.11_8 = 111100011110.001001_2 = F1E.24_{16}$   
(f)  $45316.7414_8 = 100101011001110.111100001100_2 = 4ACE.F0C_{16}$

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- 3e2.3    2.3    (a)  $1023_{16} = 1000000100011_2 = 10043_8$   
(b)  $7E6A_{16} = 111111001101010_2 = 77152_8$   
(c)  $ABCD_{16} = 1010101111001101_2 = 125715_8$   
(d)  $C350_{16} = 1100001101010000_2 = 141520_8$   
(e)  $9E36.7A_{16} = 1001111000110110.0111101_2 = 117066.364_8$   
(f)  $DEAD.BEEF_{16} = 1101111010101101.101111011101111_2 = 157255.575674_8$

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4e2.4    2.4     $32107654321_8 = 11010001\ 00011111\ 01011000\ 11010001_2$   
 $= (011\ 010\ 001)\ (000\ 011\ 111)\ (001\ 011\ 000)\ (011\ 010\ 001)_2 = (321)\ (037)\ (130)\ (321)_8$

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- 3e2.5    2.5    (a)  $1101011_2 = 107_{10}$     (b)  $174003_8 = 63491_{10}$   
(c)  $10110111_2 = 183_{10}$     (d)  $67.24_8 = 55.3125_{10}$   
(e)  $10100.1101_2 = 20.8125_{10}$  (f)  $F3A5_{16} = 62373_{10}$   
(g)  $12010_3 = 138_{10}$     (h)  $AB3D_{16} = 43837_{10}$   
(i)  $7156_8 = 3694_{10}$     (j)  $15C.38_{16} = 348.21875_{10}$

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3e2.6

- |     |                             |                              |
|-----|-----------------------------|------------------------------|
| 2.6 | (a) $125_{10} = 1111101_2$  | (b) $3489_{10} = 6641_8$     |
|     | (c) $209_{10} = 11010001_2$ | (d) $9714_{10} = 22762_8$    |
|     | (e) $132_{10} = 1000100_2$  | (f) $23851_{10} = 5D2B_{16}$ |
|     | (g) $727_{10} = 10402_5$    | (h) $57190_{10} = DF66_{16}$ |
|     | (i) $1435_{10} = 2633_8$    | (j) $65113_{10} = FE59_{16}$ |

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4e2.7

2.7

(a)	100100	(b)	1011100
	110011		100111
+ 11010		+ 101010	
<hr/>		<hr/>	
1001101		1010001	

(c)	11111110	(d)	11000000
	11100011		1100110
+ 1011101		+ 1111001	
<hr/>		<hr/>	
101000000		11011111	

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4e2.8    2.8    (a)    110000    (b)    110000    (c)    00111000    (d)    1110010  
              110011                          100111                          11100011                          1100110  
              - 11010                          - 101010                          - 1011101                          - 1111001  
              011001                          111101                          10000110                          1101101

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4e2.9

2.9 (a) 1776      (b) 57734      (c) 252757      (d) 511042

$$\begin{array}{r} + 1432 \\ \hline 3430 \end{array}$$
$$\begin{array}{r} + 1066 \\ \hline 61022 \end{array}$$
$$\begin{array}{r} + 465521 \\ \hline 740500 \end{array}$$
$$\begin{array}{r} + 57647 \\ \hline 570711 \end{array}$$

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4e2.10    2.10 (a)    1776    (b)    4F1A5    (c)    F35B    (d)    1B90F

$$\begin{array}{r} + \quad 1432 \\ \hline 2BA8 \end{array}$$
$$\begin{array}{r} + \quad B8D5 \\ \hline 5AA7A \end{array}$$
$$\begin{array}{r} + \quad 27E6 \\ \hline 11B41 \end{array}$$
$$\begin{array}{r} + \quad C44E \\ \hline 27D5D \end{array}$$

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4e2.11 2.11

	decimal	+ 25	+ 120	+82	-42	-6	-111
signed-magnitude	00011001	01111000	01010010	10101010	10000110	11101111	
two's-complement	00011001	01111000	01010010	11010110	11111010	10010001	
one's-complement	00011001	01111000	01010010	11010101	11111001	10010000	

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<b>4e2.12</b>	<b>2.12</b>	(a)    11010100	(b)    10111111
		+ 11101011	+ 11011111
		<hr/>	
		10111111	10011110
		no	no
		(c)    01011101	(d)    01100001
		+ 00110001	+ 00011111
		<hr/>	
		10001110	10000000
		yes	yes

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3e2.13 2.13 d

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- 3e2.14 2.14 The number of parity bits is minimized by making the array as close as possible to square, so the number of parity bits is on the order of  $2\sqrt{n} + 1$ . The exact answer depends on the value of  $n$ , and will be either  $2\lceil \sqrt{n} \rceil$  (e.g., for  $10 \leq n \leq 12$  or  $2\lceil \sqrt{n} \rceil + 1$  (e.g., for  $13 \leq n \leq 16$ ).

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4e2.15 2.15 Christmas and Halloween, since Dec 25 = Oct 31.

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4e2.16 2.16 C0FFEE

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4e2.17 2.17 11000000 is the only one (-64).

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- 3e2.17 2.19 Assuming that the solution  $x = 8$  is correct in some base  $b > 8$ , we can write the following equation using base-10 arithmetic:

$$5 \cdot 8^2 + (5 \cdot b + 0) \cdot 8 + 1 \cdot b^2 + 2 \cdot b + 5 = 0$$

Solving the quadratic, we get  $b = 13$  or  $b = 25$ . Next, we try the  $x = 5$  solution for both possible bases, and find that it works only for  $b = 13$ ; the Martians had 13 fingers.

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3e2.18 2.20

$$h_j = \sum_{i=0} b_{4j+i} \cdot 2^i$$

Therefore,

$$\begin{aligned} B &= \sum_{i=0}^{4n-1} b_i \cdot 2^i = \sum_{i=0}^{n-1} h_i \cdot 16^i \\ -B &= 2^{4n} - \sum_{i=0}^{4n-1} b_i \cdot 2^i = 16^n - \sum_{i=0}^{n-1} h_i \cdot 16^i \end{aligned}$$

Suppose a  $3n$ -bit number  $B$  is represented by an  $n$ -digit octal number  $Q$ . Then the two's-complement of  $B$  is represented by the 8's-complement of  $Q$ .

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- 3e2.19 2.21 The result follows directly from Tables 2–1 and 2–3. For any 4-bit string  $B$  and corresponding hex digit  $H$ , the ones' complement of  $B$  is represented by the 15s' complement of  $H$ . Since the ones' complement is obtained by complementing individual bits, we can complement them in groups of four to arrive at the result.

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3e2.20 2.22 Cases 1 and 2 assume no overflow.

Case 1 ( $x, y \geq 0$ ):

$$\begin{aligned}[x+y] &= x+y \\ &= [x]+[y]\end{aligned}$$

$$\begin{aligned}[x+y] &= 2^n - (|x| + |y|) \\ &= 2^n + 2^n - (|x| + |y|) \text{ modulo } 2^n \\ &= (2^n - |x|) + (2^n - |y|) \\ &= [x]+[y]\end{aligned}$$

Case 2 ( $x, y < 0$ ):

$$\begin{aligned}[x+y] &= 0 \\ &= 2^n \text{ modulo } 2^n \\ &= (2^n - |x|) + |y| \\ &= [x]+[y]\end{aligned}$$

$$\begin{aligned}[x+y] &= 2^n - (|x| - |y|) \text{ (using signed-magnitude rules)} \\ \text{subcase 3b: } |x| > |y|, \text{ so } x+y < 0 &= (2^n - |x|) + |y| \\ &= [x]+[y]\end{aligned}$$

Case 4 ( $x \geq 0, y < 0$ ):  $|x| \geq |y|$ , so  $x+y \geq 0$

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**3e2.21 2.23** If  $x < 0$ , then  $[x] = 2^n - 1 - |x|$ . We want to show that  $[x + y] = [x] + [y]$  modulo  $2^n - 1$ .

Cases 1 and 2 assume no overflow.

Case 1 ( $x, y \geq 0$ ):

$$\begin{aligned}|x + y| &= x + y \\&= |x| + |y|\end{aligned}$$

$$[x + y] = x + y$$

$$= (2^n - 1 + 2^n - 1 - (|x| + |y|)) \text{ mod } 2^n - 1$$

Case 2 ( $x, y < 0$ ):

$$= ((2^n - 1 - |x|) + (2^n - 1 - |y|))$$

$$= x + y$$

Case 3 ( $x < 0, y \geq 0$ ):

$$\begin{aligned}[x] + |y| &= 0 \\&= 2^n - 1 \text{ modulo } 2^n - 1\end{aligned}$$

subcase 3a:  $|x| = |y|$ , so  $x + y = 0$

$$\begin{aligned}&= 2^n - 1 - |x| + |x| \\&= (2^n - 1 - |x|) + |y| \\&= [x] + [y]\end{aligned}$$

$$[x + y] = 2^n - 1 - (|x| - |y|) \text{ (using signed-magnitude rules)}$$

subcase 3b:  $|x| = |y|$ , so  $x + y < 0$

$$\begin{aligned}&= (2^n - 1 - |x|) + y \\&= x + y\end{aligned}$$

Case 4 ( $x \geq 0, y < 0$ ):  $|x| \geq |y|$ , so  $x + y \geq 0$

$$\begin{aligned}[x + y] &= |x| - |y| \text{ (using signed-magnitude rules)} \\&= |x| + 2^n - 1 - |y| \text{ modulo } 2^n - 1 \\&= [x] + [y]\end{aligned}$$

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- 3e2.22 2.24 Starting with the arrow pointing at any number, adding a positive number causes overflow if the arrow is advanced through the +7 to -8 transition. Adding a negative number to any number causes overflow if the arrow is not advanced through the +7 to -8 transition.

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3e2.23 2.25 Case 1 ( $X \geq 0$ ) trivial

Case 2  $X < 0$  Let  $x$  be the positive magnitude of  $X$ .

$$X(\text{m-bit}) = 2^m - x$$

$$n - 1$$

$$\begin{aligned} X(\text{n-bit}) &= 2^m - x + \sum_{i=m}^{n-1} 2^i \text{ (append 1s)} \\ &= 2^n - x \end{aligned}$$

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- 3e2.24 2.26 Let the binary representation of  $X$  be  $x_{n-1}x_{n-2}\dots x_1x_0$ . Then we can write the binary representation of  $Y$  as  $x_m x_{m-1} \dots x_1 x_0$ , where  $m = n - d$ . Note that  $x_{m-1}$  is the sign bit of  $Y$ . The value of  $Y$  is

$$Y = -2^{m-1} \cdot x_{m-1} + \sum_{i=0}^{n-2} x_i \cdot 2^i$$

The value of  $X$  is

$$\begin{aligned} X &= -2^{n-1} \cdot x_{n-1} + \sum_{i=0}^{n-2} x_i \cdot 2^i \\ &= -2^{n-1} \cdot x_{n-1} + Y + 2^{m-1} \cdot x_{m-1} + \sum_{i=m-1}^{n-2} x_i \cdot 2^i \\ &= -2^{n-1} \cdot x_{n-1} + Y + 2 \cdot 2^{m-1} + \sum_{i=0}^{n-2} x_i \cdot 2^i \end{aligned}$$

Case 1 ( $x_{m-1} = 0$ ) In this case,  $X = Y$  if and only if  $-2^{n-1} \cdot x_{n-1} + \sum_{i=m}^{n-2} x_i \cdot 2^i = 0$ , which is true if and only if all of the discarded bits ( $x_m \dots x_{n-1}$ ) are 0, the same as  $x_{m-1}$ .

Case 2 ( $x_{m-1} = 1$ ) In this case,  $X = Y$  if and only if  $-2^{n-1} \cdot x_{n-1} + 2 \cdot 2^{m-1} + \sum_{i=0}^{n-2} x_i \cdot 2^i = 0$ , which is true if and only if all of the discarded bits ( $x_m \dots x_{n-1}$ ) are 1, the same as  $x_{m-1}$ .

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- 3e2.25 2.27 If the radix point is considered to be just to the right of the leftmost bit, then the largest number is  $1.11\cdots 1$  and the 2's complement of  $D$  is obtained by subtracting it from 2 (singular possessive). Regardless of the position of the radix point, the 1s' complement is obtained by subtracting  $D$  from the largest number, which has all 1s (plural).

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- 3e2.26 2.28 For the first part, note that the bit-by-bit complement of  $Y$  may be written  $\bar{Y} = 2^n - 1 - Y$ . Therefore,  $Y = 2^n - 1 - \bar{Y}$  and

$$\begin{aligned} X - Y &= X - (2^n - 1 - \bar{Y}) \\ &= X + (-2^n + 1 + \bar{Y}) \\ &= (X + \bar{Y} + 1 - 2^n) \end{aligned}$$

Next, consider the behavior of an  $n$ -bit adder for the operation  $X + \bar{Y} + 1 - 2^n$ . Suppose that no carry is produced:

$$\begin{aligned} \text{no carry} &\Rightarrow X + \bar{Y} + 1 < 2^n \\ &\Rightarrow X < 2^n - 1 - \bar{Y} \\ &\Rightarrow X < \bar{Y} \\ &\Rightarrow X - \bar{Y} < 0 \\ &\Rightarrow \text{subtraction produces a borrow} \end{aligned}$$

Likewise, we can show

$$\begin{aligned} \text{carry} &\Rightarrow X + \bar{Y} + 1 \geq 2^n \\ &\Rightarrow X \geq 2^n - 1 - \bar{Y} \\ &\Rightarrow X \geq Y \\ &\Rightarrow X - Y \geq 0 \\ &\Rightarrow \text{subtraction does not produce a borrow} \end{aligned}$$

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- 3e2.27 2.29 All  $2n$  bits are needed to represent the product of the most negative number ( $-2^{n-1}$ ) times itself:  
 $-2^{n-1} \cdot -2^{n-1} = 2^{2n-1} = 01000\dots000$ .

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3e2.28 2.30

$$\begin{aligned} B &= -b_{n-1} \cdot 2^{n-1} + \sum_{\substack{i=0 \\ n-2}} b_i \cdot 2^i \\ 2B &= -b_{n-1} \cdot 2^n + \sum_{\substack{i=0 \\ n-1}} b_i \cdot 2^{i+1} \end{aligned}$$

Case 1 ( $b_{n-1} = 0$ ) First term is 0, summation terms have shifted coefficients as specified. Overflow if  $b_{n-2} = 1$ .

Case 2 ( $b_{n-1} = 1$ ) Split first term into two halves; one half is cancelled by summation term  $b_{n-2} \cdot 2^{n-1}$  if  $b_{n-2} = 1$ . Remaining half and remaining summation terms have shifted coefficients as specified. Overflow if  $b_{n-2} = 0$ .

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- 3e2.29 2.31 To multiply a ones'-complement number by two, shift it one bit position to the left, with end-around carry from the most significant bit position. The operation overflows if  $b_{n-1}$  and  $b_{n-2}$  have opposite values at the start of the operation.

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- 4e2.32 2.32 BCD Subtraction Rule: Subtract the 4-bit binary numbers using binary arithmetic. If there was a borrow, subtract 6 from the result and record a BCD borrow. Examples:

$$\begin{array}{r} 8 & 1000 & 4 & 0100 & 5 & 0101 & 2 & 0010 \\ -3 & -0011 & -8 & -1000 & -9 & -1001 & -7 & -0111 \\ \hline 5 & 0101 & 12 & 1100, B & 12 & 1100, B & 11 & 1011, B \\ & & -6 & -0110 & -6 & -0110 & -6 & -0110 \\ \hline & & 0110, B & & 0110, B & & 5, B & 0101, B \\ & & & & & & & \end{array}$$

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- 4e2.33 2.33 With five states and eight possible 3-bit encodings, there are  $\binom{8}{5}$  ways to choose the encodings, and  $5!$  ways to assign encodings to states for each choice. Thus, the total is

$$\binom{8}{5} \cdot 5! = \frac{8!}{5! \cdot 3!} \cdot 5! = 8!/6 = 6720$$

For seven states and eight possible 3-bit encodings, there are  $\binom{8}{7}$  ways to choose the encodings, and  $7!$  ways to assign encodings to states for each choice. Thus, the total is

$$\binom{8}{7} \cdot 7! = \frac{8!}{7! \cdot 1!} \cdot 7! = 8!/1 = 40320$$

For eight states and eight possible 3-bit encodings, there is just one way to choose the encodings. Thus, the total is  $8!$  or 40320. This is the same answer as with seven states, because with each 7-state encoding, there is exactly one leftover state which would be the eighth state in a corresponding 8-state encoding.

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- 4e2.34 2.34 Basically, your boss has forbidden the 111 encoding. Since there are 6 states and now only seven allowed 3-bit encodings, there are  $\binom{7}{6}$  ways to choose the encodings, and  $6!$  ways to assign encodings to states for each choice. Thus, the total is

$$\binom{7}{6} \cdot 6! = \frac{7!}{6! \cdot 1!} \cdot 6! = 7!/1 = 5040$$

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4e2.33 2.35 001–010, 011–100, 101–110, 111–000.

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- 3e2.33 2.36 When the LSB changes from 0 to 1, there's no problem. When the LSB changes from 1 to 0, so does the next bit (and possibly others), guaranteeing a problem. So, half the boundaries are bad, a total of  $2^{n-1}$  for an  $n$ -bit encoding disc.

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- 4e2.37 2.37 The manufacturer's code fails every 4th time, for a total of  $2^{n-2}$  for an  $n$ -bit encoding disc. A standard binary code fails when the LSB changes from 1 to 0, which changes the next bit (and possibly others), guaranteeing a problem. So, half the boundaries in a standard binary code are bad, a total of  $2^{n-1}$  for an  $n$ -bit encoding disc. The manufacturer's code is only half as bad as a standard binary code.

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- 3e2.34 2.38 Perhaps the designers were worried about what would happen if the aircraft changed altitude in the middle of a transmission. With the Gray code, the codings of “adjacent” altitudes (at 50-foot increments) differ in only one bit. An altitude change during transmission affects only one bit, and whether the changed bit or the original is transmitted, the resulting code represents an altitude within one step (50 feet) of the original. With a binary code, larger altitude errors could result, say if a plane changed from 12,800 feet ( $00010000000_2$ ) to 12,750 feet ( $00001111111_2$ ) in the middle of a transmission, possibly yielding a result of 25,500 feet ( $00011111111_2$ ).

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- 3e2.35 2.39 If a pair of bits (H,L) represents the states of the high and low filaments in the bulb, a normal switch cycles through the sequence (0,0)–(0,1)–(1,0)–(1,1)–(0,0), yielding the lighting sequence OFF–DIM–MEDIUM–BRIGHT–OFF. According to the binary sequence, the low filament is stressed twice during each complete cycle. Less stress would occur if the switch used a Gray-code sequence, (0,0)–(0,1)–(1,1)–(1,0)–(0,0), yielding the lighting sequence OFF–DIM–BRIGHT–MEDIUM–OFF.

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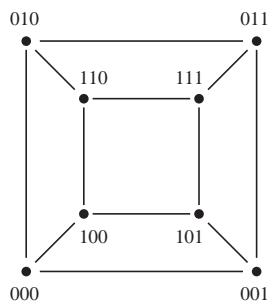
- 3e2.36 2.40 In the string representation, each position may have a 0, a 1, or an  $x$ , a total of three possibilities per position, and  $3^n$  combinations in all.

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3e2.37

2.41



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3e2.38    2.42 It can't be done, but it probably takes a topologist to prove it.

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- 3e2.39 2.43 Think of it in terms of the string notation for subcubes. There are  $\binom{n}{m}$  ways to pick the  $m$  positions that contain 0s and 1s, and  $2^m$  ways to assign 0s and 1s to a particular set of  $m$  positions. So the total is  $\binom{n}{m} \cdot 2^m$ .

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3e2.40 2.44 A possible Hamming matrix is .

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 0 & 1 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 0 \end{bmatrix}$$

The first eleven columns correspond to information bits, and the last four to parity bits.

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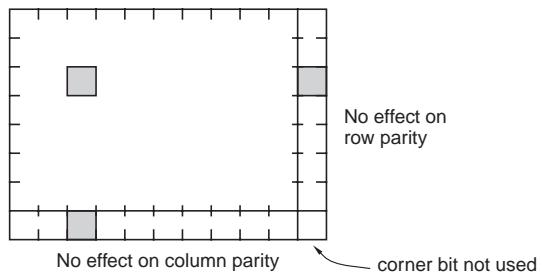
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3e2.41 2.45 000, 111

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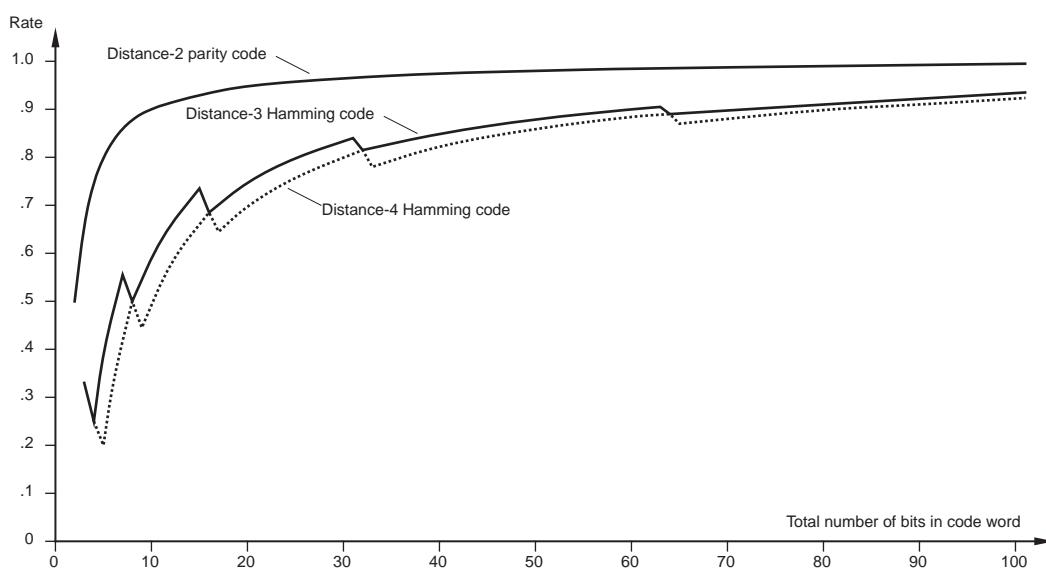
3e2.42 2.46



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3e2.43 2.47



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3e2.44 2.48

Minimum-distance-4 Hamming codes				
Information bits	Parity bits	Total bits	Rate	
1	3	3	.25	
$\leq 4$	4	$\leq 8$	.2-.5	
$\leq 11$	5	$\leq 16$	.4444–.6875	
$\leq 26$	6	$\leq 32$	.6471–.8125	
$\leq 57$	7	$\leq 64$	.7879–.8906	
$\leq 120$	8	$\leq 128$	.8769–.9375	

Minimum-distance-4 two-dimensional codes					
Information matrix	Information bits	Parity bits	Total Bits	Rate	
$1 \times 1$	1	3	4	.25	
$1 \times 2$	2	4	6	.3333	
$2 \times 2$	3–4	5	8–9	.3750–.4444	
$2 \times 3$	5–6	6	11–12	.4545–.5000	
$3 \times 3$	7–9	7	14–16	.5000–.5625	
$3 \times 4$	10–12	8	18–20	.5556–.6000	
$4 \times 4$	13–16	9	22–25	.5909–.6400	
$4 \times 5$	17–20	10	27–30	.6296–.6667	
$5 \times 5$	21–25	11	32–36	.6563–.6944	
$5 \times 6$	26–30	12	38–42	.6842–.7143	
$6 \times 6$	31–36	13	44–49	.7045–.7347	
$6 \times 7$	37–42	14	51–56	.7255–.7500	
$7 \times 7$	43–49	15	58–64	.7414–.7656	
$7 \times 8$	50–56	16	66–72	.7576–.7778	
$8 \times 8$	57–64	17	74–81	.7703–.7901	
$8 \times 9$	65–72	18	83–90	.7831–.8000	
$9 \times 9$	73–81	19	92–100	.7935–.8100	
$9 \times 10$	82–90	20	102–110	.8039–.8182	
$10 \times 10$	91–100	21	112–121	.8125–.8264	

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- 3e2.45 2.49 To get a minimum distance of 6, we make a two-dimensional code using a distance-3 Hamming code for the rows and a distance-2 even-parity check for the columns. Three possible two-dimensional matrices with a total of four information bits are summarized below.

Row data bits	Row check bits	Column data bits	Column check bits	Matrix size (rows $\times$ columns)	Total bits
4	3	1	1	$2 \times 7$	14
2	3	2	1	$3 \times 5$	15
1	2	4	1	$5 \times 3$	15

To obtain the minimum number of bits in a code word, we select the first case. The row code is a 7-bit Hamming code with four information bits and three check bits. Such a code is given in the first two columns of Table 1–14 in the text. The column code is an even-parity check with one information bit and one check bit, which is equivalent to duplicating the information bit. Thus, the two rows of each 14-bit two-dimensional code word are simply duplicates of a 7-bit code word from Table 1–14.

If the third case is selected, we get a code that is even easier to construct, though it has one more bit, a total of 15. The first column contains four information bits and an even-parity check bit. The second and third columns are copies of the first column.

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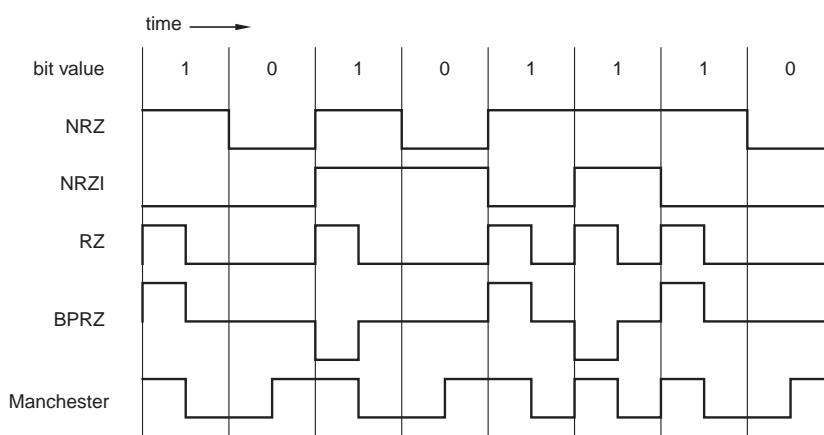
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- 3e2.46 2.50 Read the old data in block  $b$  on drive  $d$ , and in block  $b$  on drive  $n+1$  (the check drive). XOR the two blocks just read with the new data and store in block  $b$  on drive  $n+1$ . Store the new data in block  $b$ , drive  $d$ .

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3e2.47 2.51



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G3.201 3.1 The “probably” cases may cause damage to the gate if sustained.

- (a) 0
- (b) 0
- (c) 1
- (d) probably 0
- (e) undefined
- (f) probably 0
- (g) 1
- (h) probably 1

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G3.202 3.2 The “probably” cases may cause damage to the gate if sustained.

- (a) 1
- (b) 1
- (c) 0
- (d) probably 1
- (e) undefined
- (f) probably 1
- (g) 0
- (h) probably 0

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- 3e3.3 3.3 A logic buffer is a non-linear amplifier that maps the entire set of possible analog input voltages into just two output voltages, HIGH and LOW. An audio amplifier has a linear response over its specified operating range, mapping each input voltage into an output voltage that is directly proportional to the input voltage.

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3e3.4 3.4 Yes, both.

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- G3.205 3.5 False. The outputs are the same, since an OR gate with inverted inputs is the same as a NAND gate.

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- 3e3.6 3.6 From the *American Heritage Electronic Dictionary (AHED)*, copyright 1992 by Houghton Mifflin Company:
- (1) A structure that can be swung, drawn, or lowered to block an entrance or a passageway.
  - (2) a. An opening in a wall or fence for entrance or exit. b. The structure surrounding such an opening, such as the monumental or fortified entrance to a palace or walled city.
  - (3) a. A means of access: the gate to riches. b. A passageway, as in an airport terminal, through which passengers proceed for embarkation.
  - (4) A mountain pass.
  - (5) The total paid attendance or admission receipts at a public event: a good gate at the football game.
  - (6) A device for controlling the passage of water or gas through a dam or conduit.
  - (7) The channel through which molten metal flows into a shaped cavity of a mold.
  - (8) Sports. A passage between two upright poles through which a skier must go in a slalom race.
  - (9) Electronics. A circuit with multiple inputs and one output that is energized only when a designated set of input pulses is received.

Well, definition (9) is closest to one of the answers that I had in mind. The other answer I was looking for is the gate of a MOS transistor.

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- G3.207 3.7 A CMOS NAND gate uses four transistors: two *p*-channel transistors and two *n*-channel transistors.

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- G3.208 3.8 The NAND gate has 2 inputs, A and B, and output Z. Connect gate input A to the coil of Relay 1 and gate input B to the coil of Relay 2. Tie the other side of each coil to ground. Tie both normally-closed contacts to  $V_{CC}$  and the normally-open contact of Relay 1 to ground. Tie the “common” contact of Relay 1 to the normally-open contact of Relay 2. The “common” contact of Relay 2 is the gate output Z. Of course, this circuit is not really “equivalent” to the CMOS NAND gate, since the relay coils draws a lot more current than the gate terminals of MOS transistors.

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3e3.9 3.9 A NAND gate, according to the box on page 92.

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- 3e3.10 3.10 See definitions on pp. 92, 97, and 111. You're much more likely to calculate fanout. Fan-in is a concern only to the circuit designer of a gate

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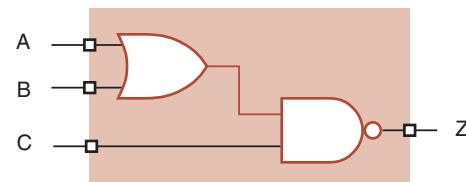
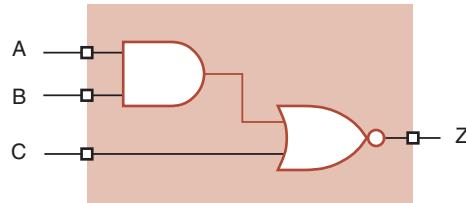
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3e3.14 3.16 A CMOS inverting gate has fewer transistors than a noninverting one, since an inversion comes “for free.”

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- G3.215 3.17 Simple, inverting CMOS gates generally have two transistors per input. Four types that meet the requirements of the problem are 3-input NAND, 3-input NOR, 3-input AND-OR-INVERT, and 3-input OR-AND-INVERT. Logic symbols for the last two types are shown below.



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- 3e3.18 3.19 One way is that a romance could be sparked, and the designers could end up with a lot less time to do their work. Another way is that the stray perfume in the IC production line could have contaminated the circuits used by the designers, leading to marginal operation, more debugging time by the dedicated designers, and less time for romance. By the way, the whole perfume story may be apocryphal.

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- 3e3.20 3.20 Using the maximum output current ratings in both states, the HIGH-state margin is 0.69V and the LOW-state margin is 1.02V. With CMOS loads (output currents less than 20  $\mu$ A), the margins improve to 1.349V and 1.25V, respectively.

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G3.219 3.21 High-state noise margin looks like about 1.2V (4.7V - 3.5V). Low-state margin is about 1.0V (1.5V - 0.5V).

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- 3e3.21 3.22 The first answer for each parameter below assumes commercial operation and that the device is used with the maximum allowable (TTL) load. The number in parentheses, if any, indicates the value obtained under a lesser but specified (CMOS) load.

$$V_{OH\min} \quad 3.84V \text{ (4.4V)}$$

$$V_{IH\min} \quad 3.15V$$

$$V_{IL\max} \quad 1.35V$$

$$V_{OL\max} \quad 0.33V \text{ (0.1V)}$$

$$I_{Imax} \quad 1\mu A$$

$$I_{OL\max} \quad 4 mA \text{ (20 } \mu A)$$

$$I_{OH\max} \quad -4 mA \text{ (-20 } \mu A)$$

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3e3.22 3.23 Current is positive if it flows *into* a node. Therefore, an output with negative current is *sourcing* current.

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- 3e3.24 3.24 (Note typo in the first printing; change “2.0–5.0 V” to “3.15–5.0 V.”) The specification for the 74HC00 shows a maximum power-supply current of 10  $\mu\text{A}$  when the inputs are at 0 or 5V, but based on the discussion in Section 3.5.3 we would expect the current to be more when the inputs are at their worst-case values (1.35 or 3.15V). If we consider “nonlogic” input values, the maximum current will flow if the inputs are held right at the switching threshold, approximately  $V_{CC}/2$ .

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- G3.225 3.25 For the 74HC00,  $I_{OHmax} = 4mA$ , while for the 74ALS00,  $I_{ILmax} = -0.2mA$ . Therefore, the LOW-state fanout is 20. For the 74HC00,  $I_{OHmax} = -4mA$ , while for the 74ALS00,  $I_{IHmax} = 0.02mA$ . Therefore, the HIGH-state fanout is 200. The overall fanout is the minimum of these two numbers, or 20.

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- 3e3.26 3.26 Using the formulas on page 120, we can estimate that  $R_{p(on)} = (5.0 - 3.84)/0.004 = 290\Omega$  or, using the higher value of  $V_{OHmin}$  in the spec, that  $R_{p(on)} = (5.0 - 4.4)/0.00002 = 30K\Omega$ . (The discrepancy shows that the output characteristic of this device is somewhat nonlinear.) We can also estimate  $R_{n(on)} = 0.33/0.004 = 82.5\Omega$ .

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G3.223 3.27 The 74HC00 output drive is so weak, it's not good for driving much:

- (a) Assume that in the LOW state the output pulls down to 0.33 V (the maximum  $V_{OL}$  spec). Then the output current is  $(5.0V - 0.33V)/120\Omega = 38.9\text{mA}$ , which is way more than the 4-mA commercial spec.
- (b) For this problem, you first have to find the Thévenin equivalent of the load, or  $148.5\Omega$  in series with 2.75 V. In the HIGH state, the gate must pull the output up to 3.84 V, a difference of 1.09 V across  $148.5\Omega$ , requiring 7.3 mA, which is out of spec. In the LOW state, we have a voltage drop of  $2.75V - 0.33V$  across  $148.5\Omega$ , so the output must sink 16.3 mA, again out of spec.
- (c) The output must source enough current to create a 3.84-V drop across an  $820\Omega$  resistor, or 4.7 mA. This is out of spec.
- (d) The Thévenin equivalent is  $235\Omega$  in series with 2.5 V. In the HIGH state, the gate must pull the output up to 3.84 V, a difference of 1.34 V across  $235\Omega$ , requiring 5.7 mA, which is out of spec. In the LOW state, we need a 2.17-V drop across  $235\Omega$ , or 9.2 mA, which is also way out of spec.
- (e) The HIGH state is no problem, because the resistor pulls the output up to 5 V on its own. In the LOW state, we need a 4.67-V drop across  $1000\Omega$ , or 4.7 mA, which is within spec.
- (f) The Thévenin equivalent is  $487\Omega$  in series with 2.03 V. In the HIGH state, the gate must pull the output up to 3.84 V, a difference of 1.81 V across  $487\Omega$ , requiring 3.7 mA, which is within spec. In the LOW state, we need a 1.7-V drop across  $487\Omega$ , or 3.5 mA, which is also within spec.
- (g) The HIGH state is no problem, because the resistor pulls the output up to 5 V on its own. In the LOW state, we need a 4.67-V drop across  $4700\Omega$ , or about 1.0 mA, which is within spec.

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3e3.27 3.28 Generally, never. However, some devices have internal pull-ups, and can therefore be allowed to “float.”

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- 3e3.28 3.29 See pages 113–114. In practice, CMOS device latch-up is most often caused by applying to an input a voltage that is more than a diode-drop higher than the power-supply voltage, typically in a situation where inputs are active but the power supply hasn't been turned on (or hasn't "ramped up") yet. This triggers a "parasitic SCR" which is part of the CMOS device's physical structure, which creates a low-impedance path between the device's power and ground terminals, even after the triggering condition is removed.

Modern CMOS devices, though still susceptible to latch up, have been somewhat "hardened" by including structures that prevent the SCR from triggering unless the higher-voltage input source is able to source *lots* of current. For example, quoting from Integrated Device Technology's 1992 *High-Performance Logic* databook,

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes. The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are used on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents from 10–20 mA, IDT products inhibit latchup at trigger currents substantially greater than this.

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- G3.229 3.30 The purpose of decoupling capacitors is to provide the instantaneous power-supply current that is required during output transitions. Capacitors have stray inductance, which acts as a barrier to current flow at high frequencies (fast transition rates). The large physical structures of large capacitors (such as power-supply filter capacitors) typically have more stray inductance than smaller capacitors, so they may actually be less effective at supplying current quickly at high frequencies.

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- 3e3.30 3.31 Before handing over a CMOS device. If you are different potentials, you may damage the device.  
By the way, it takes about 5–6 kV of potential difference to generate a static spark big enough to feel, but most devices are rated to survive only about 2 kV without damage. So even if you don't feel the static, you may be damaging devices.

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- 3e3.31 3.32 Propagation delay and transition time. If the sizes of the internal transistors are properly balanced, propagation delay tends to be about the same regardless of the transition direction. The same is true for transition time. Note that *p*-channel transistors have to be about twice the size of corresponding *n*-channel transistors to achieve the same low resistance. If the *p*-channel transistors are “undersized,” then LOW-to-HIGH transitions will tend to longer than HIGH-to-LOW ones, because the load capacitance must charge through a higher resistance.

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G3.232 3.33 (a) 5 ns; (b) 705 ns; (c) 2.2 ns; (d) 100 ns.

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- G3.233 3.34 A 5% increase in power-supply voltage has a bigger effect than the same percentage increase in internal and load capacitance, since power consumption is proportional to the square of the voltage ( $CV^2f$ ) .

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- G3.234 3.35 CMOS inputs have very low input-current requirements, typically less than a microampere of leakage current. Thus, a CMOS output with 4 mA of driving capability could theoretically drive 4000 CMOS inputs. Having this number of inputs connected to a single output is rare, except in clock-driving applications in large chips. And even in this case, a single output is unlikely to drive that many inputs, because the high capacitive load of 4000 inputs would slow down the transition times too much. Slow transition times cause uncertainty in when the transition is actually detected by different inputs, and also increases power consumption in the input structures of the driven inputs.

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- G3.235 3.36 The answer depends on operating frequency  $f$ . If  $f = 0$  and leakage (quiescent) current remains unchanged, then the 2.5-V power consumption is  $2.5/5 = 66\%$  of the 5-V power consumption. If  $f$  is large enough that most of the current is attributable to  $CV^2f$  power consumption, then the 2.5-V power consumption is  $(2.5/5)^2 = 25\%$  of the 5-V power consumption. In practice, the answer lies somewhere in between, but 25% is an often-used rule of thumb.

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G3.236 3.37 Hysteresis depends only on the difference in threshold voltages, and is 0.5 V in this case.

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- G3.237 3.38 If the output enables were changed at the same time, then the output being enabled would start driving before the other output was disabled. This would result in the bus being driven by both gates for an instant every time the output enables were switched. (Also see Section 6.6).

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- 3e3.38 3.39 Smaller resistors result in shorter rise times for LOW-to-HIGH transitions but higher power consumption in the LOW state. Stated another way, larger resistors result in lower power consumption in the LOW state but longer rise times (more ooze) for LOW -to-HIGH transitions.

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- 3e3.39    3.40 The resistor must drop  $5.0 - 2.0 - 0.37 = 2.63\text{V}$  with  $5\text{mA}$  of current through it. Therefore  $r = 2.63/0.005 = 526\Omega$ ; a good standard value would be  $510\Omega$ .

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- G3.240 3.41 For the 74HC CMOS family,  $V_{OHmin}$  is 3.8 V. So the resistor must drop  $3.8 - 2.0 = 1.8V$  with 2mA of current through it. Therefore  $r = 1.8/0.002 = 900\Omega$ ; a good standard value would be  $910\Omega$ .

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- 3e3.41    3.42 The wired output has only passive pull-up to the HIGH state. Therefore, the time for LOW-to-HIGH transitions, an important component of total delay, depends on the amount of capacitive loading and the size of the pull-up resistor. A moderate capacitive load (say, 100 pF) and even a very strong pull-up resistor (say,  $150\Omega$ ) can still lead to time constants and transition times (15 ns in this example) that are longer than the delay of an additional gate with active pull-up.

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- 3e3.42 3.43 The winner is 74FCT-T—48 mA in the LOW state and 15 mA in the HIGH state (see Table 3–8). TTL families don't come close.

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- G3.243 3.44 The “T” suffix indicates that gate inputs are guaranteed recognize TTL input levels. The absence of a “T” indicates that inputs require CMOS levels. The output characteristics of the ACT family are stronger; it can drive 24mA while the HC family can only drive 4mA. Finally, the precocious student may note that ACT is a lot faster.

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- 3e3.44 3.45 FCT devices are not targeted to be interfaced with pure CMOS loads. Anyway, in cases where they are used with pure CMOS loads, their outputs are so strong that they easily meet the CMOS input requirements, except for FCT-T, which may have a reduced  $V_{OH}$ .

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3e3.45 3.46 The typical output HIGH level is about a volt less, which reduces  $CV^2f$  power consumption.

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3e3.46 3.47  $n$  diodes are required.

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3e3.48 3.48 TTL outputs, as well as TTL-compatible CMOS outputs, are more capable of sinking current than sourcing it.

- G3.249 3.49 For each interfacing situation, we compute the fanout in the LOW state by dividing  $I_{OLmax}$  of the driving gate by  $I_{ILmax}$  of the driven gate. Similarly, the fanout in the HIGH state is computed by dividing  $I_{OLmax}$  of the driving gate by  $I_{IHmax}$  of the driven gate. The overall fanout is the lower of these two results.

Case	Low-state		High-state		Overall Fanout	Excess	
	Ratio	Fanout	Ratio	Fanout		State	Drive
74LS driving 74AS	$\frac{8mA}{0.5mA}$	16	$\frac{400\mu A}{20\mu A}$	20	16	HIGH	80μA
74LS driving 74F	$\frac{8mA}{0.6mA}$	13	$\frac{400\mu A}{20\mu A}$	20	13	HIGH	140μA
74F driving 74LS	$\frac{20mA}{0.4mA}$	50	$\frac{1000\mu A}{20\mu A}$	50	50	none	
74F driving 74AS	$\frac{20mA}{0.5mA}$	40	$\frac{1000\mu A}{20\mu A}$	50	40	HIGH	200μA
74AS driving 74S	$\frac{20mA}{2mA}$	10	$\frac{2000\mu A}{50\mu A}$	40	10	HIGH	1500μA
74S driving 74ALS	$\frac{20mA}{0.2mA}$	100	$\frac{1000\mu A}{20\mu A}$	50	50	LOW	10mA
74ALS driving 74S	$\frac{8mA}{2mA}$	4	$\frac{400\mu A}{50\mu A}$	8	4	HIGH	200μA
74F driving 74F	$\frac{20mA}{0.6mA}$	33	$\frac{1000\mu A}{20\mu A}$	50	33	HIGH	340μA
74S driving 74S	$\frac{20mA}{2mA}$	10	$\frac{1000\mu A}{50\mu A}$	20	10	HIGH	500μA
74S driving 74F	$\frac{20mA}{0.6mA}$	33	$\frac{1000\mu A}{20\mu A}$	50	33	HIGH	340μA
74F driving 74ALS	$\frac{20mA}{0.2mA}$	100	$\frac{1000\mu A}{20\mu A}$	50	50	LOW	10mA
74AS driving 74LS	$\frac{20mA}{0.4mA}$	50	$\frac{2000\mu A}{20\mu A}$	100	50	HIGH	1000μA

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- 3e3.50 3.50 For the pull-down, we must have at most a 0.5-V drop in order to create a  $V_{IL}$  that is no worse than a standard LS-TTL output driving the input. Since  $I_{ILmax} = 0.4\text{mA}$ , we get  $R_{pd} = 0.5/0.004 = 1250\Omega$  and  $P_{pd} = V_{IL}^2/R_{pd} = (0.5)^2/1250 = 0.2\text{mW}$ . (Alternatively,  $P_{pd} = V_{IL}I_{IL} = 0.5 \cdot 0.0004 = 0.2\text{mW}$ )

For the pull-up, we must have at most a 2.3-V drop in order to create a  $V_{IH}$  that is no worse than a standard LS-TTL output driving the input. Since  $I_{IHmax} = 20\mu\text{A}$ , we get  $R_{pu} = 2.3/0.00002 = 115\text{k}\Omega$  and  $P_{pu} = V_{IH}^2/R_{pu} = (2.3)^2/115000 = 0.046\text{mW}$ . (Alternatively, we could have calculated the result as  $P_{pu} = V_{IH}I_{IH} = 2.3 \cdot 0.00002 = 0.046\text{mW}$ .) The pull-up dissipates less power.

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- G3.251 3.51 The AND-OR-INVERT gate should be faster since it uses only one level of logic in its transistor logic circuit. The AND gate contains an extra level of logic, since it is built as a NAND gate followed by an inverter. This assumes that both types of gates have transistors that switch at the same speed.

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- 3e3.52 3.52 The main benefit of Schottky diodes is to prevent transistors from saturating, which allows them to switch more quickly. The main drawback is that they raise the collector-to-emitter drop across an almost-saturated transistor, which decreases LOW-state noise margin.

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- J3.253 3.53 Assuming  $I_{OL} = 8\text{mA}$ , the worst-case LOW-state noise margin is 0.3V. Assuming  $I_{OL} = 4\text{mA}$ , the worst-case LOW-state noise margin is 0.4V. The worst-case HIGH-state noise margin in any case is 0.5V (at the minimum power-supply voltage).

For the 54ALS00, the worst-case LOW-state noise margin is 0.3V over the full military temperature range, and the worst-case HIGH-state noise margin is also 0.5V.

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G3.254 3.54  $V_{OHmin} = 2.5V$ ,  $V_{IHmin} = 2.0V$ ,  $V_{ILmax} = 0.8V$ ,  $V_{OLmax} = 0.5V(0.4V)$ ,  $I_{ILmax} = -0.1mA$ ,  
 $I_{IHmax} = 20 \mu A$ ,  $I_{OLmax} = 8mA$  (4 mA),  $I_{OHmax} = -0.4mA$ .

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G3.255 3.55

$R_{VCC}$ ( $\Omega$ )	$R_{GND}$ ( $\Omega$ )	$V_{Thev}$ (V)	$R_{Thev}$ ( $\Omega$ )	LOW-state			HIGH-state		
				$V_{Thev} - V_{OL}$ (V)	$I_{OL}$ (mA)	OK?	$V_{OH} - V_{Thev}$ (V)	$I_{OH}$ ( $\mu A$ )	OK?
470	—	5.0	470	4.5	9.57	no	<0	—	yes
330	470	2.94	193.9	2.44	12.57	no	<0	—	yes
—	6.8K	0	6.8K	<0	—	yes	2.7	397	yes
910	1200	2.84	518	2.34	4.53	yes	<0	—	yes
620	—	5.0	620	4.5	7.26	yes	<0	—	yes
510	470	2.4	245	1.9	7.76	yes	0.3	1235	no
—	5.1K	0	5.1K	<0	—	yes	2.7	529	no
464	510	2.62	243	2.12	8.72	no	0.08	337	yes

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G3.256 3.56

Case	LOW-state			HIGH-state		
	$V_{ILmax}$	$V_{OLmax(T)}$	Margin	$V_{IHmin}$	$V_{OHmin(T)}$	Margin
74HCT driving 74LS	0.8V	0.33V	0.47V	2.0V	3.84V	1.84V
74ALS driving 74HCT	0.8V	0.5V	0.3V	2.0V	2.7V	0.7V
74AS driving 74VHCT	0.8V	0.5V	0.3V	2.0V	2.7V	0.7V
74VHCT driving 74F	0.8V	0.44V	0.47V	2.0V	3.80V	1.80V

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- G3.257 3.57 For each interfacing situation, we compute the fanout in the LOW state by dividing  $I_{OLmax}$  of the driving gate by  $I_{ILmax}$  of the driven gate. Similarly, the fanout in the HIGH state is computed by dividing  $I_{OHmax}$  of the driving gate by  $I_{ILmax}$  of the driven gate. The overall fanout is the lower of these two results.

Case	LOW-state		HIGH-state		Overall Fanout	Excess	
	Ratio	Fanout	Ratio	Fanout		State	Drive
74HCT driving 74LS	$\frac{4\text{mA}}{0.4\text{mA}}$	10	$\frac{4000\text{\mu A}}{20\text{\mu A}}$	200	10	HIGH	3800 $\mu\text{A}$
74VHCT driving 74S	$\frac{8\text{mA}}{2\text{mA}}$	4	$\frac{8000\text{\mu A}}{50\text{\mu A}}$	160	4	HIGH	7800 $\mu\text{A}$
74VHCT driving 74ALS	$\frac{8\text{mA}}{0.2\text{mA}}$	40	$\frac{8000\text{\mu A}}{20\text{\mu A}}$	400	40	HIGH	7200 $\mu\text{A}$
74HCT driving 74AS	$\frac{4\text{mA}}{0.5\text{mA}}$	8	$\frac{4000\text{\mu A}}{20\text{\mu A}}$	200	8	HIGH	3840 $\mu\text{A}$

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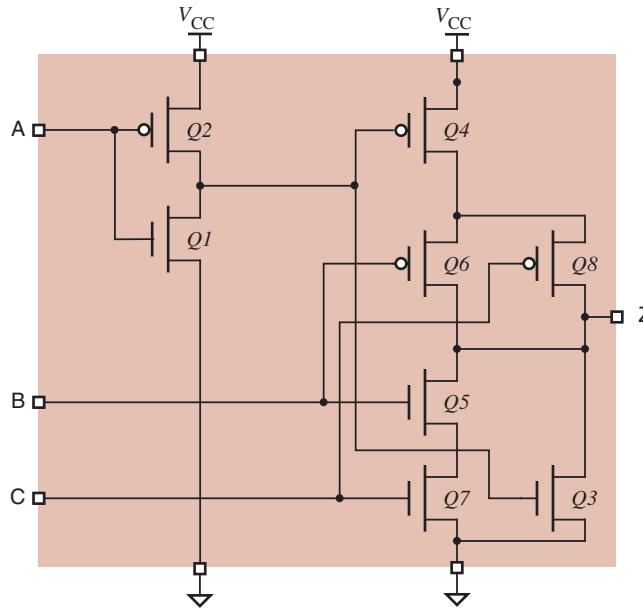
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- 3e3.58 3.58 CMOS has the widest voltage swing and therefore the highest dynamic power dissipation. It goes from 0.1V to 4.4 V, for a total swing of 4.3 V. An ECL output swings between -0.81 and -1.85, for a difference of only 1.04 V. The difference in power dissipation for a given capacitance and frequency is then the ratio of  $CV_{\text{CMOS}}^2 f$  to  $CV_{\text{ECL}}^2 f$ , or  $V_{\text{CMOS}}^2 / V_{\text{ECL}}^2$ . Plugging in the numbers tells us the dynamic power dissipation of CMOS is 17.1 times greater than ECL.

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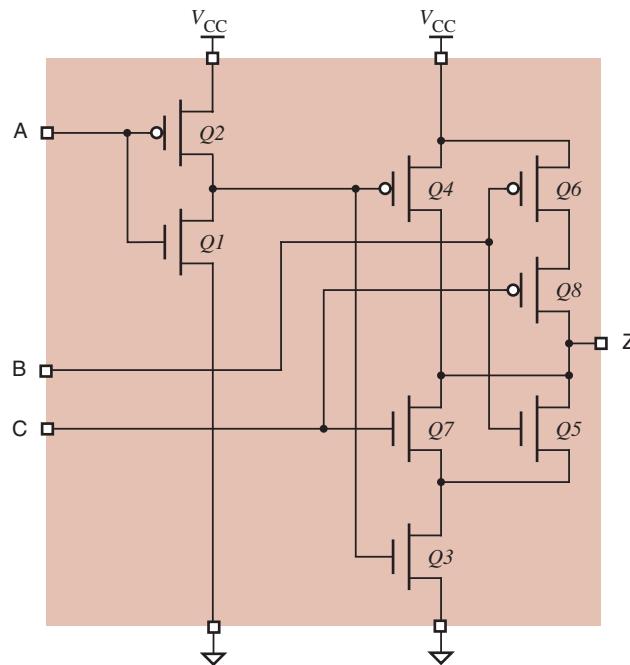
G3.259 3.59 The circuit shown below is a subset of the circuit in Figure 3–20(a) with an inverter on input A.



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**G3 . 260** 3.60 The circuit shown below is a subset of the circuit in Figure 3–22(a) with an inverter on input A.

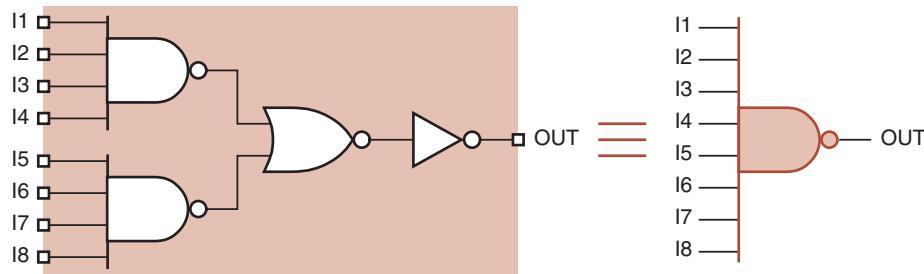


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- G3.263 3.63 Use two 4-input NAND gates on the first level, followed by a 2-input NOR, followed by an inverter, as in the figure below. This is most provides the best speed, because CMOS NOR gates are inherently slow because of the series connection of *p*-channel devices, and the 2-input NOR has the smallest number of these in series.

Designing the 8-input NAND as four 2-input NAND gates, followed by a 4-input NOR, followed by an inverter would use four more transistors and therefore more area for a given transistor size. In addition, even more area would be needed to beef up the size (and increase the speed) of the *p*-channels in the 4-input NOR gate, and the result would probably be an 8-input NAND that's still not as fast as the design in the preceding paragraph.



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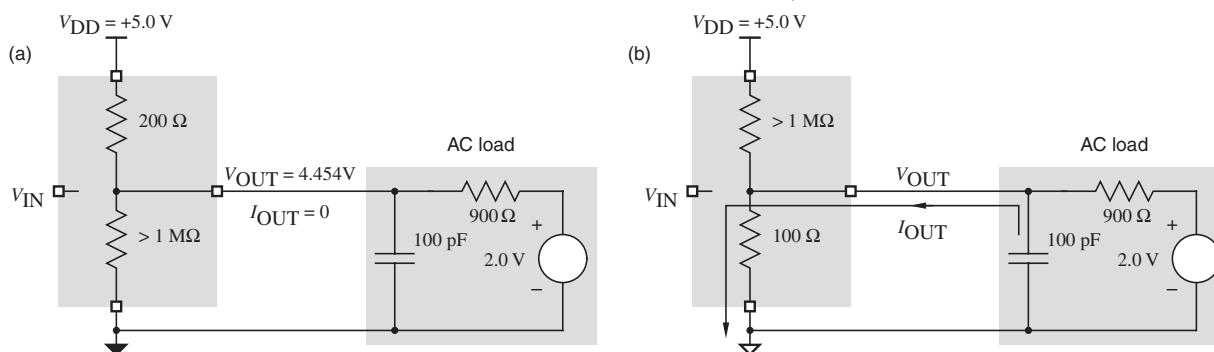
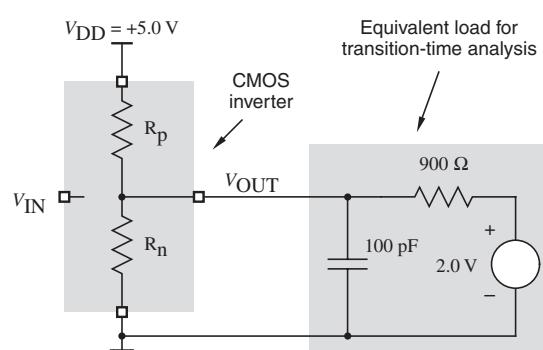
- 3e3.64 3.64 TTL-compatible inputs have  $V_{IHmin} = 2.0V$ , and typical TTL outputs have  $V_{OHmin} = 2.7V$ . CMOS output levels are already high compared to these levels, so there's no point in wasting silicon to make them any higher by lowering the voltage drop in the HIGH state.

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- 3e3.67 3.67 The rise time would not be exactly double the fall time, though this may be a useful first-order approximation. The exact amounts depend on the exact values of the HIGH and LOW thresholds within the signal swing, and also are affected by the fact that the rising and falling transitions are not straight lines but inverse exponential curves. Therefore, if the threshold occurs further along the nonlinear “tail” of the curve, the transition time to that threshold is more than proportionally affected by an increase in the  $RC$  time constant.

- G3.269 3.68 Including the DC load, a CMOS output's rise and fall times can be analyzed using the equivalent circuit shown to the right. This problem analyzes the fall time. Part (a) of the figure below shows the electrical conditions in the circuit when the output is in a steady HIGH state. Note that two resistors form a voltage divider, so the HIGH output is 4.454V, not quite 5.0 V as it was in Section 3.6.1. At time  $t = 0$  the CMOS output changes to the LOW state, resulting in the situation depicted in (b). The output will eventually reach a steady LOW voltage of 0.2 V, again determined by a voltage divider.



At time  $t = 0$ ,  $V_{OUT}$  is still 4.454V, but the Thévenin equivalent of the voltage source and the two resistors in the LOW state is  $90\Omega$  in series with a 0.2-V voltage source. At time  $t = \infty$ , the capacitor will be discharged to the Thévenin-equivalent voltage and  $V_{OUT}$  will be 0.2V. In between, the value of  $V_{OUT}$  is governed by an exponential law:

$$\begin{aligned} V_{OUT} &= 0.2V + (4.454 - 0.2V) \cdot e^{-t/(R_n C_L)} \\ &= 0.2V + 4.254 \cdot e^{-t/(90 \cdot 100 \cdot 10^{-12})}V \\ &= 0.2V + 4.254 \cdot e^{(-t)/(9 \cdot 10^{-9})}V \end{aligned}$$

Because of the DC load resistance, the time constant is a little shorter than it was in Section 3.6.1, at 9 ns. To obtain the fall time, we must solve the preceding equation for  $V_{OUT} = 3.5$  and  $V_{OUT} = 1.5$ , yielding

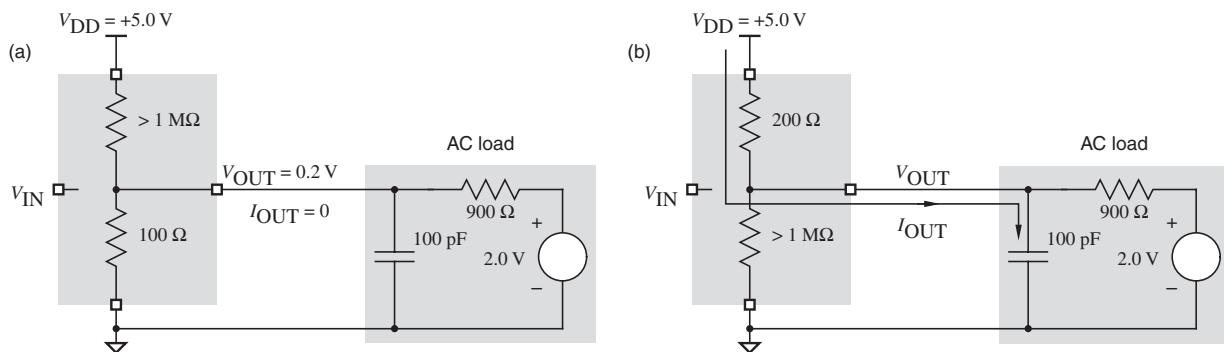
$$t = -9 \cdot 10^{-9} \cdot \ln \frac{V_{OUT} - 0.2V}{4.254}$$

$$t_{3.5} = 2.29 \text{ ns}$$

$$t_{1.5} = 10.67 \text{ ns}$$

The fall time  $t_f$  is the difference between these two numbers, or about 8.4 ns. This is slightly shorter than the 8.5 ns result in Section 3.6.1 because of the slightly shorter time constant.

- 3e3.69 3.69** Rise time can be calculated in a manner similar to the solution of Exercise 3.68. Part (a) of the figure below shows the conditions in the circuit when the output is in a steady LOW state with  $V_{OUT} = 0.2\text{ V}$  as predicted in Exercise 3.68. If at time  $t = 0$  the CMOS output changes to the HIGH state, the situation depicted in (b) results. The Thévenin equivalent of the voltage source and the two resistors in the HIGH state is  $163.6\Omega$  in series with a  $4.545\text{-V}$  voltage source.



$V_{OUT}$  cannot change instantly, but at time  $t = \infty$ , the capacitor will be charged to the Thévenin-equivalent voltage of  $4.545\text{ V}$ . Until then, the value of  $V_{OUT}$  in between is governed by an exponential law:

$$\begin{aligned} V_{OUT} &= 0.2\text{ V} + (4.545 - 0.2\text{ V}) \cdot (1 - e^{-t/R_p C_L}) \\ &= 0.2\text{ V} + 4.345 \cdot (1 - e^{-t/163.6 \cdot 100 \cdot 10^{-12}})\text{ V} \\ &= 0.2\text{ V} + 4.345 \cdot (1 - e^{-t/16.36 \cdot 10^{-9}})\text{ V} \end{aligned}$$

The  $RC$  time constant in this case is  $16.36\text{ ns}$ . To obtain the rise time, we must solve the preceding equation for  $V_{OUT} = 1.5$  and  $V_{OUT} = 3.5$ , yielding

$$t = -16.36 \cdot 10^{-9} \cdot \ln \frac{4.545 - V_{OUT}}{4.356}$$

$$t_{1.5} = 5.82\text{ ns}$$

$$t_{3.5} = 23.35\text{ ns}$$

The rise time  $t_r$  is the difference between these two numbers, or  $17.53\text{ ns}$ . Although the time constant is shorter than in Section 3.6.1, the asymptote of  $4.545\text{ V}$  is appreciably closer to the threshold than the  $5\text{-V}$  asymptote in Section 3.6.1, so the rising edge starts slowing sooner, and the overall rise time is slightly longer than the  $17\text{-ns}$  result in Section 3.6.1 (as suggested in the solution to Exercise 3.67).

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- 3e3.70 3.70 The time constant is  $1k\Omega \cdot 50 \text{ pF} = 50 \text{ ns}$ . We solve the rise-time equation for the point at which  $V_{\text{OUT}}$  is 1.5 V, as on p. 119 of the text:

$$t_{1.5} = -50 \cdot 10^{-9} \cdot \ln \frac{5.0 - 1.5}{5.0}$$

$$t_{1.5} = 17.83 \text{ ns}$$

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G3.272 3.72

$$\begin{aligned} R_{p(on)} &= \frac{V_{DD} - V_{OHminT}}{|I_{OHmaxT}|} \\ &= (5.0 - 3.84)/0.004 = 290\Omega \\ R_{n(on)} &= \frac{V_{OLmaxT}}{|I_{OLmaxT}|} \\ &= 0.33/0.004 = 55\Omega \end{aligned}$$

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- G3.274 3.74 a) For 3.3-V driving 1.8 V, the HIGH-state margin is  $2.4 - 1.2 = 1.2V$  and the LOW-state-margin is  $0.65 - 0.4 = 0.25V$ .  
b) For 2.5-V driving 1.8 V, the HIGH-state margin is  $2.0 - 1.2 = 0.8V$  and the LOW-state-margin is  $0.65 - 0.4 = 0.25V$ .

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- 3e3.74 3.75 For 3.3-V driving 5-V, the HIGH-state margin is 0.4V and the LOW-state-margin is 0.4V. For 5-V driving 3.3-V, the margins are the same.

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- 3e3.75    3.76 For 2.5-V driving 3.3-V, the HIGH-state margin is 0.0V and the LOW-state-margin is 0.4V. For 3.3-V driving 2.5-V, the HIGH-state margin is 0.7V and the LOW-state-margin is 0.3V.

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- G3.275    3.77 a) For 2.5 V, the HIGH-state margin is  $2.0 - 1.7 = 0.3V$  , the LOW-state-margin is  $0.67 - 0.4 = 0.27V$  .  
b) For 1.8 V, the HIGH-state margin is  $1.45 - 1.2 = 0.25V$  , the LOW-state-margin is  $0.65 - 0.45 = 0.20V$  .

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- G3.276 3.78 The voltage drop across the resistor is  $5.0 - 1.6 - 0.3 = 3.1\text{V}$ , so the current is  $3.1/390 = 7.9\text{mA}$ . The power dissipated is  $3.1\text{V} \times 7.9\text{mA} = 25\text{mW}$ .

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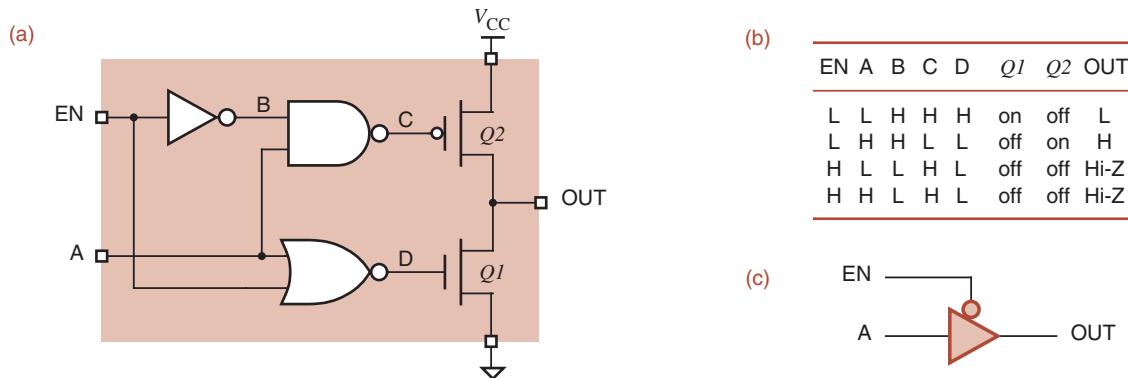
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- 3e3.77    3.79 The LSB toggles at a rate of 16 MHz. It takes two clock ticks for the LSB to complete one cycle, so the transition frequency is 8 MHz. The MSB's frequency is  $2^7$  times slower, or 62.5 KHz. The LSB's dynamic power is the most significant, but the sum of the transitions on the higher order bits, a binary series, is equivalent to almost another 8 MHz worth of transitions on a single output bit. Including the LSB, we have almost 16 MHz, but applied to the load capacitance on just a single output. If the different outputs actually have different load capacitances, then a weighted average would have to be used.

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3e3.81 3.83



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For exclusive use of adopters of the book *Digital Design Principles and Practices*, Fourth Edition, by John F. Wakerly,  
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- 3e3.95 3.86 Label the two leftmost NAND-gate outputs RS and UV, and label the topmost NAND-gate input RSUV. The output functions are

$$RS = (R \cdot S)'$$

$$UV = (U \cdot V)'$$

Without the diodes, the resistor pulls the top input of the topmost NAND gate HIGH, and its output function is

$$X = P'$$

With the diodes in place, the RSUV input is pulled LOW whenever RS or UV is LOW. Thus, the diodes perform a diode-AND function. Therefore, the new output function is

$$X = (P \cdot RSUV)'$$

$$X = (P \cdot RS \cdot UV)'$$

$$= (P \cdot (R \cdot S)' \cdot (U \cdot V)')$$

$$= P' + R \cdot S + U \cdot V$$

The diode-AND arrangement has poor LOW-state noise margins. If we assume that the diode drop is 0.7V, and that outputs RS and UV may be as high as 0.4V in the LOW state, then a “LOW” signal at RSUV may be as high as 1.1V. This is 0.3V *higher* than the maximum voltage that is guaranteed to be recognized as a LOW .

In a practical circuit, if such a kludge is really necessary, the noise margin may be improved by using germanium or Schottky diodes, which have a lower diode drop. In any case, note that the propagation delay to the X output for input transitions that cause RSUV to go HIGH may be longer than the specified gate delays, both because of the signal delay through the diode and because of the possibly long rise time of transitions on RSUV due to passive pull up by the resistor.

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G3.299 3.87

(a) Since  $V = 3.00$  is determined by the voltage divider ratio, we can write

$$5 \cdot \left( \frac{R2}{R1 + R2} \right) = 3.00$$

$$R2 = 1.50 \cdot R1$$

At the same time, the  $R = 120\Omega$  requirement constrains  $R1$  and  $R2$  as follows:

$$R = 120\Omega$$

$$R1 \parallel R2 = 120\Omega$$

$$\frac{R1 \cdot R2}{R1 + R2} = 120\Omega$$

$$R1 \cdot \left( \frac{1 \cdot 1.50}{1 + 1.50} \right) = 120\Omega$$

$$R1 = 200\Omega$$

$$R2 = 300\Omega$$

(b) In a similar way, we find

$$R1 = 331.5\Omega$$

$$R2 = 389.1\Omega$$

This is close to the  $(330/390)\Omega$  termination often used in practice

(c)

$$R1 = 312.5\Omega$$

$$R2 = 288.5\Omega$$

(d)

$$R1 = 166.7\Omega$$

$$R2 = 71.4\Omega$$

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G3.300 3.88 For 74LS, we have

$$V_{OLmax} = 0.5V$$

$$I_{LOmax} = 8mA$$

$$V_{OHmin} = 2.7V$$

$$I_{OHmax} = -400\mu A$$

For each termination, we determine whether the current exceeds the driving gate's capability in the LOW or HIGH state

(a) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ? I_{OLmax}$$

$$\frac{3.0 - 0.5}{120} = 20.8mA > I_{OLmax}$$

So a standard 74LS gate cannot properly drive this termination.

It is worth noting that in the HIGH state, the Thévenin voltage  $V$  is higher than the required  $V_{OHmin} = 2.7V$ , so the output does not have to source *any* current in the HIGH state. However, since the LOW state requires too much sink current, overall we have to say that this gate and termination are incompatible

(b) Once again, no current is required in the HIGH state. In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq I_{OLmax}$$

$$\frac{2.7 - 0.5}{179} = 12.3mA > I_{OLmax}$$

So a standard 74LS gate cannot properly drive this termination.

(c) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ? I_{OLmax}$$

$$\frac{2.4 - 0.5}{150} = 12.7mA > I_{OLmax}$$

In the HIGH state, we compute

$$\frac{V_{OH} - V_{OL}}{R} \leq ? |I_{OHmax}|$$

$$\frac{2.7 - 2.4}{150} = 2.0mA > |I_{OHmax}|$$

So a standard 74LS gate cannot properly drive this termination in either state.

(d) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ? I_{OLmax}$$

$$\frac{1.5 - 0.5}{50} = 20.0mA > I_{OLmax}$$

In the HIGH state, we compute

$$\frac{V_{OH} - V_{OL}}{R} \leq ? |I_{OHmax}|$$

$$\frac{2.7 - 1.5}{50} = 24.0mA > |I_{OHmax}|$$

So a standard 74LS gate cannot properly drive this termination in either state.

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For 74S, we have

$$V_{OLmax} = 0.5V$$

$$I_{OLmax} = 20mA$$

$$V_{OHmin} = 2.7V$$

$$I_{OHmax} = -1000\mu A$$

For each termination, we determine whether the current exceeds the driving gate's capability in the LOW or HIGH state.

(a) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ? I_{OLmax}$$

$$\frac{3.0 - 0.5}{120} = 20.8mA > I_{OLmax}$$

While no current is required in the HIGH state (since  $V > V_{OHmin}$ ), a standard 74LS gate cannot properly drive this termination.

(b) Once again, no current is required in the HIGH state. In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ? I_{OLmax}$$

$$\frac{2.7 - 0.5}{179} = 12.3mA < I_{OLmax}$$

So a standard 74S gate *can* properly drive this termination.

(c) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ? I_{OLmax}$$

$$\frac{2.4 - 0.5}{150} = 12.7mA < I_{OLmax}$$

In the HIGH state, we compute

$$\frac{V_{OH} - V_{OL}}{R} \leq ? |I_{OHmax}|$$

$$\frac{2.7 - 2.4}{150} = 2.0mA > |I_{OHmax}|$$

So a standard 74LS gate cannot properly drive this termination.

(d) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ? I_{OLmax}$$

$$\frac{1.5 - 0.5}{50} = 20.0mA = I_{OLmax}$$

In the HIGH state, we compute

$$\frac{V_{OH} - V_{OL}}{R} \leq ? |I_{OHmax}|$$

$$\frac{2.7 - 1.5}{50} = 24.0mA > |I_{OHmax}|$$

So a standard 74S gate cannot properly drive this termination in the HIGH state.

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For 74FCT-T, we have

$$V_{OLmax} = 0.55V$$

$$I_{OLmax} = 64mA$$

$$V_{OHmin} = 2.4V$$

$$I_{OHmax} = -15mA$$

For each termination, we determine whether the current exceeds the driving gate's capability in the LOW or HIGH state.

(a) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ?I_{OLmax}$$

$$\frac{3.0 - 0.55}{120} = 20.4mA < I_{OLmax}$$

No current is required in the HIGH state (since  $V > V_{OHmin}$ ), so a standard 74FCT-T gate *can* properly drive this termination in either state.

(b) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ?I_{OLmax}$$

$$\frac{2.7 - 0.55}{179} = 12.0mA < I_{OLmax}$$

No current is required in the HIGH state (since  $V > V_{OHmin}$ ), so a standard 74FCT-T gate *can* properly drive this termination in either state.

(c) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ?I_{OLmax}$$

$$\frac{2.4 - 0.55}{150} = 12.3mA < I_{OLmax}$$

No current is required in the HIGH state (since  $V = V_{OHmin}$ ), so a standard 74FCT-T gate *can* properly drive this termination in either state.

(d) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ?I_{OLmax}$$

$$\frac{1.5 - 0.55}{50} = 19.0mA < I_{OLmax}$$

In the HIGH state, we compute

$$\frac{V_{OH} - V_{OL}}{R} \leq ?|I_{OHmax}|$$

$$\frac{2.4 - 1.5}{50} = 18.0mA > |I_{OHmax}|$$

Since this exceeds the output specification in the HIGH state, a standard 74FCT-T gate cannot properly drive the termination.

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- G3.303 3.89 The longest name that we could find was 74ALVCHG162280 (14 characters), for when you need a 16-to-32 bit Registered Bus Exchanger with byte masks and 3-state outputs.

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G3.201 3.1 The “probably” cases may cause damage to the gate if sustained.

- (a) 0
- (b) 0
- (c) 1
- (d) probably 0
- (e) undefined
- (f) probably 0
- (g) 1
- (h) probably 1

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G3.202 3.2 The “probably” cases may cause damage to the gate if sustained.

- (a) 1
- (b) 1
- (c) 0
- (d) probably 1
- (e) undefined
- (f) probably 1
- (g) 0
- (h) probably 0

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- 3e3.3 3.3 A logic buffer is a non-linear amplifier that maps the entire set of possible analog input voltages into just two output voltages, HIGH and LOW. An audio amplifier has a linear response over its specified operating range, mapping each input voltage into an output voltage that is directly proportional to the input voltage.

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3e3.4 3.4 Yes, both.

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- G3.205 3.5 False. The outputs are the same, since an OR gate with inverted inputs is the same as a NAND gate.

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- 3e3.6 3.6 From the *American Heritage Electronic Dictionary (AHED)*, copyright 1992 by Houghton Mifflin Company:
- (1) A structure that can be swung, drawn, or lowered to block an entrance or a passageway.
  - (2) a. An opening in a wall or fence for entrance or exit. b. The structure surrounding such an opening, such as the monumental or fortified entrance to a palace or walled city.
  - (3) a. A means of access: the gate to riches. b. A passageway, as in an airport terminal, through which passengers proceed for embarkation.
  - (4) A mountain pass.
  - (5) The total paid attendance or admission receipts at a public event: a good gate at the football game.
  - (6) A device for controlling the passage of water or gas through a dam or conduit.
  - (7) The channel through which molten metal flows into a shaped cavity of a mold.
  - (8) Sports. A passage between two upright poles through which a skier must go in a slalom race.
  - (9) Electronics. A circuit with multiple inputs and one output that is energized only when a designated set of input pulses is received.

Well, definition (9) is closest to one of the answers that I had in mind. The other answer I was looking for is the gate of a MOS transistor.

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- G3.207 3.7 A CMOS NAND gate uses four transistors: two *p*-channel transistors and two *n*-channel transistors.

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- G3.208 3.8 The NAND gate has 2 inputs, A and B, and output Z. Connect gate input A to the coil of Relay 1 and gate input B to the coil of Relay 2. Tie the other side of each coil to ground. Tie both normally-closed contacts to  $V_{CC}$  and the normally-open contact of Relay 1 to ground. Tie the “common” contact of Relay 1 to the normally-open contact of Relay 2. The “common” contact of Relay 2 is the gate output Z. Of course, this circuit is not really “equivalent” to the CMOS NAND gate, since the relay coils draws a lot more current than the gate terminals of MOS transistors.

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3e3.9 3.9 A NAND gate, according to the box on page 92.

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- 3e3.10 3.10 See definitions on pp. 92, 97, and 111. You're much more likely to calculate fanout. Fan-in is a concern only to the circuit designer of a gate

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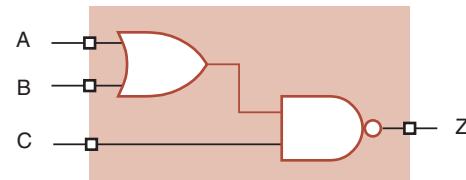
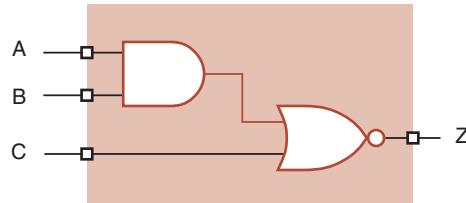
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3e3.14 3.16 A CMOS inverting gate has fewer transistors than a noninverting one, since an inversion comes “for free.”

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- G3.215 3.17 Simple, inverting CMOS gates generally have two transistors per input. Four types that meet the requirements of the problem are 3-input NAND, 3-input NOR, 3-input AND-OR-INVERT, and 3-input OR-AND-INVERT. Logic symbols for the last two types are shown below.



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- 3e3.18 3.19 One way is that a romance could be sparked, and the designers could end up with a lot less time to do their work. Another way is that the stray perfume in the IC production line could have contaminated the circuits used by the designers, leading to marginal operation, more debugging time by the dedicated designers, and less time for romance. By the way, the whole perfume story may be apocryphal.

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- 3e3.20 3.20 Using the maximum output current ratings in both states, the HIGH-state margin is 0.69V and the LOW-state margin is 1.02V. With CMOS loads (output currents less than 20  $\mu$ A), the margins improve to 1.349V and 1.25V, respectively.

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G3.219 3.21 High-state noise margin looks like about 1.2V (4.7V - 3.5V). Low-state margin is about 1.0V (1.5V - 0.5V).

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- 3e3.21 3.22 The first answer for each parameter below assumes commercial operation and that the device is used with the maximum allowable (TTL) load. The number in parentheses, if any, indicates the value obtained under a lesser but specified (CMOS) load.

$$V_{OH\min} \quad 3.84\text{V (4.4V)}$$

$$V_{IH\min} \quad 3.15\text{V}$$

$$V_{IL\max} \quad 1.35\text{V}$$

$$V_{OL\max} \quad 0.33\text{V (0.1V)}$$

$$I_{Imax} \quad 1\mu\text{A}$$

$$I_{OL\max} \quad 4\text{ mA (20 }\mu\text{A)}$$

$$I_{OH\max} \quad -4\text{ mA (-20 }\mu\text{A)}$$

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3e3.22 3.23 Current is positive if it flows *into* a node. Therefore, an output with negative current is *sourcing* current.

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- 3e3.24 3.24 (Note typo in the first printing; change “2.0–5.0 V” to “3.15–5.0 V.”) The specification for the 74HC00 shows a maximum power-supply current of 10  $\mu\text{A}$  when the inputs are at 0 or 5V, but based on the discussion in Section 3.5.3 we would expect the current to be more when the inputs are at their worst-case values (1.35 or 3.15V). If we consider “nonlogic” input values, the maximum current will flow if the inputs are held right at the switching threshold, approximately  $V_{CC}/2$ .

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- G3.225 3.25 For the 74HC00,  $I_{OHmax} = 4mA$ , while for the 74ALS00,  $I_{ILmax} = -0.2mA$ . Therefore, the LOW-state fanout is 20. For the 74HC00,  $I_{OHmax} = -4mA$ , while for the 74ALS00,  $I_{IHmax} = 0.02mA$ . Therefore, the HIGH-state fanout is 200. The overall fanout is the minimum of these two numbers, or 20.

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- 3e3.26 3.26 Using the formulas on page 120, we can estimate that  $R_{p(on)} = (5.0 - 3.84)/0.004 = 290\Omega$  or, using the higher value of  $V_{OHmin}$  in the spec, that  $R_{p(on)} = (5.0 - 4.4)/0.00002 = 30K\Omega$ . (The discrepancy shows that the output characteristic of this device is somewhat nonlinear.) We can also estimate  $R_{n(on)} = 0.33/0.004 = 82.5\Omega$ .

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G3.223 3.27 The 74HC00 output drive is so weak, it's not good for driving much:

- (a) Assume that in the LOW state the output pulls down to 0.33 V (the maximum  $V_{OL}$  spec). Then the output current is  $(5.0V - 0.33V)/120\Omega = 38.9\text{mA}$ , which is way more than the 4-mA commercial spec.
- (b) For this problem, you first have to find the Thévenin equivalent of the load, or  $148.5\Omega$  in series with 2.75 V. In the HIGH state, the gate must pull the output up to 3.84 V, a difference of 1.09 V across  $148.5\Omega$ , requiring 7.3 mA, which is out of spec. In the LOW state, we have a voltage drop of  $2.75V - 0.33V$  across  $148.5\Omega$ , so the output must sink 16.3 mA, again out of spec.
- (c) The output must source enough current to create a 3.84-V drop across an  $820\Omega$  resistor, or 4.7 mA. This is out of spec.
- (d) The Thévenin equivalent is  $235\Omega$  in series with 2.5 V. In the HIGH state, the gate must pull the output up to 3.84 V, a difference of 1.34 V across  $235\Omega$ , requiring 5.7 mA, which is out of spec. In the LOW state, we need a 2.17-V drop across  $235\Omega$ , or 9.2 mA, which is also way out of spec.
- (e) The HIGH state is no problem, because the resistor pulls the output up to 5 V on its own. In the LOW state, we need a 4.67-V drop across  $1000\Omega$ , or 4.7 mA, which is within spec.
- (f) The Thévenin equivalent is  $487\Omega$  in series with 2.03 V. In the HIGH state, the gate must pull the output up to 3.84 V, a difference of 1.81 V across  $487\Omega$ , requiring 3.7 mA, which is within spec. In the LOW state, we need a 1.7-V drop across  $487\Omega$ , or 3.5 mA, which is also within spec.
- (g) The HIGH state is no problem, because the resistor pulls the output up to 5 V on its own. In the LOW state, we need a 4.67-V drop across  $4700\Omega$ , or about 1.0 mA, which is within spec.

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3e3.27 3.28 Generally, never. However, some devices have internal pull-ups, and can therefore be allowed to “float.”

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- 3e3.28 3.29 See pages 113–114. In practice, CMOS device latch-up is most often caused by applying to an input a voltage that is more than a diode-drop higher than the power-supply voltage, typically in a situation where inputs are active but the power supply hasn't been turned on (or hasn't "ramped up") yet. This triggers a "parasitic SCR" which is part of the CMOS device's physical structure, which creates a low-impedance path between the device's power and ground terminals, even after the triggering condition is removed.

Modern CMOS devices, though still susceptible to latch up, have been somewhat "hardened" by including structures that prevent the SCR from triggering unless the higher-voltage input source is able to source *lots* of current. For example, quoting from Integrated Device Technology's 1992 *High-Performance Logic* databook,

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes. The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are used on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents from 10–20 mA, IDT products inhibit latchup at trigger currents substantially greater than this.

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- G3.229 3.30 The purpose of decoupling capacitors is to provide the instantaneous power-supply current that is required during output transitions. Capacitors have stray inductance, which acts as a barrier to current flow at high frequencies (fast transition rates). The large physical structures of large capacitors (such as power-supply filter capacitors) typically have more stray inductance than smaller capacitors, so they may actually be less effective at supplying current quickly at high frequencies.

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- 3e3.30 3.31 Before handing over a CMOS device. If you are different potentials, you may damage the device.  
By the way, it takes about 5–6 kV of potential difference to generate a static spark big enough to feel, but most devices are rated to survive only about 2 kV without damage. So even if you don't feel the static, you may be damaging devices.

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- 3e3.31 3.32 Propagation delay and transition time. If the sizes of the internal transistors are properly balanced, propagation delay tends to be about the same regardless of the transition direction. The same is true for transition time. Note that *p*-channel transistors have to be about twice the size of corresponding *n*-channel transistors to achieve the same low resistance. If the *p*-channel transistors are “undersized,” then LOW-to-HIGH transitions will tend to longer than HIGH-to-LOW ones, because the load capacitance must charge through a higher resistance.

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G3.232 3.33 (a) 5 ns; (b) 705 ns; (c) 2.2 ns; (d) 100 ns.

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- G3.233 3.34 A 5% increase in power-supply voltage has a bigger effect than the same percentage increase in internal and load capacitance, since power consumption is proportional to the square of the voltage ( $CV^2f$ ) .

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- G3.234 3.35 CMOS inputs have very low input-current requirements, typically less than a microampere of leakage current. Thus, a CMOS output with 4 mA of driving capability could theoretically drive 4000 CMOS inputs. Having this number of inputs connected to a single output is rare, except in clock-driving applications in large chips. And even in this case, a single output is unlikely to drive that many inputs, because the high capacitive load of 4000 inputs would slow down the transition times too much. Slow transition times cause uncertainty in when the transition is actually detected by different inputs, and also increases power consumption in the input structures of the driven inputs.

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- G3.235 3.36 The answer depends on operating frequency  $f$ . If  $f = 0$  and leakage (quiescent) current remains unchanged, then the 2.5-V power consumption is  $2.5/5 = 66\%$  of the 5-V power consumption. If  $f$  is large enough that most of the current is attributable to  $CV^2f$  power consumption, then the 2.5-V power consumption is  $(2.5/5)^2 = 25\%$  of the 5-V power consumption. In practice, the answer lies somewhere in between, but 25% is an often-used rule of thumb.

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G3.236 3.37 Hysteresis depends only on the difference in threshold voltages, and is 0.5 V in this case.

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- G3.237 3.38 If the output enables were changed at the same time, then the output being enabled would start driving before the other output was disabled. This would result in the bus being driven by both gates for an instant every time the output enables were switched. (Also see Section 6.6).

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- 3e3.38 3.39 Smaller resistors result in shorter rise times for LOW-to-HIGH transitions but higher power consumption in the LOW state. Stated another way, larger resistors result in lower power consumption in the LOW state but longer rise times (more ooze) for LOW -to-HIGH transitions.

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- 3e3.39 3.40 The resistor must drop  $5.0 - 2.0 - 0.37 = 2.63\text{V}$  with  $5\text{mA}$  of current through it. Therefore  $r = 2.63/0.005 = 526\Omega$ ; a good standard value would be  $510\Omega$ .

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- G3.240 3.41 For the 74HC CMOS family,  $V_{OHmin}$  is 3.8 V. So the resistor must drop  $3.8 - 2.0 = 1.8V$  with 2mA of current through it. Therefore  $r = 1.8/0.002 = 900\Omega$ ; a good standard value would be  $910\Omega$ .

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- 3e3.41    3.42 The wired output has only passive pull-up to the HIGH state. Therefore, the time for LOW-to-HIGH transitions, an important component of total delay, depends on the amount of capacitive loading and the size of the pull-up resistor. A moderate capacitive load (say, 100 pF) and even a very strong pull-up resistor (say,  $150\Omega$ ) can still lead to time constants and transition times (15 ns in this example) that are longer than the delay of an additional gate with active pull-up.

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- 3e3.42 3.43 The winner is 74FCT-T—48 mA in the LOW state and 15 mA in the HIGH state (see Table 3–8). TTL families don't come close.

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- G3.243 3.44 The “T” suffix indicates that gate inputs are guaranteed recognize TTL input levels. The absence of a “T” indicates that inputs require CMOS levels. The output characteristics of the ACT family are stronger; it can drive 24mA while the HC family can only drive 4mA. Finally, the precocious student may note that ACT is a lot faster.

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- 3e3.44 3.45 FCT devices are not targeted to be interfaced with pure CMOS loads. Anyway, in cases where they are used with pure CMOS loads, their outputs are so strong that they easily meet the CMOS input requirements, except for FCT-T, which may have a reduced  $V_{OH}$ .

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3e3.45 3.46 The typical output HIGH level is about a volt less, which reduces  $CV^2f$  power consumption.

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3e3.46 3.47  $n$  diodes are required.

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3e3.48 3.48 TTL outputs, as well as TTL-compatible CMOS outputs, are more capable of sinking current than sourcing it.

- G3.249 3.49 For each interfacing situation, we compute the fanout in the LOW state by dividing  $I_{OLmax}$  of the driving gate by  $I_{ILmax}$  of the driven gate. Similarly, the fanout in the HIGH state is computed by dividing  $I_{OLmax}$  of the driving gate by  $I_{IHmax}$  of the driven gate. The overall fanout is the lower of these two results.

Case	Low-state		High-state		Overall Fanout	Excess	
	Ratio	Fanout	Ratio	Fanout		State	Drive
74LS driving 74AS	$\frac{8mA}{0.5mA}$	16	$\frac{400\mu A}{20\mu A}$	20	16	HIGH	80μA
74LS driving 74F	$\frac{8mA}{0.6mA}$	13	$\frac{400\mu A}{20\mu A}$	20	13	HIGH	140μA
74F driving 74LS	$\frac{20mA}{0.4mA}$	50	$\frac{1000\mu A}{20\mu A}$	50	50	none	
74F driving 74AS	$\frac{20mA}{0.5mA}$	40	$\frac{1000\mu A}{20\mu A}$	50	40	HIGH	200μA
74AS driving 74S	$\frac{20mA}{2mA}$	10	$\frac{2000\mu A}{50\mu A}$	40	10	HIGH	1500μA
74S driving 74ALS	$\frac{20mA}{0.2mA}$	100	$\frac{1000\mu A}{20\mu A}$	50	50	LOW	10mA
74ALS driving 74S	$\frac{8mA}{2mA}$	4	$\frac{400\mu A}{50\mu A}$	8	4	HIGH	200μA
74F driving 74F	$\frac{20mA}{0.6mA}$	33	$\frac{1000\mu A}{20\mu A}$	50	33	HIGH	340μA
74S driving 74S	$\frac{20mA}{2mA}$	10	$\frac{1000\mu A}{50\mu A}$	20	10	HIGH	500μA
74S driving 74F	$\frac{20mA}{0.6mA}$	33	$\frac{1000\mu A}{20\mu A}$	50	33	HIGH	340μA
74F driving 74ALS	$\frac{20mA}{0.2mA}$	100	$\frac{1000\mu A}{20\mu A}$	50	50	LOW	10mA
74AS driving 74LS	$\frac{20mA}{0.4mA}$	50	$\frac{2000\mu A}{20\mu A}$	100	50	HIGH	1000μA

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- 3e3.50 3.50 For the pull-down, we must have at most a 0.5-V drop in order to create a  $V_{IL}$  that is no worse than a standard LS-TTL output driving the input. Since  $I_{ILmax} = 0.4\text{mA}$ , we get  $R_{pd} = 0.5/0.004 = 1250\Omega$  and  $P_{pd} = V_{IL}^2/R_{pd} = (0.5)^2/1250 = 0.2\text{mW}$ . (Alternatively,  $P_{pd} = V_{IL}I_{IL} = 0.5 \cdot 0.0004 = 0.2\text{mW}$ )

For the pull-up, we must have at most a 2.3-V drop in order to create a  $V_{IH}$  that is no worse than a standard LS-TTL output driving the input. Since  $I_{IHmax} = 20\mu\text{A}$ , we get  $R_{pu} = 2.3/0.00002 = 115\text{k}\Omega$  and  $P_{pu} = V_{IH}^2/R_{pu} = (2.3)^2/115000 = 0.046\text{mW}$ . (Alternatively, we could have calculated the result as  $P_{pu} = V_{IH}I_{IH} = 2.3 \cdot 0.00002 = 0.046\text{mW}$ .) The pull-up dissipates less power.

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- G3.275    3.77 a) For 2.5 V, the HIGH-state margin is  $2.0 - 1.7 = 0.3V$  , the LOW-state-margin is  $0.67 - 0.4 = 0.27V$  .  
b) For 1.8 V, the HIGH-state margin is  $1.45 - 1.2 = 0.25V$  , the LOW-state-margin is  $0.65 - 0.45 = 0.20V$  .

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- G3.251 3.51 The AND-OR-INVERT gate should be faster since it uses only one level of logic in its transistor logic circuit. The AND gate contains an extra level of logic, since it is built as a NAND gate followed by an inverter. This assumes that both types of gates have transistors that switch at the same speed.

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- 3e3.52 3.52 The main benefit of Schottky diodes is to prevent transistors from saturating, which allows them to switch more quickly. The main drawback is that they raise the collector-to-emitter drop across an almost-saturated transistor, which decreases LOW-state noise margin.

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- J3.253 3.53 Assuming  $I_{OL} = 8\text{mA}$ , the worst-case LOW-state noise margin is 0.3V. Assuming  $I_{OL} = 4\text{mA}$ , the worst-case LOW-state noise margin is 0.4V. The worst-case HIGH-state noise margin in any case is 0.5V (at the minimum power-supply voltage).

For the 54ALS00, the worst-case LOW-state noise margin is 0.3V over the full military temperature range, and the worst-case HIGH-state noise margin is also 0.5V.

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G3.254 3.54  $V_{OHmin} = 2.5V$ ,  $V_{IHmin} = 2.0V$ ,  $V_{ILmax} = 0.8V$ ,  $V_{OLmax} = 0.5V(0.4V)$ ,  $I_{ILmax} = -0.1mA$ ,  
 $I_{IHmax} = 20 \mu A$ ,  $I_{OLmax} = 8mA$  (4 mA),  $I_{OHmax} = -0.4mA$ .

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G3.255 3.55

$R_{VCC}$ ( $\Omega$ )	$R_{GND}$ ( $\Omega$ )	$V_{Thev}$ (V)	$R_{Thev}$ ( $\Omega$ )	LOW-state			HIGH-state		
				$V_{Thev} - V_{OL}$ (V)	$I_{OL}$ (mA)	OK?	$V_{OH} - V_{Thev}$ (V)	$I_{OH}$ ( $\mu A$ )	OK?
470	—	5.0	470	4.5	9.57	no	<0	—	yes
330	470	2.94	193.9	2.44	12.57	no	<0	—	yes
—	6.8K	0	6.8K	<0	—	yes	2.7	397	yes
910	1200	2.84	518	2.34	4.53	yes	<0	—	yes
620	—	5.0	620	4.5	7.26	yes	<0	—	yes
510	470	2.4	245	1.9	7.76	yes	0.3	1235	no
—	5.1K	0	5.1K	<0	—	yes	2.7	529	no
464	510	2.62	243	2.12	8.72	no	0.08	337	yes

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G3.256 3.56

Case	LOW-state			HIGH-state		
	$V_{ILmax}$	$V_{OLmax(T)}$	Margin	$V_{IHmin}$	$V_{OHmin(T)}$	Margin
74HCT driving 74LS	0.8V	0.33V	0.47V	2.0V	3.84V	1.84V
74ALS driving 74HCT	0.8V	0.5V	0.3V	2.0V	2.7V	0.7V
74AS driving 74VHCT	0.8V	0.5V	0.3V	2.0V	2.7V	0.7V
74VHCT driving 74F	0.8V	0.44V	0.47V	2.0V	3.80V	1.80V

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- G3.257 3.57 For each interfacing situation, we compute the fanout in the LOW state by dividing  $I_{OLmax}$  of the driving gate by  $I_{ILmax}$  of the driven gate. Similarly, the fanout in the HIGH state is computed by dividing  $I_{OHmax}$  of the driving gate by  $I_{ILmax}$  of the driven gate. The overall fanout is the lower of these two results.

Case	LOW-state		HIGH-state		Overall Fanout	Excess	
	Ratio	Fanout	Ratio	Fanout		State	Drive
74HCT driving 74LS	$\frac{4\text{mA}}{0.4\text{mA}}$	10	$\frac{4000\text{\mu A}}{20\text{\mu A}}$	200	10	HIGH	3800 $\mu\text{A}$
74VHCT driving 74S	$\frac{8\text{mA}}{2\text{mA}}$	4	$\frac{8000\text{\mu A}}{50\text{\mu A}}$	160	4	HIGH	7800 $\mu\text{A}$
74VHCT driving 74ALS	$\frac{8\text{mA}}{0.2\text{mA}}$	40	$\frac{8000\text{\mu A}}{20\text{\mu A}}$	400	40	HIGH	7200 $\mu\text{A}$
74HCT driving 74AS	$\frac{4\text{mA}}{0.5\text{mA}}$	8	$\frac{4000\text{\mu A}}{20\text{\mu A}}$	200	8	HIGH	3840 $\mu\text{A}$

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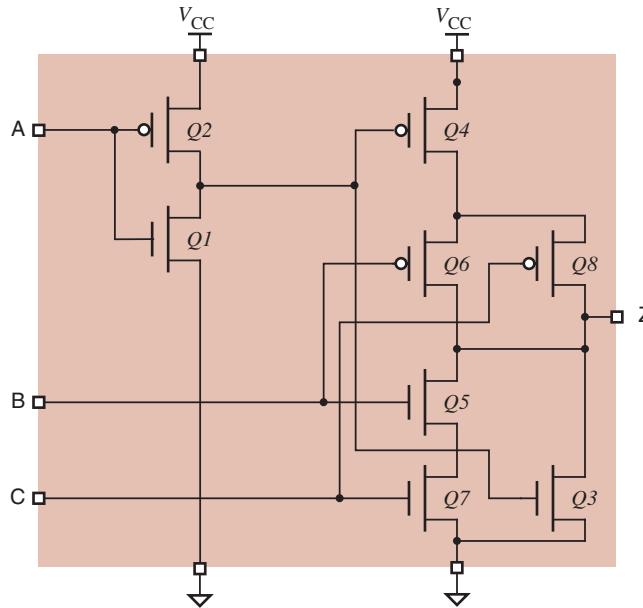
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- 3e3.58 3.58 CMOS has the widest voltage swing and therefore the highest dynamic power dissipation. It goes from 0.1V to 4.4 V, for a total swing of 4.3 V. An ECL output swings between -0.81 and -1.85, for a difference of only 1.04 V. The difference in power dissipation for a given capacitance and frequency is then the ratio of  $CV_{\text{CMOS}}^2 f$  to  $CV_{\text{ECL}}^2 f$ , or  $V_{\text{CMOS}}^2 / V_{\text{ECL}}^2$ . Plugging in the numbers tells us the dynamic power dissipation of CMOS is 17.1 times greater than ECL.

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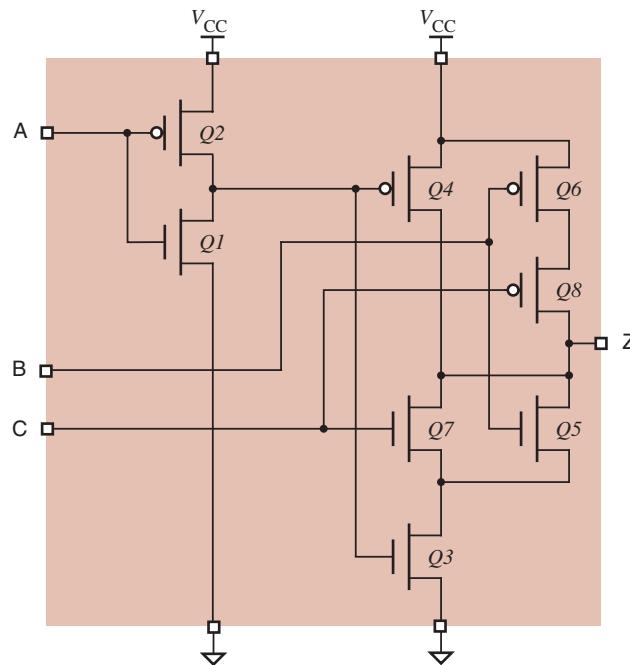
G3.259 3.59 The circuit shown below is a subset of the circuit in Figure 3–20(a) with an inverter on input A.



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**G3 . 260** 3.60 The circuit shown below is a subset of the circuit in Figure 3–22(a) with an inverter on input A.

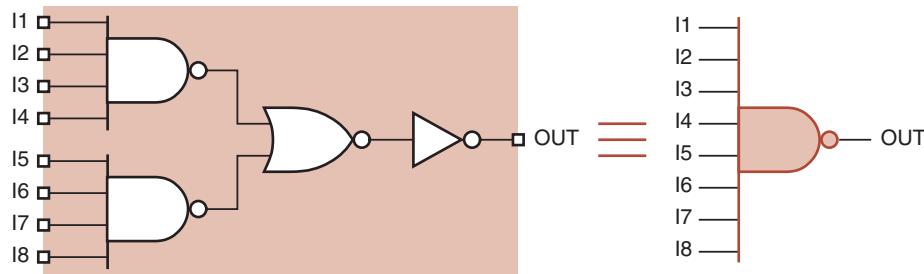


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- G3.263 3.63 Use two 4-input NAND gates on the first level, followed by a 2-input NOR, followed by an inverter, as in the figure below. This is most provides the best speed, because CMOS NOR gates are inherently slow because of the series connection of *p*-channel devices, and the 2-input NOR has the smallest number of these in series.

Designing the 8-input NAND as four 2-input NAND gates, followed by a 4-input NOR, followed by an inverter would use four more transistors and therefore more area for a given transistor size. In addition, even more area would be needed to beef up the size (and increase the speed) of the *p*-channels in the 4-input NOR gate, and the result would probably be an 8-input NAND that's still not as fast as the design in the preceding paragraph.



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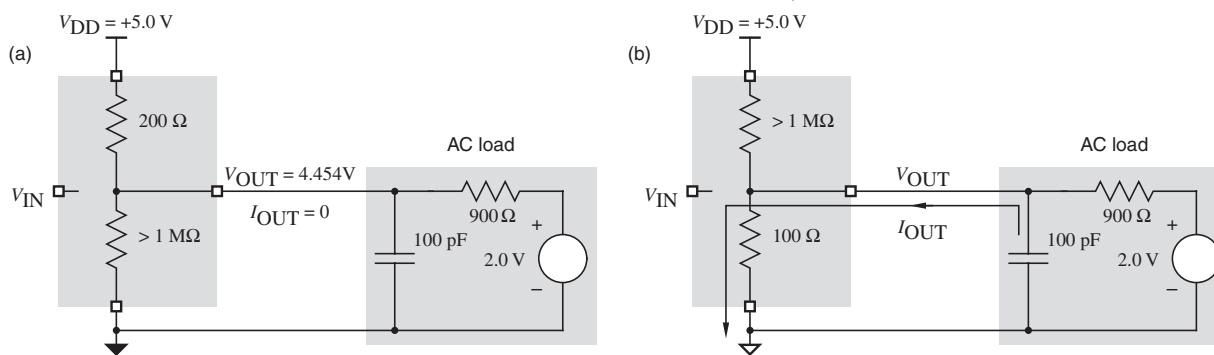
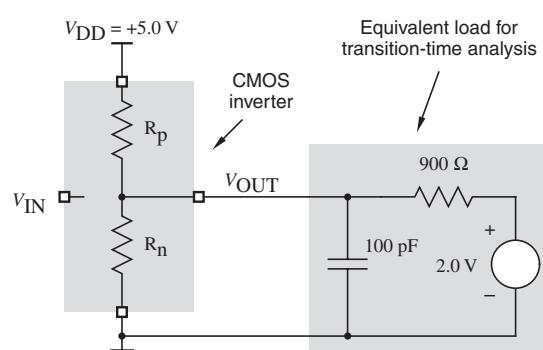
- 3e3.64 3.64 TTL-compatible inputs have  $V_{IHmin} = 2.0V$ , and typical TTL outputs have  $V_{OHmin} = 2.7V$ . CMOS output levels are already high compared to these levels, so there's no point in wasting silicon to make them any higher by lowering the voltage drop in the HIGH state.

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- 3e3.67 3.67 The rise time would not be exactly double the fall time, though this may be a useful first-order approximation. The exact amounts depend on the exact values of the HIGH and LOW thresholds within the signal swing, and also are affected by the fact that the rising and falling transitions are not straight lines but inverse exponential curves. Therefore, if the threshold occurs further along the nonlinear “tail” of the curve, the transition time to that threshold is more than proportionally affected by an increase in the  $RC$  time constant.

- G3.269 3.68 Including the DC load, a CMOS output's rise and fall times can be analyzed using the equivalent circuit shown to the right. This problem analyzes the fall time. Part (a) of the figure below shows the electrical conditions in the circuit when the output is in a steady HIGH state. Note that two resistors form a voltage divider, so the HIGH output is 4.454V, not quite 5.0 V as it was in Section 3.6.1. At time  $t = 0$  the CMOS output changes to the LOW state, resulting in the situation depicted in (b). The output will eventually reach a steady LOW voltage of 0.2 V, again determined by a voltage divider.



At time  $t = 0$ ,  $V_{OUT}$  is still 4.454V, but the Thévenin equivalent of the voltage source and the two resistors in the LOW state is  $90\Omega$  in series with a 0.2-V voltage source. At time  $t = \infty$ , the capacitor will be discharged to the Thévenin-equivalent voltage and  $V_{OUT}$  will be 0.2V. In between, the value of  $V_{OUT}$  is governed by an exponential law:

$$\begin{aligned} V_{OUT} &= 0.2V + (4.454 - 0.2V) \cdot e^{-t/(R_n C_L)} \\ &= 0.2V + 4.254 \cdot e^{-t/(90 \cdot 100 \cdot 10^{-12})}V \\ &= 0.2V + 4.254 \cdot e^{(-t)/(9 \cdot 10^{-9})}V \end{aligned}$$

Because of the DC load resistance, the time constant is a little shorter than it was in Section 3.6.1, at 9 ns. To obtain the fall time, we must solve the preceding equation for  $V_{OUT} = 3.5$  and  $V_{OUT} = 1.5$ , yielding

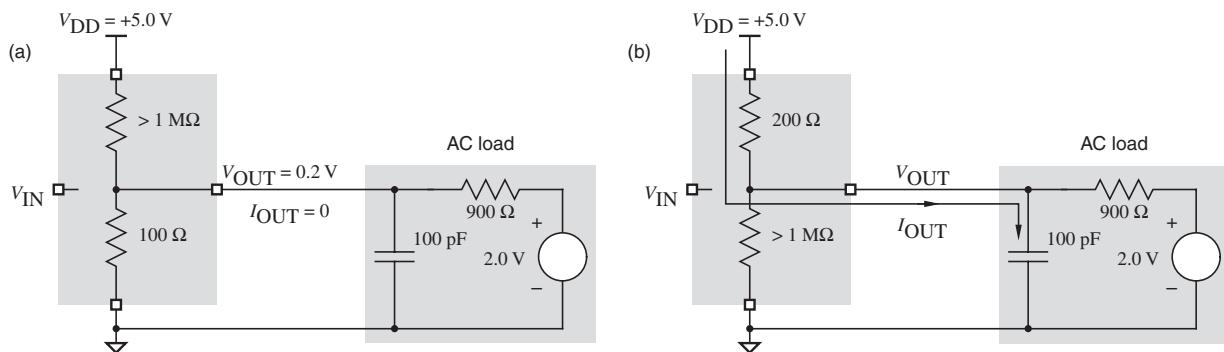
$$t = -9 \cdot 10^{-9} \cdot \ln \frac{V_{OUT} - 0.2V}{4.254}$$

$$t_{3.5} = 2.29 \text{ ns}$$

$$t_{1.5} = 10.67 \text{ ns}$$

The fall time  $t_f$  is the difference between these two numbers, or about 8.4 ns. This is slightly shorter than the 8.5 ns result in Section 3.6.1 because of the slightly shorter time constant.

- 3e3.69 3.69** Rise time can be calculated in a manner similar to the solution of Exercise 3.68. Part (a) of the figure below shows the conditions in the circuit when the output is in a steady LOW state with  $V_{OUT} = 0.2\text{ V}$  as predicted in Exercise 3.68. If at time  $t = 0$  the CMOS output changes to the HIGH state, the situation depicted in (b) results. The Thévenin equivalent of the voltage source and the two resistors in the HIGH state is  $163.6\Omega$  in series with a  $4.545\text{-V}$  voltage source.



$V_{OUT}$  cannot change instantly, but at time  $t = \infty$ , the capacitor will be charged to the Thévenin-equivalent voltage of  $4.545\text{ V}$ . Until then, the value of  $V_{OUT}$  in between is governed by an exponential law:

$$\begin{aligned} V_{OUT} &= 0.2\text{ V} + (4.545 - 0.2\text{ V}) \cdot (1 - e^{-t/R_p C_L}) \\ &= 0.2\text{ V} + 4.345 \cdot (1 - e^{-t/163.6 \cdot 100 \cdot 10^{-12}})\text{ V} \\ &= 0.2\text{ V} + 4.345 \cdot (1 - e^{-t/16.36 \cdot 10^{-9}})\text{ V} \end{aligned}$$

The  $RC$  time constant in this case is  $16.36\text{ ns}$ . To obtain the rise time, we must solve the preceding equation for  $V_{OUT} = 1.5$  and  $V_{OUT} = 3.5$ , yielding

$$t = -16.36 \cdot 10^{-9} \cdot \ln \frac{4.545 - V_{OUT}}{4.356}$$

$$t_{1.5} = 5.82\text{ ns}$$

$$t_{3.5} = 23.35\text{ ns}$$

The rise time  $t_r$  is the difference between these two numbers, or  $17.53\text{ ns}$ . Although the time constant is shorter than in Section 3.6.1, the asymptote of  $4.545\text{ V}$  is appreciably closer to the threshold than the  $5\text{-V}$  asymptote in Section 3.6.1, so the rising edge starts slowing sooner, and the overall rise time is slightly longer than the  $17\text{-ns}$  result in Section 3.6.1 (as suggested in the solution to Exercise 3.67).

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- 3e3.70 3.70 The time constant is  $1k\Omega \cdot 50 \text{ pF} = 50 \text{ ns}$ . We solve the rise-time equation for the point at which  $V_{\text{OUT}}$  is 1.5 V, as on p. 119 of the text:

$$t_{1.5} = -50 \cdot 10^{-9} \cdot \ln \frac{5.0 - 1.5}{5.0}$$

$$t_{1.5} = 17.83 \text{ ns}$$

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G3.272 3.72

$$\begin{aligned} R_{p(on)} &= \frac{V_{DD} - V_{OHminT}}{|I_{OHmaxT}|} \\ &= (5.0 - 3.84)/0.004 = 290\Omega \\ R_{n(on)} &= \frac{V_{OLmaxT}}{|I_{OLmaxT}|} \\ &= 0.33/0.004 = 55\Omega \end{aligned}$$

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- G3.274 3.74 a) For 3.3-V driving 1.8 V, the HIGH-state margin is  $2.4 - 1.2 = 1.2V$  and the LOW-state-margin is  $0.65 - 0.4 = 0.25V$ .  
b) For 2.5-V driving 1.8 V, the HIGH-state margin is  $2.0 - 1.2 = 0.8V$  and the LOW-state-margin is  $0.65 - 0.4 = 0.25V$ .

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- 3e3.74 3.75 For 3.3-V driving 5-V, the HIGH-state margin is 0.4V and the LOW-state-margin is 0.4V. For 5-V driving 3.3-V, the margins are the same.

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- 3e3.75    3.76 For 2.5-V driving 3.3-V, the HIGH-state margin is 0.0V and the LOW-state-margin is 0.4V. For 3.3-V driving 2.5-V, the HIGH-state margin is 0.7V and the LOW-state-margin is 0.3V.

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- G3.276 3.78 The voltage drop across the resistor is  $5.0 - 1.6 - 0.3 = 3.1\text{V}$ , so the current is  $3.1/390 = 7.9\text{mA}$ . The power dissipated is  $3.1\text{V} \times 7.9\text{mA} = 25\text{mW}$ .

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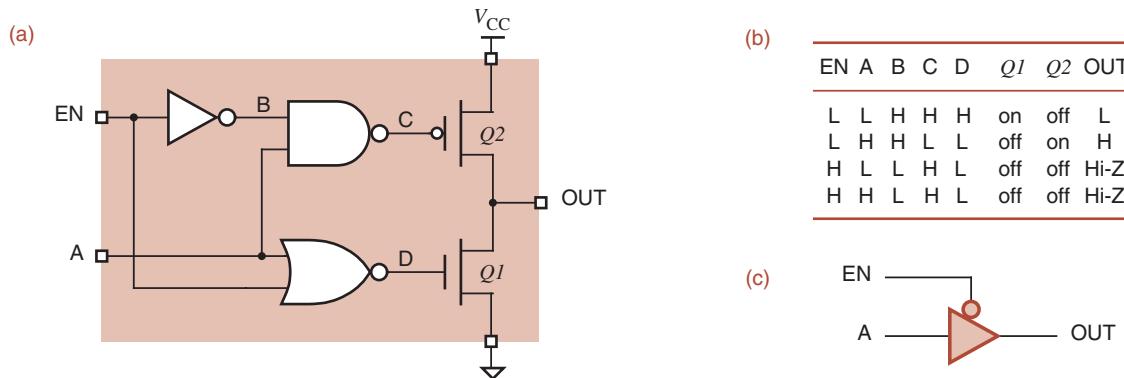
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- 3e3.77    3.79 The LSB toggles at a rate of 16 MHz. It takes two clock ticks for the LSB to complete one cycle, so the transition frequency is 8 MHz. The MSB's frequency is  $2^7$  times slower, or 62.5 KHz. The LSB's dynamic power is the most significant, but the sum of the transitions on the higher order bits, a binary series, is equivalent to almost another 8 MHz worth of transitions on a single output bit. Including the LSB, we have almost 16 MHz, but applied to the load capacitance on just a single output. If the different outputs actually have different load capacitances, then a weighted average would have to be used.

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3e3.81 3.83



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For exclusive use of adopters of the book *Digital Design Principles and Practices*, Fourth Edition, by John F. Wakerly,  
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- 3e3.95 3.86 Label the two leftmost NAND-gate outputs RS and UV, and label the topmost NAND-gate input RSUV. The output functions are

$$RS = (R \cdot S)'$$

$$UV = (U \cdot V)'$$

Without the diodes, the resistor pulls the top input of the topmost NAND gate HIGH, and its output function is

$$X = P'$$

With the diodes in place, the RSUV input is pulled LOW whenever RS or UV is LOW. Thus, the diodes perform a diode-AND function. Therefore, the new output function is

$$\begin{aligned} X &= (P \cdot RSUV)' \\ X &= (P \cdot RS \cdot UV)' \\ &= (P \cdot (R \cdot S)' \cdot (U \cdot V)') \\ &= P' + R \cdot S + U \cdot V \end{aligned}$$

The diode-AND arrangement has poor LOW-state noise margins. If we assume that the diode drop is 0.7V, and that outputs RS and UV may be as high as 0.4V in the LOW state, then a “LOW” signal at RSUV may be as high as 1.1V. This is 0.3V *higher* than the maximum voltage that is guaranteed to be recognized as a LOW .

In a practical circuit, if such a kludge is really necessary, the noise margin may be improved by using germanium or Schottky diodes, which have a lower diode drop. In any case, note that the propagation delay to the X output for input transitions that cause RSUV to go HIGH may be longer than the specified gate delays, both because of the signal delay through the diode and because of the possibly long rise time of transitions on RSUV due to passive pull up by the resistor.

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G3.299 3.87

(a) Since  $V = 3.00$  is determined by the voltage divider ratio, we can write

$$5 \cdot \left( \frac{R2}{R1 + R2} \right) = 3.00$$

$$R2 = 1.50 \cdot R1$$

At the same time, the  $R = 120\Omega$  requirement constrains  $R1$  and  $R2$  as follows:

$$R = 120\Omega$$

$$R1 \parallel R2 = 120\Omega$$

$$\frac{R1 \cdot R2}{R1 + R2} = 120\Omega$$

$$R1 \cdot \left( \frac{1 \cdot 1.50}{1 + 1.50} \right) = 120\Omega$$

$$R1 = 200\Omega$$

$$R2 = 300\Omega$$

(b) In a similar way, we find

$$R1 = 331.5\Omega$$

$$R2 = 389.1\Omega$$

This is close to the  $(330/390)\Omega$  termination often used in practice

(c)

$$R1 = 312.5\Omega$$

$$R2 = 288.5\Omega$$

(d)

$$R1 = 166.7\Omega$$

$$R2 = 71.4\Omega$$

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G3.300 3.88 For 74LS, we have

$$V_{OLmax} = 0.5V$$

$$I_{LOmax} = 8mA$$

$$V_{OHmin} = 2.7V$$

$$I_{OHmax} = -400\mu A$$

For each termination, we determine whether the current exceeds the driving gate's capability in the LOW or HIGH state

(a) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ? I_{OLmax}$$

$$\frac{3.0 - 0.5}{120} = 20.8mA > I_{OLmax}$$

So a standard 74LS gate cannot properly drive this termination.

It is worth noting that in the HIGH state, the Thévenin voltage  $V$  is higher than the required  $V_{OHmin} = 2.7V$ , so the output does not have to source *any* current in the HIGH state. However, since the LOW state requires too much sink current, overall we have to say that this gate and termination are incompatible

(b) Once again, no current is required in the HIGH state. In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq I_{OLmax}$$

$$\frac{2.7 - 0.5}{179} = 12.3mA > I_{OLmax}$$

So a standard 74LS gate cannot properly drive this termination.

(c) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ? I_{OLmax}$$

$$\frac{2.4 - 0.5}{150} = 12.7mA > I_{OLmax}$$

In the HIGH state, we compute

$$\frac{V_{OH} - V_{OL}}{R} \leq ? |I_{OHmax}|$$

$$\frac{2.7 - 2.4}{150} = 2.0mA > |I_{OHmax}|$$

So a standard 74LS gate cannot properly drive this termination in either state.

(d) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ? I_{OLmax}$$

$$\frac{1.5 - 0.5}{50} = 20.0mA > I_{OLmax}$$

In the HIGH state, we compute

$$\frac{V_{OH} - V_{OL}}{R} \leq ? |I_{OHmax}|$$

$$\frac{2.7 - 1.5}{50} = 24.0mA > |I_{OHmax}|$$

So a standard 74LS gate cannot properly drive this termination in either state.

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For 74S, we have

$$V_{OLmax} = 0.5V$$

$$I_{OLmax} = 20mA$$

$$V_{OHmin} = 2.7V$$

$$I_{OHmax} = -1000\mu A$$

For each termination, we determine whether the current exceeds the driving gate's capability in the LOW or HIGH state.

(a) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ? I_{OLmax}$$

$$\frac{3.0 - 0.5}{120} = 20.8mA > I_{OLmax}$$

While no current is required in the HIGH state (since  $V > V_{OHmin}$ ), a standard 74LS gate cannot properly drive this termination.

(b) Once again, no current is required in the HIGH state. In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ? I_{OLmax}$$

$$\frac{2.7 - 0.5}{179} = 12.3mA < I_{OLmax}$$

So a standard 74S gate *can* properly drive this termination.

(c) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ? I_{OLmax}$$

$$\frac{2.4 - 0.5}{150} = 12.7mA < I_{OLmax}$$

In the HIGH state, we compute

$$\frac{V_{OH} - V_{OL}}{R} \leq ? |I_{OHmax}|$$

$$\frac{2.7 - 2.4}{150} = 2.0mA > |I_{OHmax}|$$

So a standard 74LS gate cannot properly drive this termination.

(d) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ? I_{OLmax}$$

$$\frac{1.5 - 0.5}{50} = 20.0mA = I_{OLmax}$$

In the HIGH state, we compute

$$\frac{V_{OH} - V_{OL}}{R} \leq ? |I_{OHmax}|$$

$$\frac{2.7 - 1.5}{50} = 24.0mA > |I_{OHmax}|$$

So a standard 74S gate cannot properly drive this termination in the HIGH state.

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For 74FCT-T, we have

$$V_{OLmax} = 0.55V$$

$$I_{OLmax} = 64mA$$

$$V_{OHmin} = 2.4V$$

$$I_{OHmax} = -15mA$$

For each termination, we determine whether the current exceeds the driving gate's capability in the LOW or HIGH state.

(a) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ?I_{OLmax}$$

$$\frac{3.0 - 0.55}{120} = 20.4mA < I_{OLmax}$$

No current is required in the HIGH state (since  $V > V_{OHmin}$ ), so a standard 74FCT-T gate *can* properly drive this termination in either state.

(b) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ?I_{OLmax}$$

$$\frac{2.7 - 0.55}{179} = 12.0mA < I_{OLmax}$$

No current is required in the HIGH state (since  $V > V_{OHmin}$ ), so a standard 74FCT-T gate *can* properly drive this termination in either state.

(c) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ?I_{OLmax}$$

$$\frac{2.4 - 0.55}{150} = 12.3mA < I_{OLmax}$$

No current is required in the HIGH state (since  $V = V_{OHmin}$ ), so a standard 74FCT-T gate *can* properly drive this termination in either state.

(d) In the LOW state, we compute

$$\frac{V - V_{OL}}{R} \leq ?I_{OLmax}$$

$$\frac{1.5 - 0.55}{50} = 19.0mA < I_{OLmax}$$

In the HIGH state, we compute

$$\frac{V_{OH} - V_{OL}}{R} \leq ?|I_{OHmax}|$$

$$\frac{2.4 - 1.5}{50} = 18.0mA > |I_{OHmax}|$$

Since this exceeds the output specification in the HIGH state, a standard 74FCT-T gate cannot properly drive the termination.

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- G3.303 3.89 The longest name that we could find was 74ALVCHG162280 (14 characters), for when you need a 16-to-32 bit Registered Bus Exchanger with byte masks and 3-state outputs.

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3e4.1 4.1 FAILURE' · DESIGNER · STUDIED' + NERD · STUDIED

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3e4.2

4.2

T2:

X	X + 1	=	1
0	1	=	1
1	1	=	1

T4:

X	X'	(X')'	=	X'
0	1	0	=	0
1	0	1	=	1

T3:

X	X + X	=	X
0	0	=	0
1	1	=	1

T5:

X	X'	X + X'	=	1
0	1	1	=	1
1	0	1	=	1

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3e4.3 4.3

T1'			
X	X·1	=	X
0	0	=	0
1	1	=	1
T3'			
X	X·X	=	X
0	0	=	0
1	1	=	1

T2'				
X	X·0	=	0	
0	0	=	0	
1	0	=	0	
T5'				
X	X'	X·X'	=	0
0	1	0	=	0
1	0	0	=	0

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3e4.4 4.4

T6					T9					
X	Y	X + Y	=	Y + X	X	Y	X · Y	X + X · Y	=	Y + X
0	0	0	=	0	0	0	0	0	=	0
0	1	1	=	1	0	1	0	0	=	0
1	0	1	=	1	1	0	0	1	=	1
1	1	1	=	1	1	1	1	1	=	1

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- G4.205 4.5 The original expression assumes precedence of · over + , that is, the expression is  $(W \cdot X) + (Y \cdot Z)$  . The parenthesization must be retained for the correct result,  $(W' + X') \cdot (Y' + Z')$ , or the precedence must be swapped.

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G4.206 4.6 The answers for parts (a), (b), (c) are as follows.

$$\begin{aligned} & W \cdot X \cdot Y \cdot Z \cdot (W \cdot X \cdot Y \cdot Z' + W \cdot X' \cdot Y \cdot Z + W' \cdot X \cdot Y \cdot Z + W \cdot X \cdot Y' \cdot Z) \\ &= W \cdot X \cdot Y \cdot Z \cdot W \cdot X \cdot Y \cdot Z' + W \cdot X \cdot Y \cdot Z \cdot W \cdot X' \cdot Y \cdot Z \\ &\quad + W \cdot X \cdot Y \cdot Z \cdot W' \cdot X \cdot Y \cdot Z + W \cdot X \cdot Y \cdot Z \cdot W \cdot X \cdot Y' \cdot Z \quad (\text{T8}) \\ &= 0 + 0 + 0 + 0 \quad (\text{T6}', \text{T5}', \text{T2}') \\ &= 0 \quad (\text{A4}') \end{aligned}$$

$$\begin{aligned} & A \cdot B + A \cdot B \cdot C' \cdot D + A \cdot B \cdot D \cdot E' + A' \cdot B \cdot C' \cdot E + A' \cdot B' \cdot C' \cdot E \\ &= A \cdot B + A \cdot B \cdot D \cdot E' + A' \cdot B \cdot C' \cdot E + A' \cdot B' \cdot C' \cdot E \quad (\text{T9}) \\ &= A \cdot B + A' \cdot B \cdot C' \cdot E + A' \cdot B' \cdot C' \cdot E \quad (\text{T9}) \\ &= A \cdot B + A' \cdot C' \cdot E \quad (\text{T10}) \end{aligned}$$

$$\begin{aligned} & M \cdot R \cdot P + Q \cdot O' \cdot R' + M \cdot N + Q \cdot P \cdot M \cdot O' + O \cdot N \cdot M \\ &= M \cdot R \cdot P + Q \cdot O' \cdot R' + Q \cdot P \cdot M \cdot O' + M \cdot N + O \cdot N \cdot M \quad (\text{T6}) \\ &= M \cdot R \cdot P + Q \cdot O' \cdot R' + Q \cdot P \cdot M \cdot O' + M \cdot N \quad (\text{T9}) \\ &= R \cdot (M \cdot P) + R' \cdot (Q \cdot O') + (M \cdot P) \cdot (Q \cdot O') + M \cdot N \quad (\text{T6}', \text{T7}') \\ &= R \cdot (M \cdot P) + R' \cdot (Q \cdot O') + M \cdot N \quad (\text{T11}) \\ &= R \cdot M \cdot P + R' \cdot Q \cdot O' + M \cdot N \quad (\text{T7}') \end{aligned}$$

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G4.207	4.7	(a)	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><th>X</th><th>Y</th><th>Z</th><th>F</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	Y	Z	F	0	0	0	0	(b)	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><th>W</th><th>X</th><th>Y</th><th>Z</th><th>F</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr></table>	W	X	Y	Z	F	0	0	0	0	1	(c)	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><th>W</th><th>X</th><th>Y</th><th>Z</th><th>F</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	W	X	Y	Z	F	0	0	0	0	0	(d)	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>F</th><th>+</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	A	B	C	D	F	+	0	0	0	0	0	0
X	Y	Z	F																																														
0	0	0	0																																														
W	X	Y	Z	F																																													
0	0	0	0	1																																													
W	X	Y	Z	F																																													
0	0	0	0	0																																													
A	B	C	D	F	+																																												
0	0	0	0	0	0																																												
			0 0 0 0	0 0 0 0 1	0 0 0 0 0		0 0 0 0 0		0 0 0 0 0																																								
			0 0 1 1	0 0 0 1 1	0 0 0 1 0		0 0 0 1 0		0 0 0 1 0																																								
			0 1 0 1	0 0 1 0 0	0 0 1 0 0		0 0 1 0 0		0 0 1 0 1																																								
			0 1 1 1	0 0 1 1 1	0 0 1 1 0		0 0 1 1 1		0 0 1 1 1																																								
			1 0 0 0	0 1 0 0 1	0 1 0 0 1		0 1 0 0 0		0 1 0 0 0																																								
			1 0 1 0	0 1 0 1 1	0 1 0 1 1		0 1 0 1 0		0 1 0 1 0																																								
			1 1 0 0	0 1 1 0 1	0 1 1 0 1		0 1 1 0 1		0 1 1 0 1																																								
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			<u>1 1 1 0</u>	<u>1 0 0 0 1</u>	<u>1 0 0 0 1</u>		<u>1 0 0 0 1</u>		<u>1 0 0 0 1</u>																																								
				1 0 0 1 1	1 0 0 1 1		1 0 0 1 1		1 0 0 1 1																																								
				1 0 1 0 0	1 0 1 0 0		1 0 1 0 0		1 0 1 0 1																																								
				1 0 1 1 1	1 0 1 1 1		1 0 1 1 1		1 0 1 1 1																																								
				1 1 0 0 1	1 1 0 0 1		1 1 0 0 0		1 1 0 0 0																																								
				1 1 0 1 0	1 1 0 1 1		1 1 0 1 0		1 1 0 1 0																																								
				1 1 1 0 0	1 1 1 0 0		1 1 1 0 0		1 1 1 0 1																																								
				1 1 1 1 0	1 1 1 1 1		1 1 1 1 1		1 1 1 1 0																																								
			<u>1 1 1 1 0</u>	<u>1 1 1 1 1</u>	<u>1 1 1 1 1</u>		<u>1 1 1 1 1</u>		<u>1 1 1 1 0</u>																																								

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(e)	V	W	X	Y	Z	F
0	0	0	0	0	0	0
0	0	0	0	1	0	
0	0	0	1	0	0	
0	0	0	1	1	0	
0	0	1	0	0	0	
0	0	1	0	1	1	
0	0	1	1	1	0	
0	0	1	1	1	1	
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1	1	1	0	1	1	
1	1	1	1	0	0	
1	1	1	1	1	0	

(f)	A	B	C	D	E	F
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0	0	0	0	0	1	1
0	0	0	1	0	0	1
0	0	0	1	1	1	1
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1	1	1	0	0	0	0
1	1	1	0	1	1	0
1	1	1	1	0	0	0
1	1	1	1	1	1	0

(g)	W	X	Y	Z	F
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
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1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	1	1	1

(i)	A	B	C	D	F
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	1
0	1	1	1	1	1
1	1	1	1	1	1

((h))

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

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G4.209 4.9

(a)  $F = X' \cdot Y + Y' \cdot X = (X + Y) \cdot (X' + Y')$

(b)  $F = A \cdot B = (A + B) \cdot (A + B') \cdot (A' + B)$

(c)  $F = A' \cdot B' \cdot C + A' \cdot B \cdot C' + A \cdot B' \cdot C' + A \cdot B \cdot C$   
 $= (A + B + C) \cdot (A + B' + C') \cdot (A' + B + C') \cdot (A' + B' + C')$

(d)  $F = W' \cdot X \cdot Y' + W \cdot X' \cdot Y' + W \cdot X' \cdot Y$   
 $= (W + X + Y) \cdot (W + X' + Y) \cdot (W + X' + Y') \cdot (W' + X' + Y) \cdot (W' + X' + Y')$

(e)  $F = X' \cdot Y' \cdot Z' + X' \cdot Y' \cdot Z + X' \cdot Y \cdot Z' + X' \cdot Y \cdot Z + X \cdot Y \cdot Z = (X' + Y + Z) \cdot (X' + Y + Z') \cdot (X' + Y' + Z)$

(f)  $F = V' \cdot W' \cdot X' + V' \cdot W' \cdot X + V' \cdot W \cdot X + V \cdot W' \cdot X' + V \cdot W' \cdot X + V \cdot W \cdot X' + V \cdot W \cdot X = (V + W' + X)$

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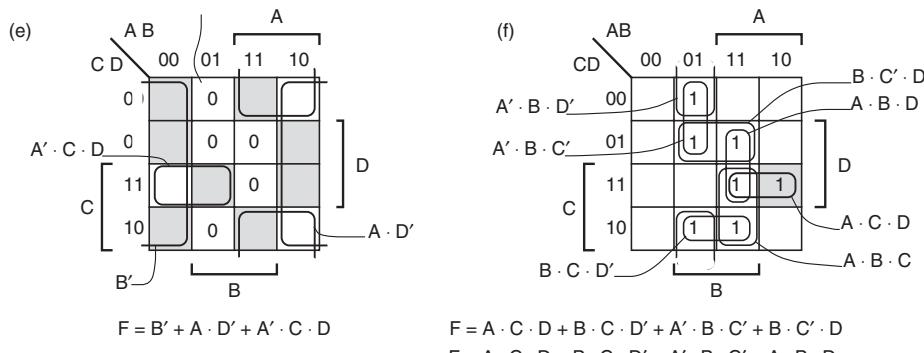
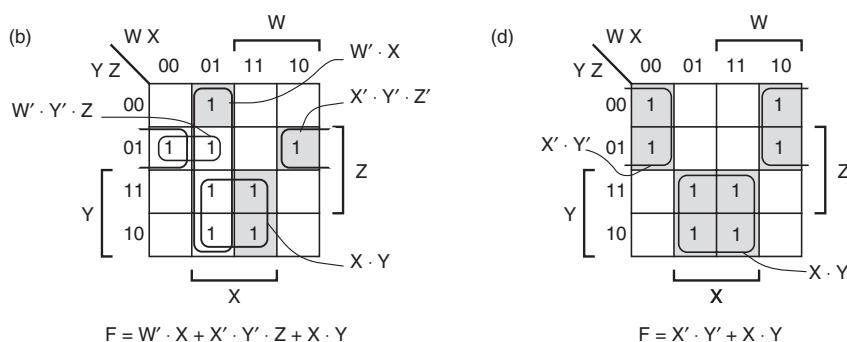
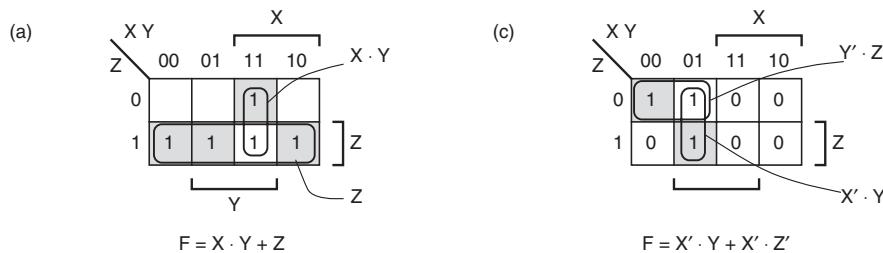
- 3e4.11    4.12 Each product term of a canonical sum has  $n$  literals, regardless of whether or not the canonical sum happens to be a minimal sum. However, if the canonical sum is a minimal sum, there can be no other minimal sum. Another minimal sum would have to have the same number of product terms, each with  $n$  literals. But since  $n$ -literal product terms (minterms) correspond exactly to the 1s of the logic function, such a minimal sum would cover a different set of 1s and therefore could not be the same logic function.

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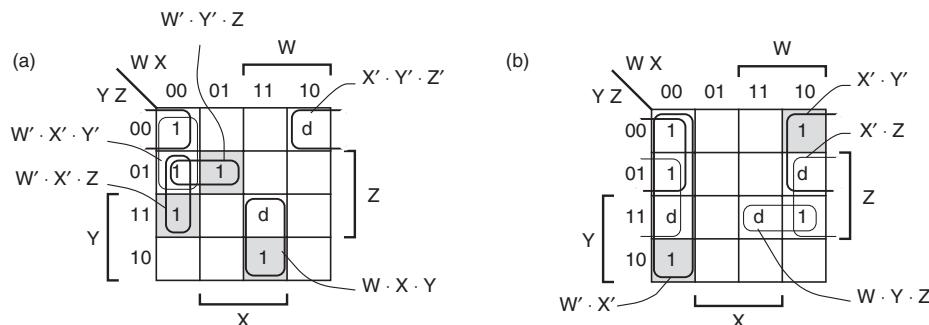
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- 3e4.12 4.13 (1) Including inverters makes the problem too difficult. (2) In modern PLD-based designs, inverters do cost nothing and really can be ignored.

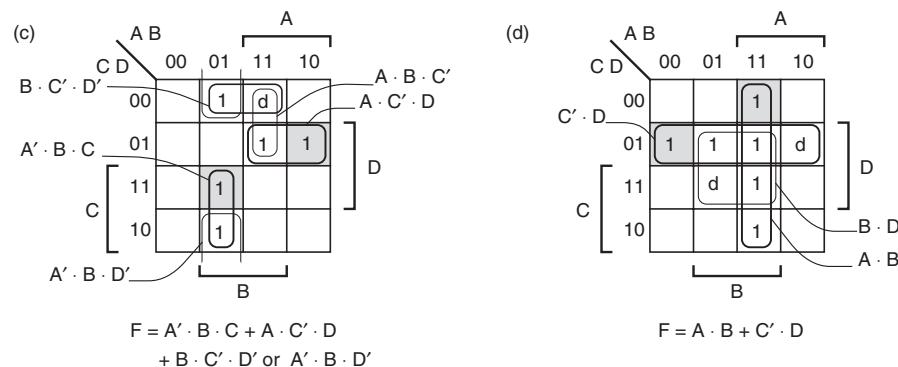
G4.213 4.14



G4.219 4.18

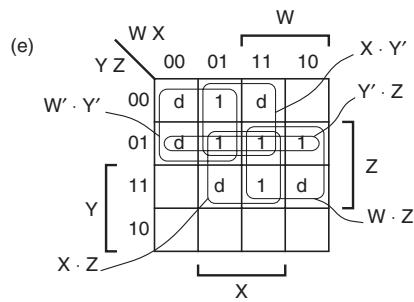


$$F = W' \cdot Y' \cdot Z + W' \cdot X' \cdot Z + W \cdot X \cdot Y + W' \cdot X' \cdot Y' \text{ or } X' \cdot Y' \cdot Z'$$



$$F = A' \cdot B \cdot C + A \cdot C' \cdot D + B \cdot C' \cdot D' \text{ or } A' \cdot B \cdot D'$$

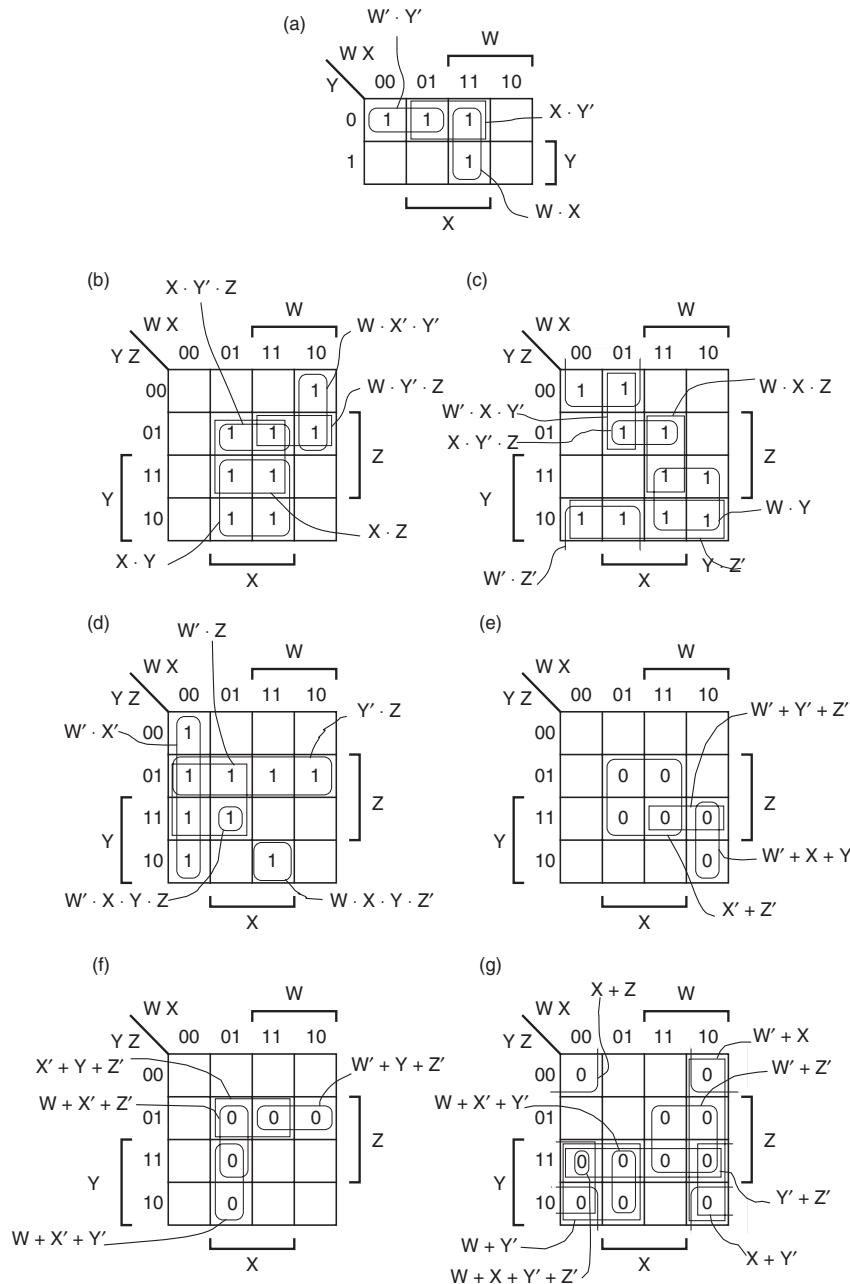
$$F = A \cdot B + C' \cdot D$$



$$F = X \cdot Y' + W \cdot Z$$

G4.222

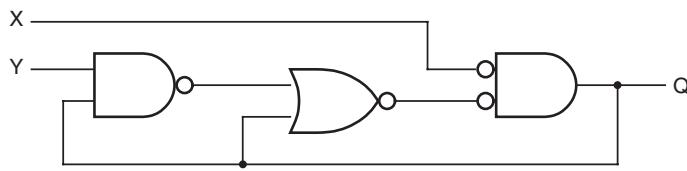
- 4.19** Consensus terms that must be added to cover the hazards are “circled” with rectangles. In (d), the  $W' \cdot X \cdot Y \cdot Z$  term may be eliminated in the hazard-free design. In (g), terms  $W + X' + Y'$  and  $W + X + Y' + Z'$  may be eliminated in the hazard-free design.



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3e4.28 4.20



Analyzing this circuit with the standard method for feedback sequential circuits (Section 5.5), we get the following excitation equation:

$$\begin{aligned} Q^* &= X' \cdot ((Y \cdot Q)' + Q) \\ &= X' \cdot (Y' + Q' + Q) \\ &= X' \cdot 1 = X' \end{aligned}$$

Thus,  $Q^*$  is a function of  $X$  alone, and is independent of the circuit's previous "state."

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3e4.29 4.21

$$\begin{aligned} X \cdot 1 &= X \text{ (T1')} \\ X \cdot (Y + Y') &= X \text{ (T5)} \\ X \cdot Y + X \cdot Y' &= X \text{ (T8)} \end{aligned}$$

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3e4.30 4.22

$$X \cdot Y + X' \cdot Z = X \cdot Y + X' \cdot Z + Y \cdot Z \text{ (T11)}$$

$$Y \cdot X + Y' \cdot X = Y \cdot X + Y' \cdot X + X \cdot X \text{ (rename } X \rightarrow Y \text{ and } Y, Z \rightarrow X\text{)}$$

$$\begin{aligned} X \cdot Y + X \cdot Y' &= X \cdot Y + X \cdot Y' + X \text{ (T6' } \times 4, \text{ T3')} \\ &= X \text{ (T9 } \times 2) \end{aligned}$$

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3e4.31 4.23

$$\begin{aligned}(X + Y') \cdot Y &= X \cdot Y + Y' \cdot Y \text{ (T8)} \\ &= X \cdot Y + Y \cdot Y' \text{ (T6')} \\ &= X \cdot Y + 0 \text{ (T5')} \\ &= X \cdot Y \text{ (T1)}\end{aligned}$$

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3e4.32 4.24

$$\begin{aligned}(X + Y) \cdot (X' + Z) &= (X + Y) \cdot X' + (X + Y) \cdot Z \quad (\text{T8}) \\&= X' \cdot (X + Y) + Z \cdot (X + Y) \quad (\text{T6}' \times 2) \\&= X' \cdot X + X' \cdot Y + Z \cdot X + Z \cdot Y \quad (\text{T8} \times 2) \\&= 0 + X' \cdot Y + X \cdot Z + Y \cdot Z \quad (\text{T5}', \text{T6}' \times 2) \\&= X' \cdot Y + X \cdot Z + Y \cdot Z \quad (\text{T1}) \\&= X' \cdot Y + X \cdot Z \quad (\text{T11})\end{aligned}$$

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G4.233 4.25 To answer this problem rigorously, we must make a formal definition of an  $n$ -input OR function:

$$\begin{aligned}\text{OR}(X_1, X_2, X_3, \dots, X_{n-1}, X_n) &= 0 \text{ if all } X_j \text{'s are 0} \\ &= 1 \text{ otherwise}\end{aligned}$$

Then we can show by finite induction that

$$\text{OR}(X_1, X_2, X_3, \dots, X_{n-1}, X_n) = X_n + (X_{n-1} + (\dots + (X_3 + (X_2 + X_1))\dots))$$

The right-hand side uses  $n-1$  binary OR operators, corresponding to  $n-1$  2-input OR gates.

In the proof, the basis step ( $n=2$ ) is obvious—a 2-input OR function requires  $2-1=1$  2-input OR gate. For the induction step, we write an  $n$ -input OR function as follows:

$$\text{OR}(X_1, X_2, X_3, \dots, X_{n-1}, X_n) = X_n + \text{OR}(X_1, X_2, X_3, \dots, X_{n-1})$$

This expression is valid, since the right-hand side is 1 if and only if all of the  $X_i$ 's are 1. Substituting the expression for an  $(n-1)$ -input AND (which is assumed valid in this step), we get the desired result:

$$\text{OR}(X_1, X_2, X_3, \dots, X_{n-1}, X_n) = X_n + (X_{n-1} + (\dots + (X_3 + (X_2 + X_1))\dots))$$

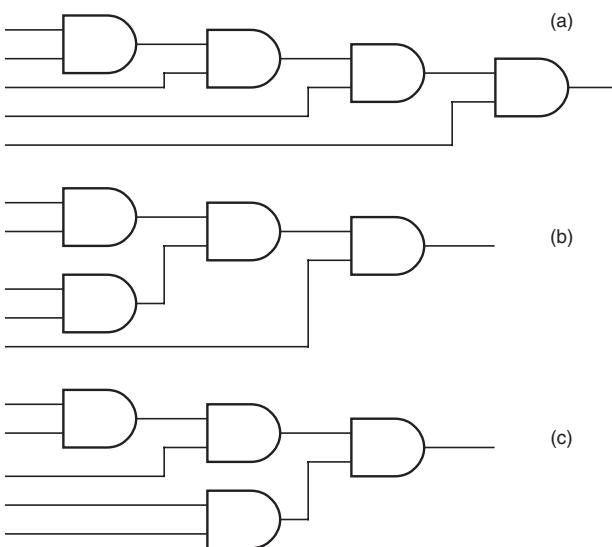
NOR gates cannot be expanded in this way, since extra inverters are needed to undo and redo the NOR's inversion. To prove this result formally, use a counterexample—show that no possible interconnection of two 2-input NOR gates (there are only a few) performs a 3-input NOR function.

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3e4.34

- 4.26 There are three possible patterns for interconnecting four 2-input AND gates, shown in the figure to the right. For each pattern, there are  $4!$  ways to assign a physical gate to a position in the pattern. If a gate's inputs include both a primary input and another gate's output, there are two ways to choose which is which. Thus, there are  $4! \cdot 2^3$  ways to get a 5-input AND function according to pattern (a),  $4! \cdot 2^2$  according to (b), and  $4! \cdot 2^2$  according to (c), a total of 336 ways. Finally, for each such 5-input AND function, there are  $5!$  different ways to assign V, W, X, Y, and Z to the inputs, so the final total is 40,320.



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3e4.35 4.27

$$\begin{aligned} X_1 \cdot X_2 \cdot \dots \cdot X_n &= X_1 \cdot X_2 \cdot \dots \cdot (X_n \cdot X_n) \text{ (T6', T7' as required)} \\ &= X_1 \cdot X_2 \cdot \dots \cdot X_n \text{ (T3')} \\ X_1 + X_2 + \dots + X_n + X_n &= X_1 + X_2 + \dots + (X_n + X_n) \text{ (T6, T7 as required)} \\ &= (X_1 + X_2 + \dots + X_n) \text{ (T3)} \end{aligned}$$

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- 3e4.36 4.28** In order to prove T13, we first use perfect induction in the basis step to prove the  $n=2$  case  $[(X_1 \cdot X_2)' = X_1' + X_2']$ , as shown in the table to the right.

In the induction step, we assume that the theorem is true for  $n$ , and prove that it's true for  $n+1$ :

$X_1$	$X_2$	$X_1'$	$X_2'$	$X_1 \cdot X_2$	$(X_1 \cdot X_2)'$	$=$	$X_1' + X_2'$
0	0	1	1	0	1	=	1
0	1	1	0	0	1	=	1
1	0	0	1	0	1	=	1
1	1	0	0	1	0	=	0

$$\begin{aligned}
 (X_1 \cdot X_2 \cdot \dots \cdot X_n \cdot X_{n+1}) &= X_1 \cdot X_2 \cdot \dots \cdot (X_n \cdot X_{n+1}) \quad (\text{T6}', \text{T7}' \text{ as required}) \\
 &= X_1' + X_2' + \dots + (X_n \cdot X_{n+1})' \quad (\text{since true for } n) \\
 &= X_1' + X_2' + \dots + X_n' + X_{n+1}' \quad (\text{since true for } n = 2)
 \end{aligned}$$

The proof of  $T13'$  is just the dual of the foregoing.

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3e4.37 4.29 Figure 3–4(d) is more appropriate, since electrically a TTL NOR gate is just the wired-AND of inverters.

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3e4.38 4.30

$$\begin{aligned} & B' \cdot C + A \cdot C \cdot D' + A' \cdot C + E \cdot B' + E \cdot (A + C) \cdot (A' + D') \\ &= B' \cdot C + B' \cdot E + A \cdot D' \cdot C + A' \cdot C + E \cdot (A + C) \cdot (A' + D') \text{ (T6, T6', T7, T7')} \\ &= B' \cdot (C + E) + (A \cdot D' + A') \cdot C + E \cdot (A + C) \cdot (A' + D') \text{ (T8)} \\ &= B' \cdot (C + E) + (D' + A') \cdot C + E \cdot (A + C) \cdot (A' + D') \text{ (T11, T9)} \\ &= B' \cdot (C + E) + (C + E \cdot (A + C)) \cdot (A' + D') \text{ (T8, etc)} \\ &= B' \cdot (C + E) + (C + E \cdot (A + C)) \cdot (A \cdot D)' \text{ (T11)} \end{aligned}$$

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- 3e4 . 40    4.31 One method is based on splitting the truth table into  $X_1 = 0$  and  $X_1 = 1$  portions, and constructing the function. An algebraic method is described below.

Any function  $F(X_1, \dots, X_n)$  can be written as a sum of products. Eliminating redundant terms ( $X \cdot X' = 0$ , etc.) and factoring out  $X_1$  and  $X_1'$ , we can write  $F$  as follows:

$$F = X_1 \cdot G_1 + X_1' \cdot G_2 + G_3$$

where

$G_1$ ,  $G_2$ , and  $G_3$  are functions of  $X_2 \dots X_n$ . Then

$$\begin{aligned} F(0, X_2, \dots, X_n) &= 0 \cdot G_1 + 1 \cdot G_2 + G_3 \\ &= G_2 + G_3 \end{aligned}$$

$$\begin{aligned} F(1, X_2, \dots, X_n) &= 1 \cdot G_1 + 0 \cdot G_2 + G_3 \\ &= G_1 + G_3 \end{aligned}$$

and

$$\begin{aligned} X_1 \cdot F(0, X_2, \dots, X_n) + X_1' \cdot F(1, X_2, \dots, X_n) &= X_1 \cdot (G_2 + G_3) + X_1' \cdot (G_1 + G_3) \\ &= X_1 \cdot G_1 + X_1 \cdot G_3 + X_1' \cdot G_2 + X_1' \cdot G_3 \\ &= X_1 \cdot G_1 + X_1' \cdot G_2 + (X_1 + X_1') \cdot G_3 \\ &= X_1 \cdot G_1 + X_1' \cdot G_2 + G_3 \\ &= F(X_1, X_2, \dots, X_n) \end{aligned}$$

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3e4.41 4.32

$$\begin{aligned}F(X_1, \dots, X_i, X_{i+1}, \dots, X_n) &= X'_1 \cdot \dots \cdot X'_i \cdot F(0, \dots, 0, X_{i+1}, \dots, X_n) \\&\quad + X'_1 \cdot \dots \cdot X'_i \cdot F(0, \dots, 1, X_{i+1}, \dots, X_n) \\&\quad \dots \\&\quad + \underbrace{X'_1 \cdot \dots \cdot X'_i}_{2^i \text{ minterms}} \cdot F(\underbrace{1, \dots, 1}_{2^i \text{ combs}}, X_{i+1}, \dots, X_n)\end{aligned}$$

A dual theorem may be written based on maxterms.

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- 3e4.42 4.33 Let  $i=n$  above. We get  $n$ -variable minterms, each AND'ed with 1 or 0 (to include or exclude) depending on the value of  $F$  for each input combination. This is the canonical sum. The canonical product results if we start with the dual theorem.

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3e4.39 4.34

(a) True. If  $A \cdot B = 0$  then either  $A = 0$  or  $B = 0$ . If  $A + B = 1$  then either  $A = 1$  or  $B = 1$ . Therefore,  $A, B = 0, 1$  or  $1, 0$ , and  $A = B'$ .

(b) True. We prove that  $X = Y'$  for every input combination, using the same reasoning as in (a).

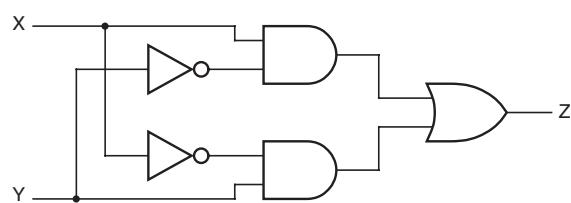
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3e4.43 4.35

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

$$Z = X' \cdot Y + X \cdot Y'$$



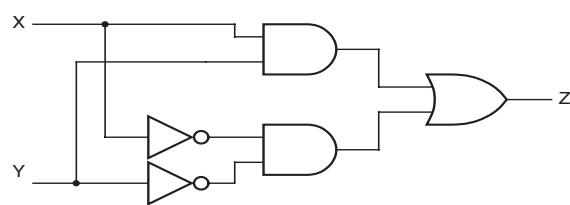
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G4.243 4.36

X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	1

$$Z = X \cdot Y + X' \cdot Y'$$



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- G4.244 4.37 According to switching algebra, the output is always one. However, it may “glitch” on 0-to-1 or 1-to-0 input transitions, because of unequal delays through internal paths.

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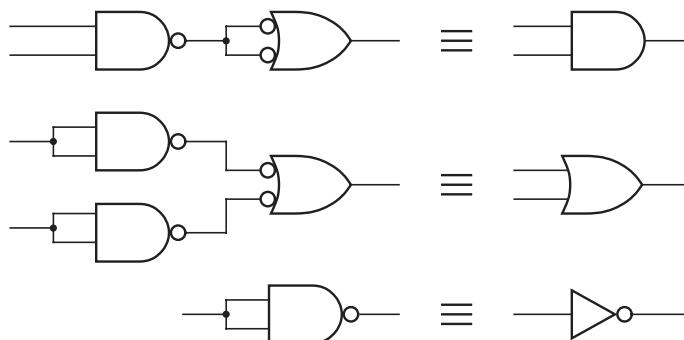
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- G4.245 4.38 An inverter function can be obtained by tying one input of the XNOR gate to logic 0 (LOW) and using the remaining input and output.

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- 3e4.46 4.39 Yes, 2-input NAND gates form a complete set of logic gates. We prove the result in the figure on the right by showing that these gates can be used to make 2-input AND gates, 2-input OR gates, and inverters, which form a complete set.

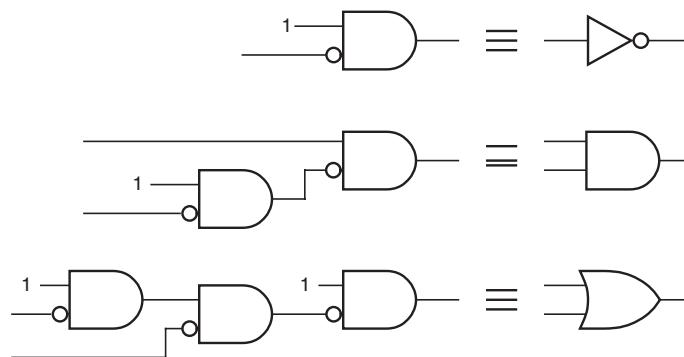


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G4.247

- 4.40 Yes, the 2-input “inhibit” AND gates form a complete set of logic gates. We prove the result in the figure on the right by showing that these gates can be used to make 2-input AND gates, 2-input OR gates, and inverters, which form a complete set. They are called “inhibit” gates because applying a 1 to the inverted input stops the signal on the other input from being copied to the output, which is then always 0. The last question is just another one of George’s wisecracks.



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- G4.248 4.41 No, 2-input XNOR gates do not form a complete set. The only things we can do are tie inputs together, yielding  $F = 1$ , and tie an input LOW or HIGH, yielding  $F = X'$  or  $F = X$ . We can make an inverter but no AND or OR.

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- 3e4.50 4.42 Y1 is 1 if A1 and B1 are both 1  
*but* A2 and B2 are not both 1; Y2  
is defined symmetrically.

A1	B1	A2	B2	Y1	Y2	A1	B1	A2	B2	Y1	Y2
0	0	0	0	0	0	1	0	0	0	0	0
0	0	0	1	0	0	1	0	0	1	0	0
0	0	1	0	0	0	1	0	1	0	0	0
0	0	1	1	0	1	1	0	1	1	0	1
0	1	0	0	0	0	1	1	0	0	1	0
0	1	0	1	0	0	1	1	0	1	1	0
0	1	1	0	0	0	1	1	1	0	1	0
0	1	1	1	0	1	1	1	1	1	0	0

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- G4.253 4.44 Consider the structure of the truth table for an  $n$ -variable function; it has  $2^n$  rows. Each row can specify the function's value as 0 or 1. Thus, there are  $2^{2^n}$  different ways to fill in the truth table, and  $2^{2^n}$  different  $n$ -variable functions. If we want just the functions using all  $n$ -variables, we need to eliminate all of the logic functions of  $n - 1$  variables, and the result is  $2^{2^n} - 2^{2^{n-1}}$ .

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- G4.254 4.45 Consider the structure of the truth table for an  $n$ -variable function; it has  $2^n$  rows. Each row can specify the function's value as 0 or 1. Thus, there are  $2^{2^n}$  different ways to fill in the truth table, and  $2^{2^n}$  different  $n$ -variable functions. So, there are 256 different functions of 3 variables, as shown in the first table below. However, we are given the restriction that in normally occurring input combinations, at least two of the variables must be 1. So we are only interested in the four input combinations shown in the second table below. Thus, there are only 16 possible functions that are "different" for these 16 input combinations. Considering the 16 ways to fill in the truth table, we may enumerate 16 representative functions as shown in the third table below.

Note that each "representative" function was derived assuming that its output for each of the four unused input combinations is 0. For each "representative" function, there are 15 other functions that give different outputs for the unused input combinations. In many cases, a simpler representative function could have been chosen; for example, the eight function is just a 3-input NAND gate if the outputs for the unused input combinations are assumed to all be 1.

X	Y	Z	F
0	0	0	$F_0$
0	0	1	$F_1$
0	1	0	$F_2$
0	1	1	$F_3$
1	0	0	$F_4$
1	0	1	$F_5$
1	1	0	$F_6$
1	1	1	$F_7$

X	Y	Z	F
0	1	1	$F_3$
1	0	1	$F_5$
1	1	0	$F_6$
1	1	1	$F_7$

$F_7$	$F_6$	$F_5$	$F_3$	F	$F_7$	$F_6$	$F_5$	$F_3$	F
0	0	0	0	0	1	0	0	0	$X \cdot Y \cdot Z$
0	0	0	1	$X' \cdot Y \cdot Z$	1	0	0	1	$Y \cdot Z$
0	0	1	0	$X \cdot Y' \cdot Z$	1	0	1	0	$X \cdot Z$
0	0	1	1	$X' \cdot Y \cdot Z + X \cdot Y' \cdot Z$	1	0	1	1	$X \cdot Z + Y \cdot Z$
0	1	0	0	$X \cdot Y \cdot Z'$	1	1	0	0	$X \cdot Y$
0	1	0	1	$X \cdot Y \cdot Z' + X' \cdot Y \cdot Z$	1	1	0	1	$X \cdot Y + Y \cdot Z$
0	1	1	0	$X \cdot Y \cdot Z' + X \cdot Y' \cdot Z$	1	1	1	0	$X \cdot Y + X \cdot Z$
0	1	1	1	$X \cdot Y \cdot Z' + X \cdot Y' \cdot Z + X' \cdot Y \cdot Z$	1	1	1	1	1

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3e4.52    4.46 Take the dual, “multiply out,” and take the dual again. The result is the same as “adding out.”

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G4.255 4.47 To get students onto the right track, the exercises on self-dual functions should be preceded by a new exercise:

Prove that  $F^D(X_1, X_2, \dots, X_n) = [F(X'_1, X'_2, \dots, X'_n)']$ . [Solution: Swap  $X_i$  and  $X'_i$  in the generalized DeMorgan's theorem.]

Now, the answers to the current exercise:

- (a) Self-dual, since  $F^D = X = F$ .
- (b) Not self-dual, since

$$\begin{aligned} F &= X' \cdot Y' \cdot Z + X' \cdot Y \cdot Z' + X \cdot Y' \cdot Z + X \cdot Y \cdot Z \\ F^D &= (X' + Y' + Z) \cdot (X' + Y + Z') \cdot (X + Y' + Z) \cdot (X + Y + Z) \\ &= \prod_{X, Y, Z} (6, 5, 2, 0) \neq \sum_{X, Y, Z} (1, 2, 5, 7) = F \end{aligned}$$

- (c) Self-dual, since

$$F^D = (X' + Y + Z') \cdot (X + Y' + Z') \cdot (X + Y) = (X \cdot Y + X \cdot Z' + Y \cdot Z') = F$$

- (d) Self-dual, since

$$\begin{aligned} F^D &= [W + (X \oplus Y \oplus Z \oplus W')] \cdot (X \oplus Y \oplus Z)^D \\ &= W \cdot (X \oplus Y \oplus Z)^D + (W' \oplus X \oplus Y \oplus Z)^D \cdot (X \oplus Y \oplus Z)^D \end{aligned}$$

But  $X \oplus Y \oplus Z = \sum_{X, Y, Z} (0, 3, 5, 6)$ , which is self-dual from (b). Therefore,

$$F^D = W \cdot (X \oplus Y \oplus Z)' + W' \cdot (X \oplus Y \oplus Z) \neq F$$

- (e) Not self-dual. Consider an input combination  $I$  with three 1s. Then  $F(I) = 1$  and  $F(I') = 1$ ;  $F(I) \neq F(I)'$  for some input combination, so the function is not self-dual.
- (f) Self-dual. Let  $I$  be an input combination such that  $F$  is 1, that is,  $I$  has five or more 1s. Then the complement of that input combination, denoted  $I'$ , has four or fewer 1s, and  $F(I') = 0 = F(I)'$ . Similarly, if  $I$  has four or fewer 1s, then  $I'$  has five or more 1s, and  $F(I') = 1 = F(I)'$ . Thus, for any input combination  $I$ ,  $F(I) = F(I)' = F^D(I)$ , and  $F$  is self-dual.

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- 3e4.56 4.48** According to the “extra” exercise in preceding solution, we need  $F(I) = F(I')$  for all input combinations  $I$ . Consider a general  $n$ -variable truth table, and divide it in half:

$X_1$	$X_2$	...	$X_n$	$F$
0	0	...	0	$F_0$
0	0	...	1	$F_1$
		...		...
0	1	...	1	$F_{2^{n-1}-1}$
<hr/>				
1	0	...	0	$F_{2^{n-1}}$
1	0	...	1	$F_{2^{n-1}+1}$
		...		...
1	1	...	1	$F_{2^n-1}$

The function is self-dual if the values of  $F_{2^{n-1}}, F_{2^{n-1}+1}, \dots, F_{2^n-1}$  are the opposite of  $F_0, F_1, \dots, F_{2^{n-1}-1}$  and in the opposite order.

There are  $2^{2^{n-1}}$  possible assignments of 0s and 1s to  $F_0, F_1, \dots, F_{2^{n-1}-1}$ , and for each one there is a corresponding self-dual  $n$ -variable logic function.

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3e4.57 4.49 Note that  $(G^D)^D = G$ .

$$\begin{aligned}F^D &= [X_1 + G^D(X_2, \dots, X_n)] \cdot [X_1' + G(X_2, \dots, X_n)] \\&= X_1 \cdot G(X_2, \dots, X_n) + X_1' \cdot G^D(X_2, \dots, X_n) + G(X_2, \dots, X_n) \cdot G^D(X_2, \dots, X_n) \\&= X_1 \cdot G(X_2, \dots, X_n) + X_1' \cdot G^D(X_2, \dots, X_n) \text{ (consensus)} \\&= F\end{aligned}$$

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3e4 . 58    4.50 (a) 16 ns. (c) 18 ns. (d) 10 ns.

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- 3e4.62 4.51 For the function  $F(X_1, \dots, X_i, X_{i+1}, \dots, X_n)$  let us assume without loss of generality that the first  $i$  variables,  $X_1, \dots, X_i$  are the ones that take on all  $2^i$  possible combinations within the set of  $2^i$  1-cells. Then the canonical sum for those 1-cells may be written as follows:

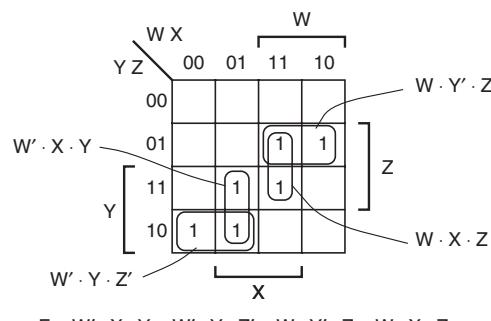
$$\begin{aligned} S = & X_1' \cdot \dots \cdot X_i' \cdot P(X_{i+1}, \dots, X_n) \\ & + X_1' \cdot \dots \cdot X_i \cdot P(X_{i+1}, \dots, X_n) \\ & \dots \\ & + \underbrace{X_1 \cdot \dots \cdot X_i}_{2^i \text{ terms}} \cdot P(X_{i+1}, \dots, X_n) \end{aligned}$$

where  $P(X_{i+1}, \dots, X_n)$  is the  $(n-i)$ -variable product term specified by the rule. The expression above is just the generalized Shannon expansion for  $P$ , and thus equals  $P$ .

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3e4.63 4.52

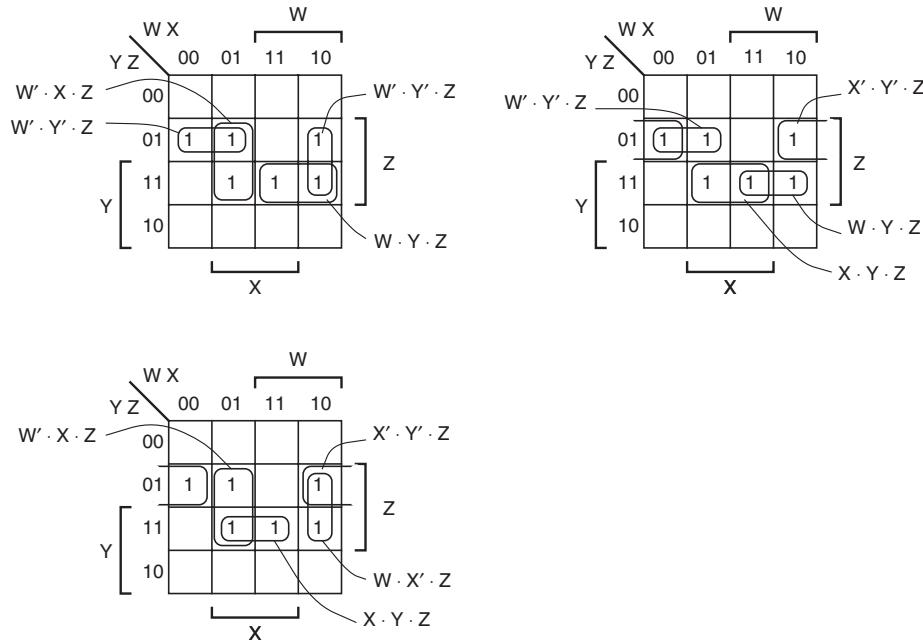


$$F = W' \cdot X \cdot Y + W' \cdot Y \cdot Z' + W \cdot Y' \cdot Z + W \cdot X \cdot Z$$

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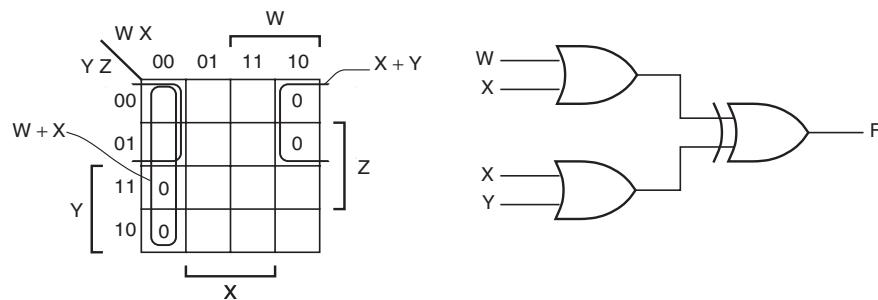
**3e4.64 4.53** The logic function in Figure 4-36 has three irredundant sums:



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G4.265 4.54



If the OR gates are changed to NOR gates the solution remains unchanged.

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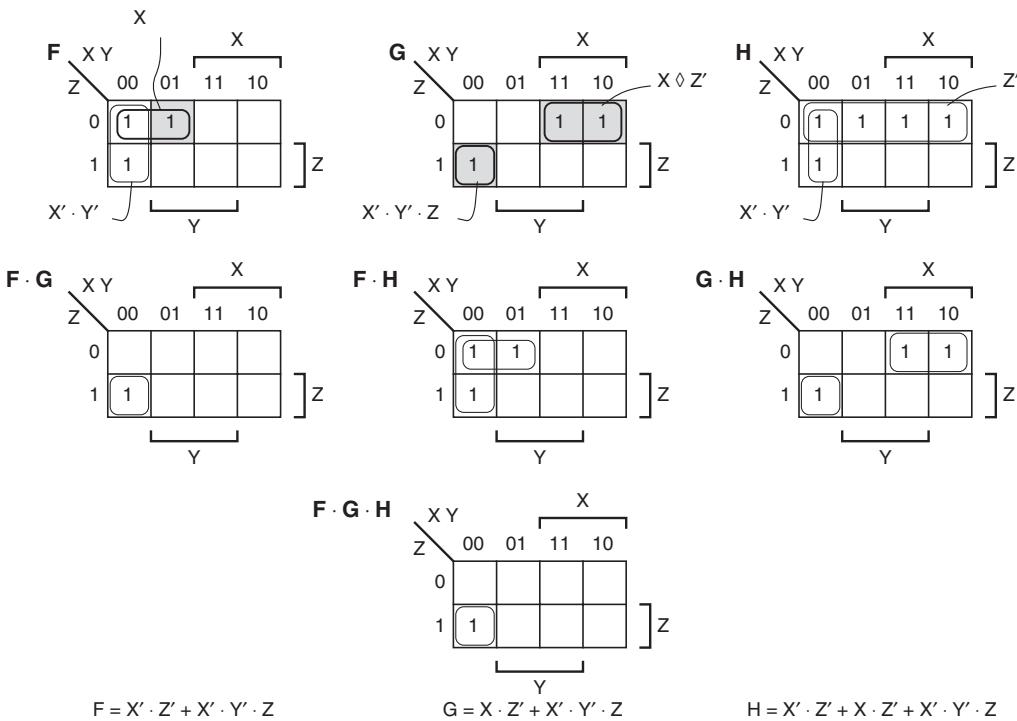
G4.266 4.55

$$\begin{aligned}F = & Q_2 \cdot P_2' + Q_2 \cdot Q_1 \cdot P_1' + Q_2 \cdot Q_0 \cdot P_1' \cdot P_0' + Q_0 \cdot P_2' \cdot P_1' \cdot P_0' \\& + Q_1 \cdot P_2' \cdot P_1' + Q_1 \cdot Q_0 \cdot P_2' \cdot P_0' + Q_2 \cdot Q_1 \cdot Q_0 \cdot P_0'\end{aligned}$$

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3e4.67 4.56



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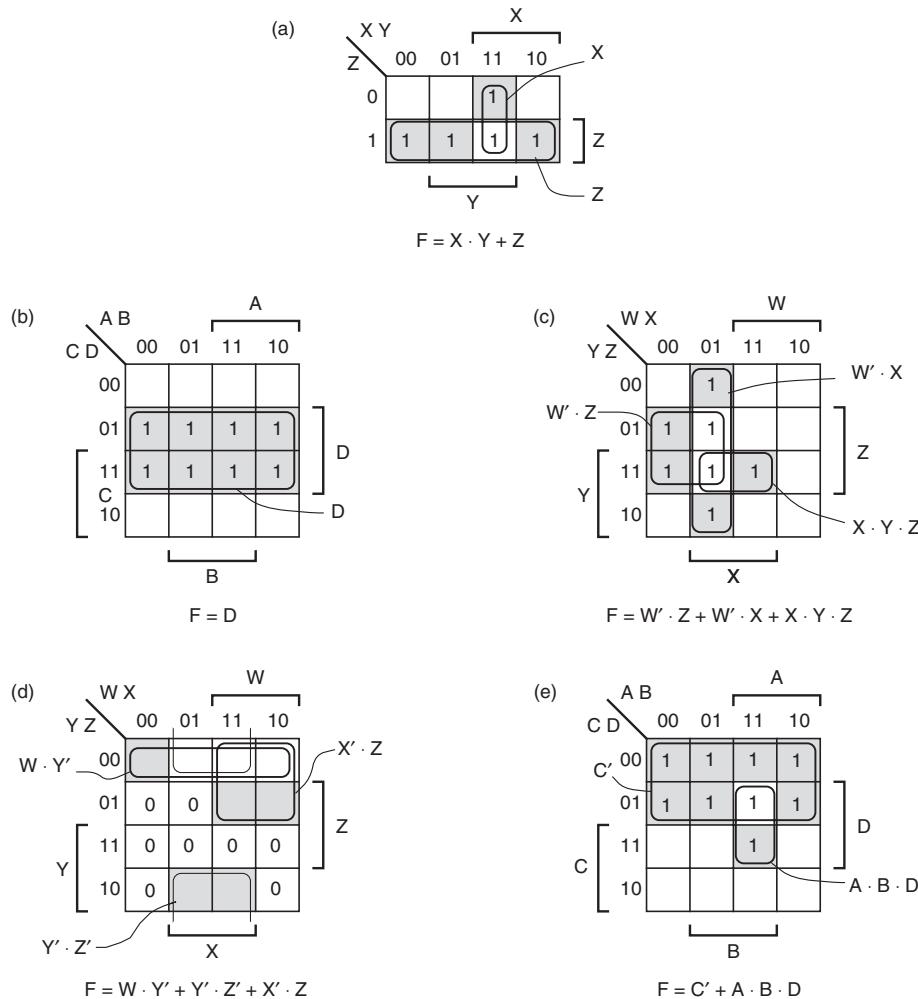
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- G4.268 4.57 The first step is to check whether any term covers any other. By inspection, no. Next, use consensus to see if any smaller product terms can be generated.

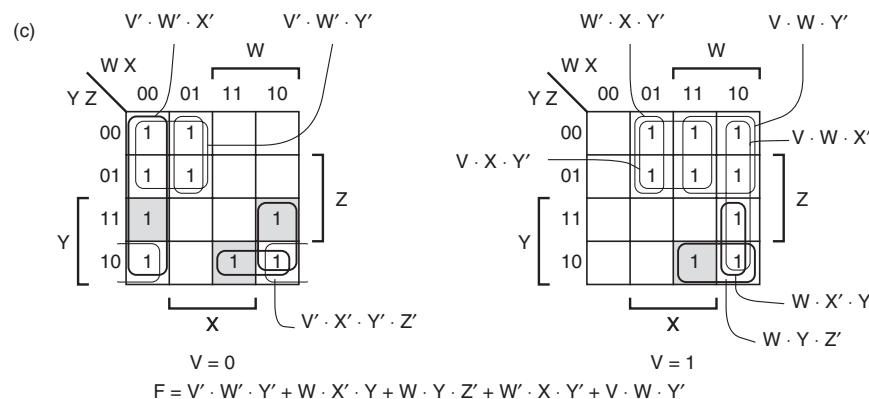
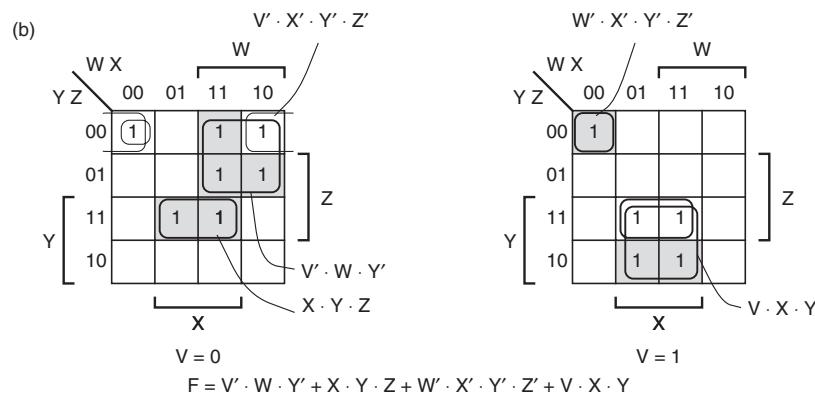
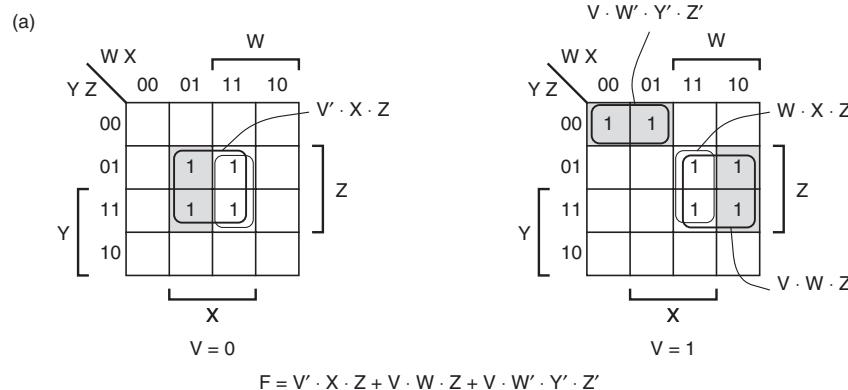
$$\text{consensus } (S' \cdot T \cdot U \cdot V \cdot W, T' \cdot S \cdot U' \cdot W \cdot Y) = S' \cdot T \cdot V \cdot W \cdot Y$$

The consensus term covers  $S' \cdot T \cdot V \cdot W \cdot X' \cdot Y$  in the original expression, which therefore is not minimal. The minimal sum is just the sum of the first two product terms.

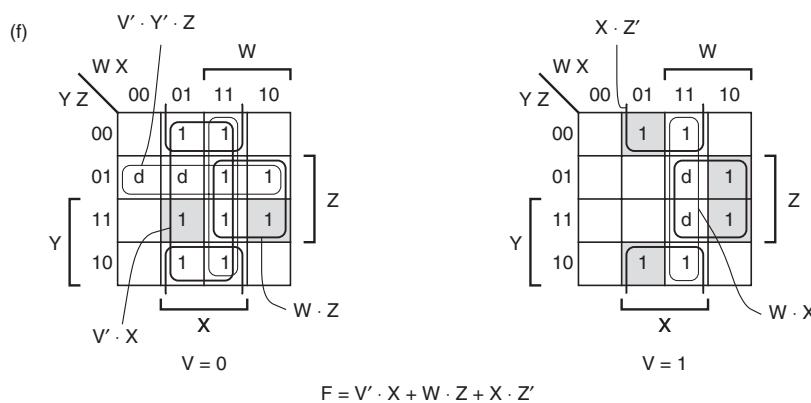
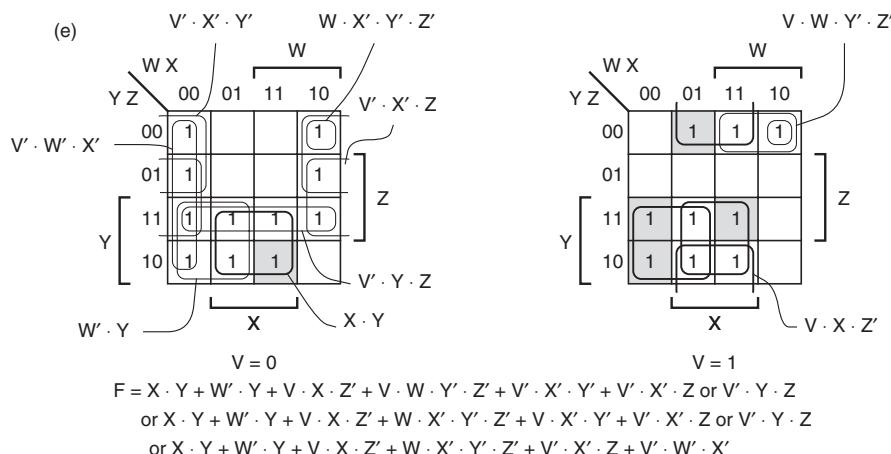
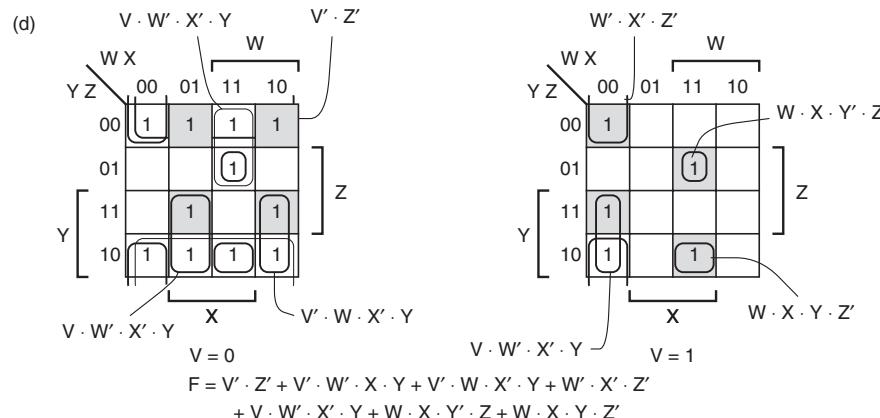
- G4.269 4.58 For part (d), note that it is easiest to work with the product-of-sums directly; rather than multiplying out, one simply enters the 0s on the map.



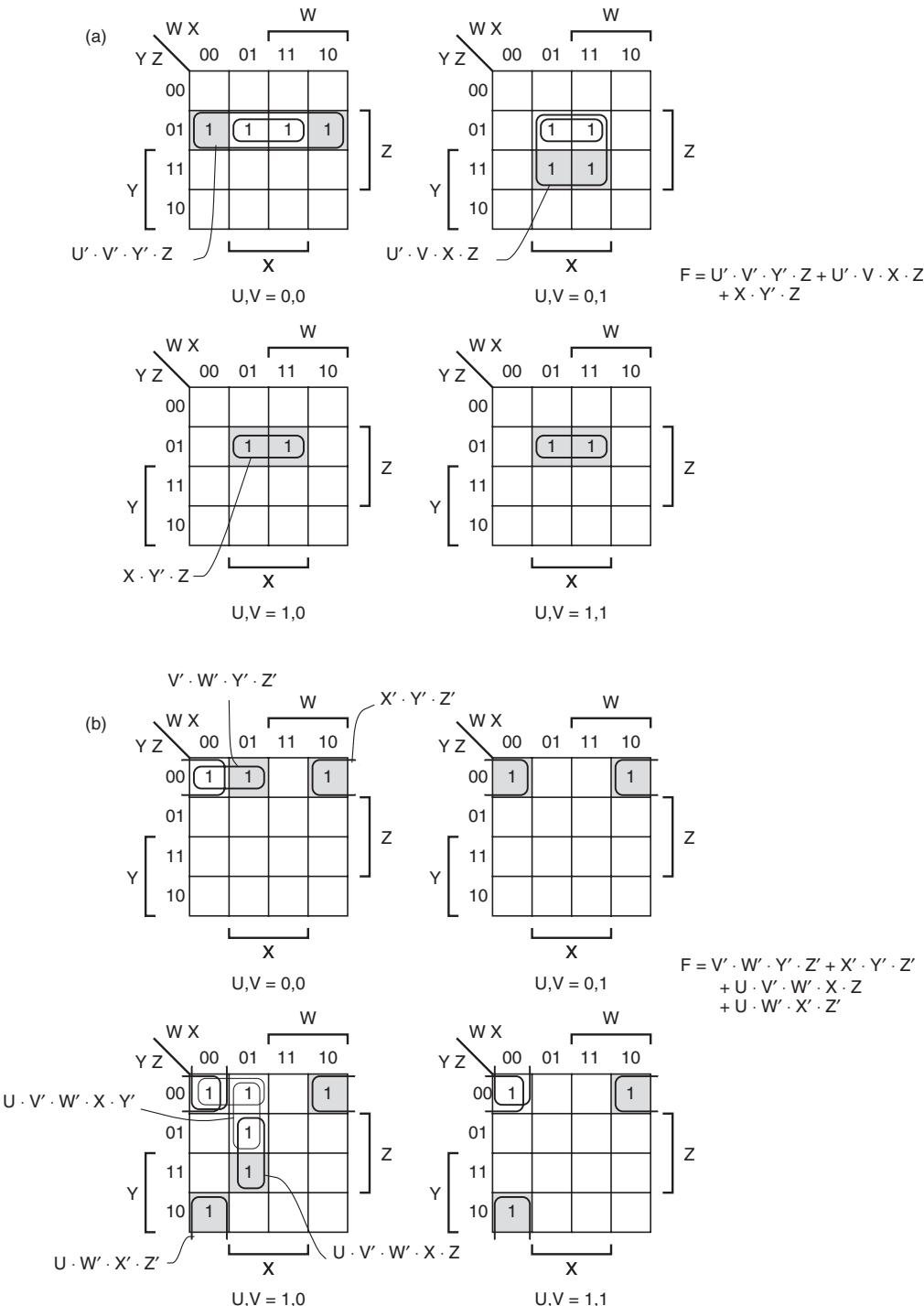
3e4.72 4.59



(continued)



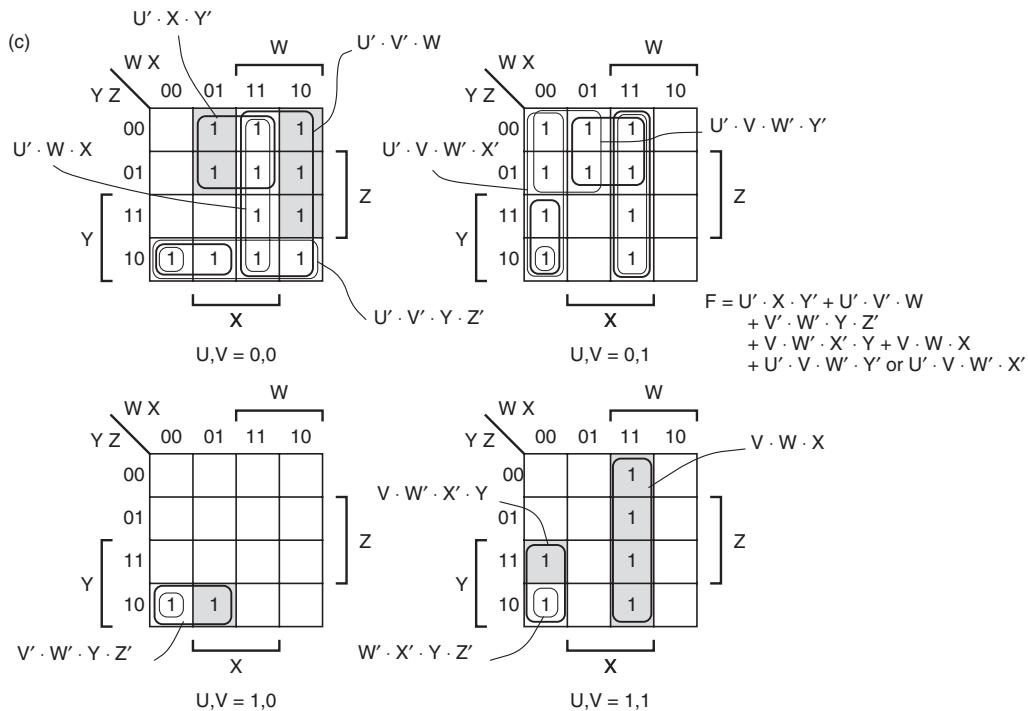
3e4.74 4.60



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(continued)

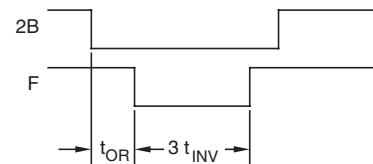


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3e4.83

- 4.61 The name of the circuit comes from its output equation,  $F = \overline{B} \text{ OR } \overline{\overline{B}}$ . On the falling edge of  $\overline{B}$ , this circuit generates a negative pulse on  $F$ . Note that this is typically an unreliable way to generate a pulse because the width of the pulse depends on the inverter delays, which in turn depend on electrical characteristics that vary with voltage, temperature, and the IC manufacturing process.



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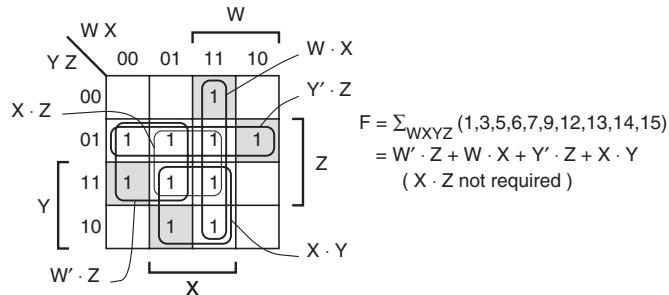
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- 3e4.84 4.62 There are no static-0 hazards in a properly designed 2-level AND-OR circuit, as discussed in Section 3.5.2. We can show that there are no static-1 hazards by contradiction. Suppose an  $n$ -variable function has two adjacent input combinations  $I$  and  $J$  that have a static-1 hazard. By definition,  $I$  and  $J$  both produce a 1 output, and since they are adjacent, they are covered by a single  $(n-1)$ -variable product term. This product term is either a prime implicant, or is included in some prime implicant. Since the complete sum includes all prime implicants,  $I$  and  $J$  are both covered by a single product term (AND gate), and no glitch is possible.

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3e4.85 4.63



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- 5.1 Please extract the source-code file Dec2to4.abl from the accompanying .zip file.

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- 5.2 Please extract the source-code file PrimeDet.abl from the accompanying .zip file.

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- 5.11 Always use blocking assignments (=) in always blocks intended to synthesize combinational logic.

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- 5.18 When targeting the design to an XC9500-series CPLD, the Xilinx ISE tools reduce it to a single XOR gate.

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- 5.19 Please extract the source-code file `MultiDet.abl` from the accompanying `.zip` file.

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- 5.20 Please extract the source-code file MultiDtT.abl from the accompanying .zip file.

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- 5.21 Please extract the source-code file NonWhenEx.abl from the accompanying .zip file.

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**5.23** Please extract the source-code file primeEx.vhd from the accompanying .zip file.

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- 5.24 There are two versions of the solution in the accompanying .zip file. The architecture in file M35Det.vhd uses VHDL's mod operation, which gives the simplest, least-prone-to-error solution. However, the mod operation is not synthesizable by most tools unless the modulus is a power of 2. The architecture in file M35Detc.vhd uses case statements to enumerate the multiples of 3 and 5.

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- 5.25** Please extract the source-code file M35DetTB.vhd from the accompanying .zip file. Note that the mod operation should be supported by the simulator that runs the test bench, even if it is not supported in synthesis.

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- 5.34 There are two versions of the solution in the accompanying .zip file. The architecture in file M35Det.v uses Verilog's modulo (%) operation, which gives the simplest, least-prone-to-error solution. However, the modulo operation is not synthesizable by most tools unless the modulus is a power of 2. The architecture in file M35Detc.v uses case statements to enumerate the multiples of 3 and 5.

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- 5.35** Please extract the source-code file M35Det\_tb.v from the accompanying .zip file. Note that the % operation should be supported by the simulator that runs the test bench, even if it is not supported in synthesis.

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- 5.36 There are two source-code files in the accompanying .zip file: the Verilog module `Vrprimebv8.v` and the test bench `Vrprimebv8_tb.v`.

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**5.37** Please extract the source-code file `VrFAdflow.v` from the accompanying `.zip` file.

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- 5.38 There are two different versions of the solution in the accompanying .zip file. The module VrAdder4.v uses four instance statements. The module VrAdder4g.v uses a generate block and can be easily modified to create a ripple adder of any desired width. A useful additional exercise is to further modify this program so that the width can be changed by changing the value of a single, declared parameter.

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- 5.39 Please extract the source-code file VrAdder4\_tb.v from the accompanying .zip file.

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- 5.40 Please extract the source-code file VrAdder16.v from the accompanying .zip file.

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- 5.41 Please extract the source-code file VrAdder16\_tb.v from the accompanying .zip file. The test bench uses the strategy of specifying different, odd step amounts for the loops that control the X and Y operands, so that many different combinations are tested. Another approach would be to use a 32-bit random-number generator (for example, using an LFSR as in Chapter 8) to generate the operands. In any case, it seems prudent and easy enough to test each pair of operands with both possible values of the carry-in (Cin).

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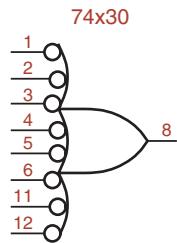
G5.201 6.1 Presumably, “billions and billions” means at least 4 billion, or about  $2^{32}$ . Thus, we’ll need functions with at least 32 input bits, such as the following:

- A 32-input parity generator. The truth table has  $2^{32}$  rows for all the combinations of inputs D0–D31, and one column for the output PARITY.
- A logic-function generator for two 16-bit operands. The truth table has  $2^{36}$  rows for all the combinations of inputs X0–X15, Y0–Y15, and F0–3 (to select one of 16 functions), and 16 columns for outputs S0–S15.
- A 8-input, 4-bit multiplexer with enable. The truth table has  $2^{36}$  rows for all the combinations of the 32 data bits, three select bits, and enable, and four columns for the data outputs.
- An “Adjacency Detector” for the 50 U.S. states. The circuit has 50 inputs corresponding to the 50 U.S. states, and one output C. The truth table has  $2^{50}$  rows corresponding to all possible subsets of the states, and one column for the output C. The output C is 1 if it is possible to drive to all states in the selected subset without ever leaving the selected subset of states.

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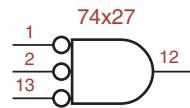
3e5 . 2      6.2



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3e5.3      6.3



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3e5.4 6.4 READY' is an expression, with ' being a unary operator. Use a name like READY\_L or /READY instead.

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- 3e5.5    6.5 In most logic technologies (including CMOS and TTL), inverting gates are faster and have fewer transistors than noninverting ones. Also, some signals must be created active-low in order to drive the predefined, active-low control inputs of MSI and LSI devices.

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- G5.206 6.6 A signal from a bubble output is connected to a nonbubble input when the negated state of the signal should enable the function. For example, the negated state may indicate an opposite function, such as the READ\_L bubble output going to a nonbubble input to indicate WRITE\_H. As another example, BOIL\_WATER and ENABLE\_POT\_WARMER on your coffee maker might require the assertion of BREWING\_L, but the AND gate that generates the COFFEE\_READY indicator would require the negation of BREWING\_L (meaning NOT\_BREWING\_H) and the assertion of NOT\_YET\_STALE.

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- G5.206 6.7 False. It's true that in most logic technologies, all inputs of a primitive logic gate have the same active level. However, it is also possible to define gates that have one input active high and another active low, such as the inhibit gate in Sections 5.3.1 and 5.4.1. In most technologies, this behavior is obtained at the expense of an inverter on the input of a primitive gate.

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- 3e5.7 6.8 Hierarchical, since only one copy of the network-port schematic need be drawn. You might say, “Well, I can make it non-hierarchical (flat), draw one original schematic page for one port, and copy it eleven more times.” There are two drawbacks to this approach:
- (1) You have to manually renumber the identifiers (reference designators and signal names) on each page to distinguish the ports.
  - (2) If you find later that a change is needed, you have to manually update twelve pages, and make sure they’re all done identically.

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- 3e5.8    6.9 Both LOW-to-HIGH and HIGH-to-LOW transitions cause positive transitions on the outputs of three gates (every second gate), and negative transitions on the other three. Thus, the total delay in either case is

$$\begin{aligned} t_p &= 3t_{pLH(LS00)} + 3t_{pHL(LS00)} \\ &= 3 \cdot 15 + 3 \cdot 15 \\ &= 90 \text{ ns} \end{aligned}$$

Since  $t_{pLH}$  and  $t_{pHL}$  for a 74LS00 are identical, the same result is obtained using a single worst-case delay of 15 ns.

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- G5.209 6.10 Both LOW-to-HIGH and HIGH-to-LOW transitions cause positive transitions on the outputs of three gates (every second gate), and negative transitions on the other three. Thus, the total delay in either case is

$$\begin{aligned}, &= 3t_{pLH(AHCT00)} + 3t_{pHL(AHCT00)} \\ &= 3 \cdot 9 + 3 \cdot 9 \\ &= 54 \text{ ns}\end{aligned}$$

Since  $t_{pLH}$  and  $t_{pHL}$  for a 74AHCT00 are identical, the same result is obtained using a single worst-case delay of 9 ns.

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G5.210 6.11 In this case all transitions go in the same direction. Thus,

$$\begin{aligned}t_{\text{pLH}} &= 6t_{\text{pLH(LS21)}} \\&= 6 \cdot 15 = 90 \text{ ns}\end{aligned}$$

$$\begin{aligned}t_{\text{pHL}} &= 6t_{\text{pHL(LS21)}} \\&= 6 \cdot 20 = 120 \text{ ns}\end{aligned}$$

Without inverters to “flip” the transition polarity at each stage, the asymmetry between  $t_{\text{pLH}}$  and  $t_{\text{pHL}}$  grows with the number of stages. A worst-case calculation yields 120 ns, which is in fact achieved in HIGH-to-LOW transitions.

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- G5.211    6.12 Both LOW-to-HIGH and HIGH-to-LOW transitions cause positive transitions on the outputs of three gates (every second gate), and negative transitions on the other three. Thus, the total delay in either case is

$$\begin{aligned} t_p &= 2t_{pLH(AHCT02)} + 2t_{pHL(AHCT02)} + 1t_{pLH(LS00)} + 1t_{pHL(LS00)} \\ &= 2 \cdot 3.4 + 2 \cdot 4.5 + 9 + 10 \\ &= 34.8 \text{ ns} \end{aligned}$$

A worst-case calculation yields  $4 \cdot 8.5 + 2 \cdot 15 = 64$  ns , which is never achieved in practice.

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- 3e5.12 6.13 The smallest typical delay through one 'LS86 for any set of conditions is 10 ns. Use the rule of thumb, "minimum equals one-fourth to one-third of typical," we estimate 3 ns as the minimum delay through one gate. Therefore, the minimum delay through the four gates is estimated at 12 ns.

The above estimate is conservative, as it does not take into account the actual transitions in the conditions shown. For a LOW-to-HIGH input transition, the four gates have typical delays of 13, 10, 10, and 20 ns, a total of 53 ns, so the minimum is estimated at one-fourth of this or 13 ns. For a HIGH-to-LOW input transition, the four gates have typical delays of 20, 12, 12, and 13 ns, a total of 57 ns, so the minimum is estimated at 14 ns.

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- 3e5.13 6.14 For both LOW-to-HIGH and HIGH-to-LOW transitions, each of the four gates has a delay of 40 ns, a total of 160 ns. A worst-case analysis yields the same result, since  $t_{PLH}$  and  $t_{PHL}$  are identical.

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- 3e5.14 6.15 For a LOW-to-HIGH transition, the four gates have delays of 10.5, 10.5, 10.5, and 10 ns, a total of 41.5 ns. For a HIGH -to-LOW transition, the four gates have delays of 10, 10, 10, and 10.5 ns, a total of 40.5 ns. A worst-case analysis predicts a delay of 42 ns, which is not quite achieved.

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- 3e5.15 6.16 A decoder with active-low outputs ought to be faster, considering that this decoder structure can be implemented directly with inverting gates (which are faster than noninverting) as shown in Figures 5–35 and 5–37.

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- 3e5.16 6.17 The worst-case '138 output will have a transition in the same direction as the worst-case '139 output, so we use  $t_{pHL}$  numbers for both, which is the worst combination. The delay through the '139 is 38 ns, and from the active-low enable input of the '138 is 32 ns, for a total delay of 70 ns. Using "worst-case" numbers for the parts and ignoring the structure of the circuit, an overly pessimistic result of 79 ns is obtained.

We can also work the problem with 74HCT parts. Worst-case delay through the '139 is 43 ns, and from the active-low enable input of the '138 is 42 ns, for a total delay of 85 ns. Ignoring the structure of the circuit, an overly pessimistic result of 88 ns is obtained.

We can also work the problem with 74FCT parts. Worst-case delay through the '139 is 9 ns, and from the active-low enable input of the '138 is 8 ns, for a total delay of 17 ns. Ignoring the structure of the circuit, a slightly pessimistic result of 18 ns is obtained.

Finally, we can work the problem with 74AHCT parts. Worst-case delay through the '139 is 10.5 ns, and from the active-low enable input of the '138 is 12 ns, for a total delay of 22.5 ns. Ignoring the structure of the circuit, a slightly pessimistic result of 23.5 ns is obtained.

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- G5.217 6.18 Examination reveals that the most likely maximum delay path is from one of the 74AHCT139 inputs to the 74AHCT138 outputs. The delays from the EN3\_L (74AHCT139 1G) input and the N3, N4 (74AHCT139 1A, 1B) inputs are calculated as follows:

$$\begin{aligned} t_{pLH(EN3\_L)} &= t_{pLH(AHCT139 ENB)} + t_{pLH(AHCT138 G2)} \\ &= (9.5 + 12) = 21.5 \text{ ns} \end{aligned}$$

$$\begin{aligned} t_{pHL(EN3\_L)} &= t_{pHL(AHCT139 ENB)} + t_{pHL(AHCT138 G2)} \\ &= (9 + 8) = 17 \text{ ns} \end{aligned}$$

$$\begin{aligned} t_{pLH(SEL)} &= t_{pLH(AHCT139 SEL)} + t_{pLH(AHCT138 G2)} \\ &= (10.5 + 8) = 18.5 \text{ ns} \end{aligned}$$

$$\begin{aligned} t_{pHL(SEL)} &= t_{pHL(AHCT139 SEL)} + t_{pLH(AHCT138 G2)} \\ &= (9 + 12) = 21 \text{ ns} \end{aligned}$$

The worst-case delay is  $t_{pLH(EN3\_L)} = 21.5 \text{ ns}$ . Examination of Table 5-3 confirms that this delay is longer than any of the delays from N0-2, EN1 and EN2\_L to the 74AHCT138 outputs.

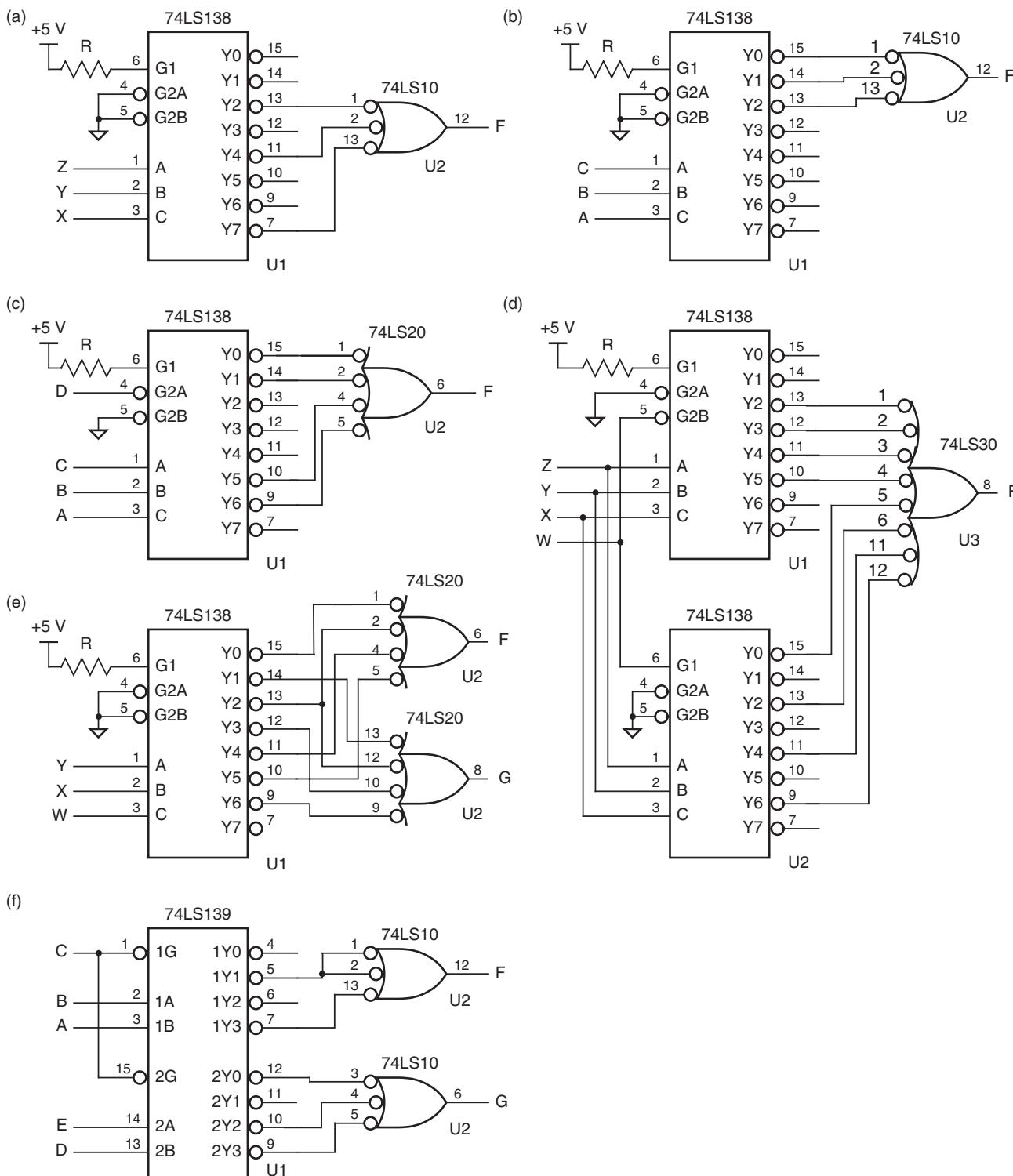
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6.19

Inputs						Outputs							
G1	G2A	G2B	C	B	A	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0	x	x	x	x	x	0	0	0	0	0	0	0	0
x	0	x	x	x	x	0	0	0	0	0	0	0	0
x	x	0	x	x	x	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	1
1	1	1	0	0	1	0	0	0	0	0	0	1	0
1	1	1	0	1	0	0	0	0	0	0	1	0	0
1	1	1	0	1	1	0	0	0	0	1	0	0	0
1	1	1	1	0	0	0	0	0	1	0	0	0	0
1	1	1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	1	1	0	0	0	0	0	0	0

G5.219 6.20



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- 3e5.21 6.21 Both halves of the '139 are enabled simultaneously when EN\_L is asserted. Therefore, two three-state drivers will be enabled to drive SDATA at the same time. Perhaps the designer forgot to put an extra inverter on the signal going to 1G or 2G, which would ensure that exactly one source drives SDATA at all times.

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- 3e5 .22    6.22 The total delay is the sum of the decoding delay through the 74LS139, enabling delay of a 74LS151, and delay through a 74LS20:  $38 + 30 + 15 = 83$  ns .

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- G5.223 6.23 If the 74AHCT151 Y' output is used, then either 1 or 3 levels of inverting gates are needed. The only 1-level solution is a 74x20, or a wider gate not listed in the table. If the Y output is used, then 2 levels of inverting gates or any number of non-inverting gates are needed. A 2-level solution with inverting gates needs both NOR and NAND gates. A 2-level solution with non-inverting gates needs just OR gates, so the solution is the 74AHCT32, with a delay of  $8.5 + 8.5 = 17$  ns. The total delay is the sum of the decoding delay through the 74AHCT139, enabling delay of a 74AHCT151, and delay through two 74AHCT32's:  $10.5 + 7 + 17 = 34.5$  ns .

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- G5 .224 6.24 If the number of levels (gates) is odd, the inverter bubbles all cancel in pairwise fashion except for the last one, so we get even parity.

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- 3e5.25 6.25 The worst-case delay is the sum of the delays through an 'LS280, select-to-output through an 'LS138, and through an 'LS86:  $50 + 41 + 30 = 121$  ns .

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- G5.226 6.26 The worst-case delay is the sum of the delays through an 'AHCT280, select-to-output through an 'AHCT138, and through an 'AHCT86:  $10 + 13 + 10 = 33 \text{ ns}$ .

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G5.227

6.27

$$(A = B) = (A_3 \oplus B_3)' \cdot (A_2 \oplus B_2)' \cdot (A_1 \oplus B_1)' \cdot (A_0 \oplus B_0)'$$

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G5.229 6.28 Define  $\text{EQ}_i = (\text{Pi} \oplus \text{Qi})'$ . Then

$$(\text{PEQQ\_L} = (\text{EQ}_7 \cdot \text{EQ}_6 \cdot \text{EQ}_5 \cdot \text{EQ}_4 \cdot \text{EQ}_3 \cdot \text{EQ}_2 \cdot \text{EQ}_1 \cdot \text{EQ}_0)')$$

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G5.228 6.29

$$c_1 = x_0 \cdot y_0 \text{ (Assuming } c_0 = 0)$$

$$\begin{aligned}c_2 &= x_1 \cdot y_1 + x_1 \cdot c_1 + y_1 \cdot c_1 \\&= x_1 \cdot y_1 + x_1 \cdot (x_0 \cdot y_0) + y_1 \cdot (x_0 \cdot y_0) \\c_3 &= x_2 \cdot y_2 + x_2 \cdot c_2 + y_2 \cdot c_2 \\&= x_2 \cdot y_2 + x_2 \cdot (x_1 \cdot y_1 + x_1 \cdot (x_0 \cdot y_0) + y_1 \cdot (x_0 \cdot y_0)) + y_2 \cdot (x_1 \cdot y_1 + x_1 \cdot (x_0 \cdot y_0) + y_1 \cdot (x_0 \cdot y_0)) \\s_3 &= x_3 \oplus y_3 \oplus c_3 \\s_3 &= x_3 \oplus y_3 \oplus [x_2 \cdot y_2 + x_2 \cdot (x_1 \cdot y_1 + x_1 \cdot (x_0 \cdot y_0) + y_1 \cdot (x_0 \cdot y_0)) + y_2 \cdot (x_1 \cdot y_1 + x_1 \cdot (x_0 \cdot y_0) + y_1 \cdot (x_0 \cdot y_0))]\end{aligned}$$

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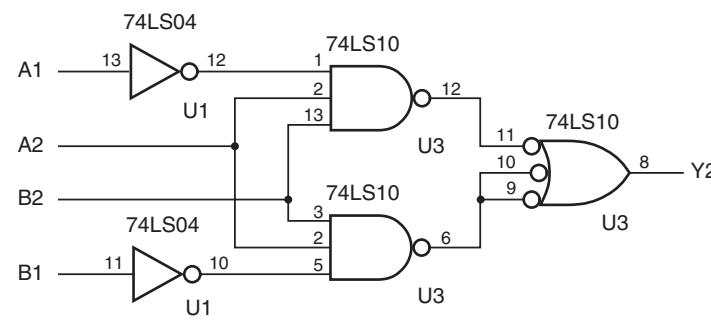
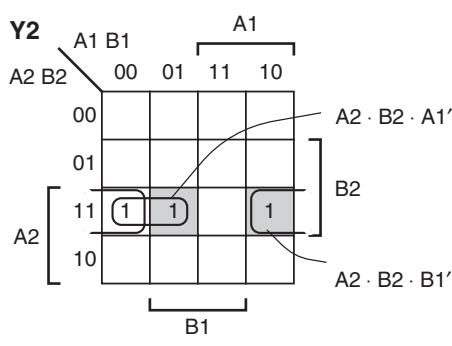
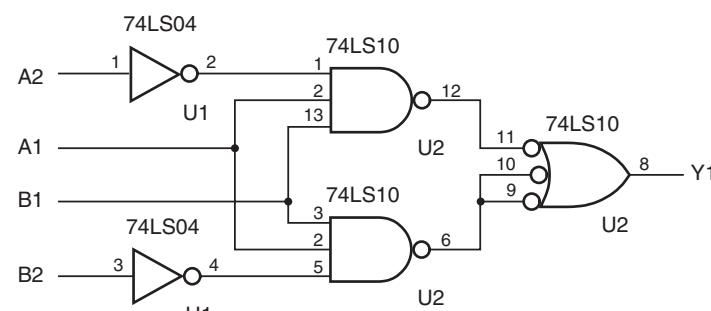
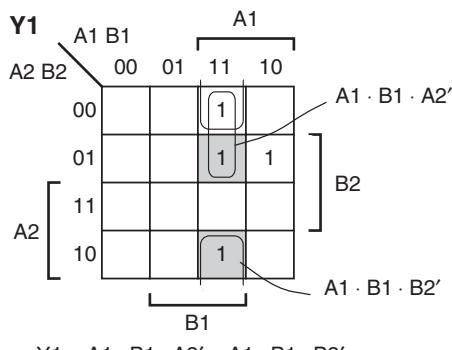
3e5.30 6.30 The worst-case delay is the sum of four numbers:

- In U1, the worst-case delay from any input to C4 (22 ns).
- In U2, the worst-case delay from C0 to C4 (22 ns).
- In U3, the worst-case delay from C0 to C4 (22 ns).
- In U4, the worst-case delay from C0 to any sum output (24 ns).

Thus, the total worst-case delay is 90 ns.

3e5.31 6.31

A1	B1	A2	B2	Y1	Y2	A1	B1	A2	B2	Y1	Y2
0	0	0	0	0	0	1	0	0	0	0	0
0	0	0	1	0	0	1	0	0	1	0	0
0	0	1	0	0	0	1	0	1	0	0	0
0	0	1	1	0	1	1	0	1	1	0	1
0	1	0	0	0	0	1	1	0	0	1	0
0	1	0	1	0	0	1	1	0	1	1	0
0	1	1	0	0	0	1	1	1	0	1	0
0	1	1	1	0	1	1	1	1	1	0	0



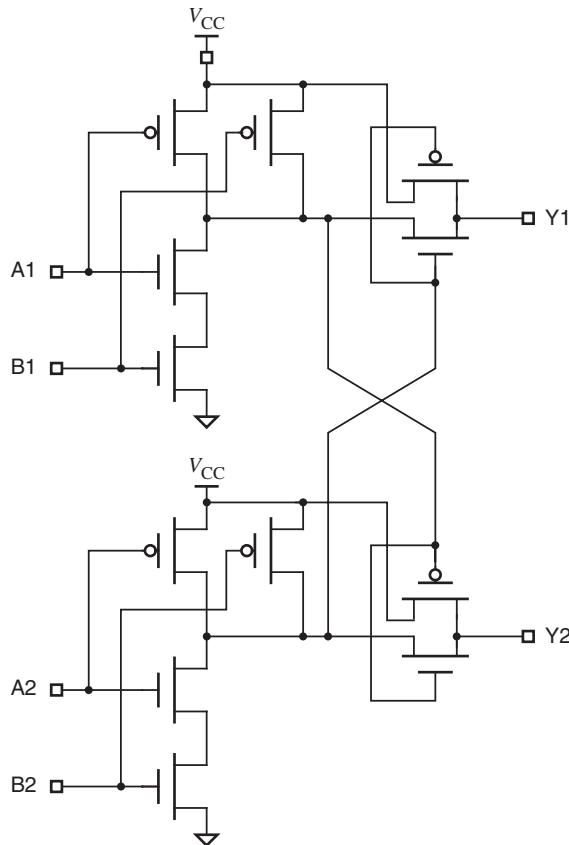
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- G5.232 6.32 The circuit below realizes an NBUT gate (a BUT gate with inverted outputs). To get a noninverting BUT gate, add an inverter to each output. Note that this design uses a “trick” by splitting the input signals to the *p*- and *n*-channel transistors in the “transmission gates.” This may or may not give acceptable electrical performance, depending on the characteristics of the transistors in the particular CMOS process used.

$$Y_1 = ((A_1 \cdot B_1) \cdot (A_2 \cdot B_2))'$$

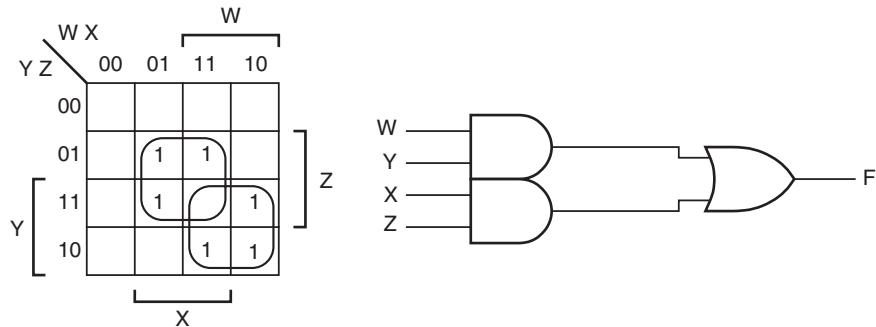
$$Y_2 = ((A_2 \cdot B_2) \cdot (A_1 \cdot B_1))'$$



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- G5.234 6.33 BUT-action turns off both gate outputs in cases where they would otherwise both be 1, eliminating the overlapped minterm in the Karnaugh map as shown.



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- 6.34 The accompanying .zip file contains a Verilog solution only, in source file `ButGate.v`.

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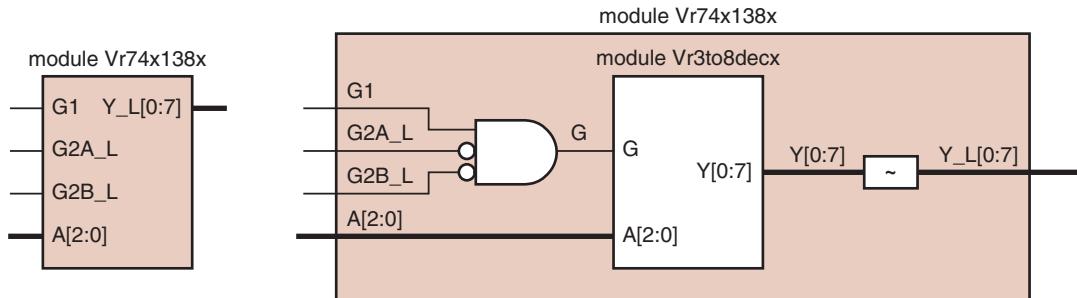
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**6.35** The accompanying .zip file contains a Verilog solution only, in source files ButFunc.v and ButFunc\_tb.v.

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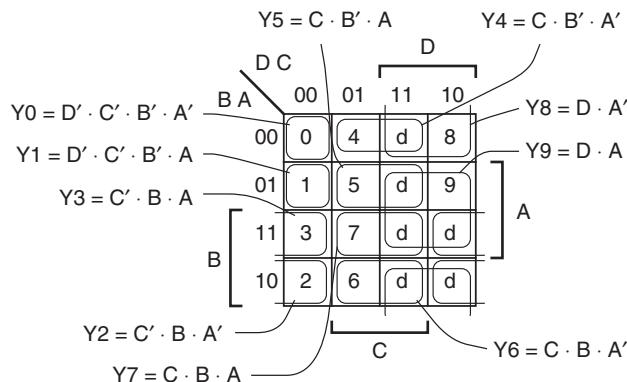
- 6.37 The accompanying .zip file contains two source files, Vr3to8decx.v (the generic decoder) and Vr74138x.v (emulating the 74x138 decoder). The relationship between the modules is shown in the figure below.



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- 3e5.36 6.38 As shown by the equations on the Karnaugh map, the gates for Y8 and Y9 require only two inputs, and the gates for Y2–Y7 require three inputs. The Y0 and Y1 gates require four inputs as before.



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3e5 .37    6.39 There are 10 functions, so there would be  $2^{10} - 1$  maps to look at.

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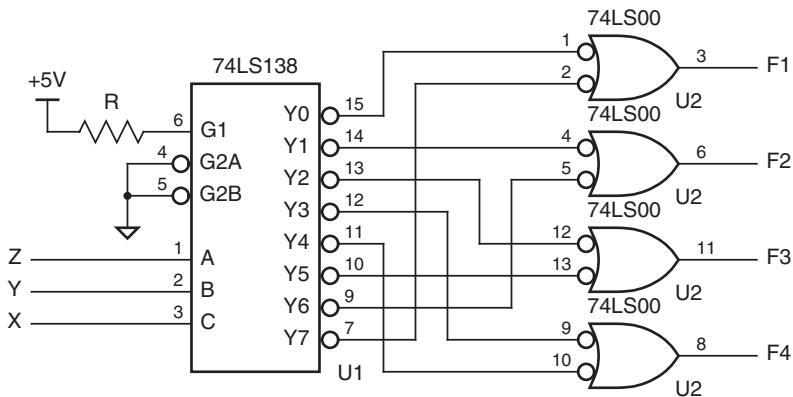
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- 3e5.38 6.40 The EN2\_L input is faster, since it goes straight to the '138s. However, it presents four loads to whatever is driving it. The EN3\_L input, though slower, has only one load.

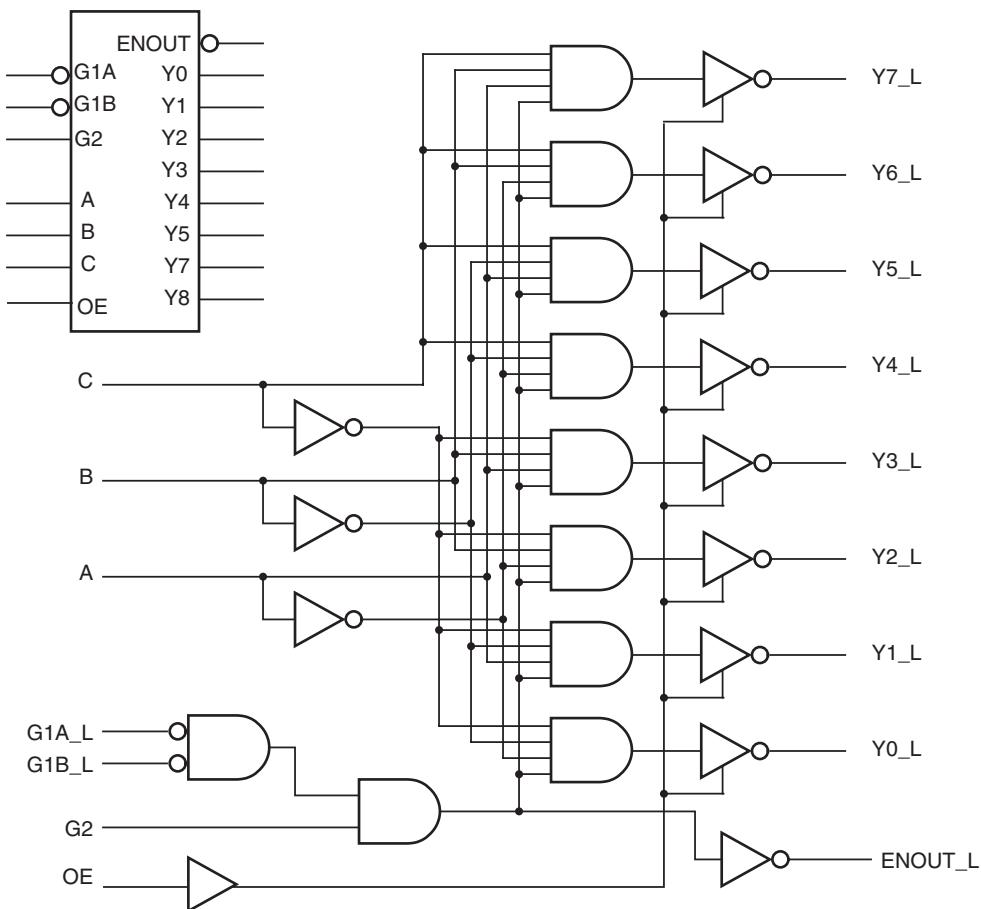
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3e5.82 6.43



- G5.242 6.44 (a) Note that C, B, and A could be labeled active-low, in which case the order of outputs Y0–Y7 would be reversed.



(b) The circuit is a 3-to-8 decoder with three-state outputs.

A, B, C Select inputs; C is most significant.

G1A\_L, G1B\_L, G2 Enable inputs. All must be asserted to enable an output.

OE Output enable input. When asserted, outputs are driven, otherwise they are tri-stated.

Y0–Y7\_L Decoded outputs. These are driven when OE is asserted, and tri-stated otherwise. When all enable inputs are asserted, the output selected by the select inputs is asserted.

ENOUT\_L Enable output. Asserted when all of the enable inputs are asserted.

(c) See figure in part (a).

(d) This part competes with the 'LS138. Its main use would be in applications requiring an active-low decoder and tri-state outputs so that it could be put on a bus. However, nowadays most designers would use a PLD such as the GAL16V8 when faced with such a requirement.

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**6.47** Please extract the Verilog source file `Vr7segE.v` from the accompanying `.zip` file.

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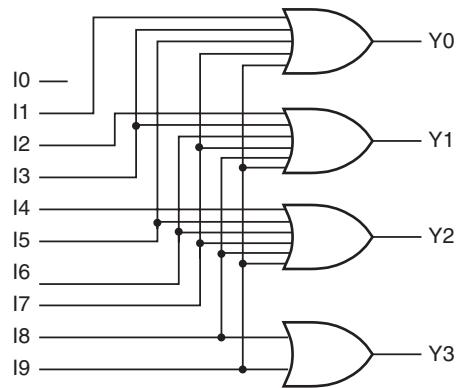
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- 6.48 Please extract the Verilog source file Vr7segx.v from the accompanying .zip file.

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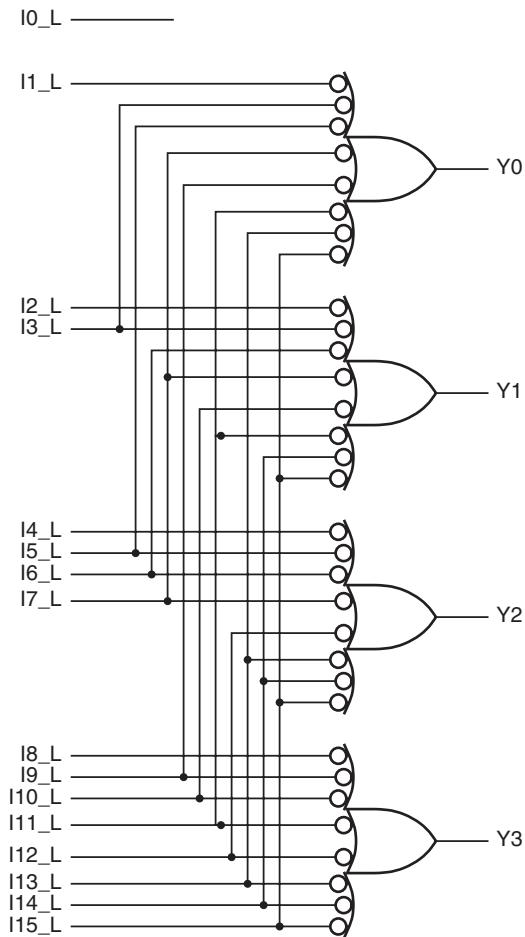
G5 .245 6.50



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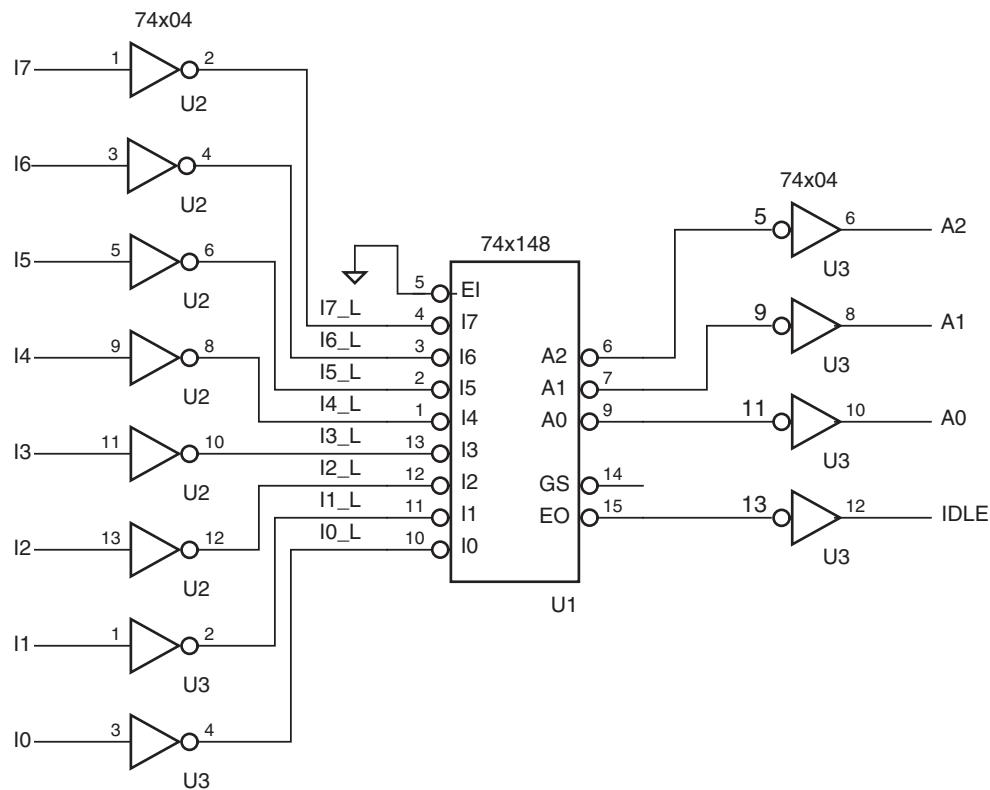
3e5.46 6.51 The inputs are active low and the outputs are active high in this design.



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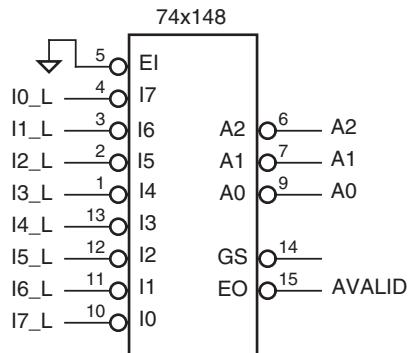
3e5.47 6.52



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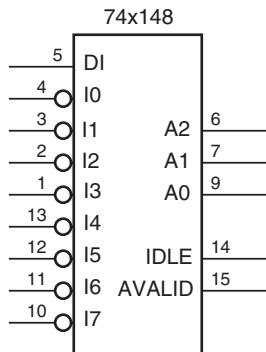
3e5.48 6.53



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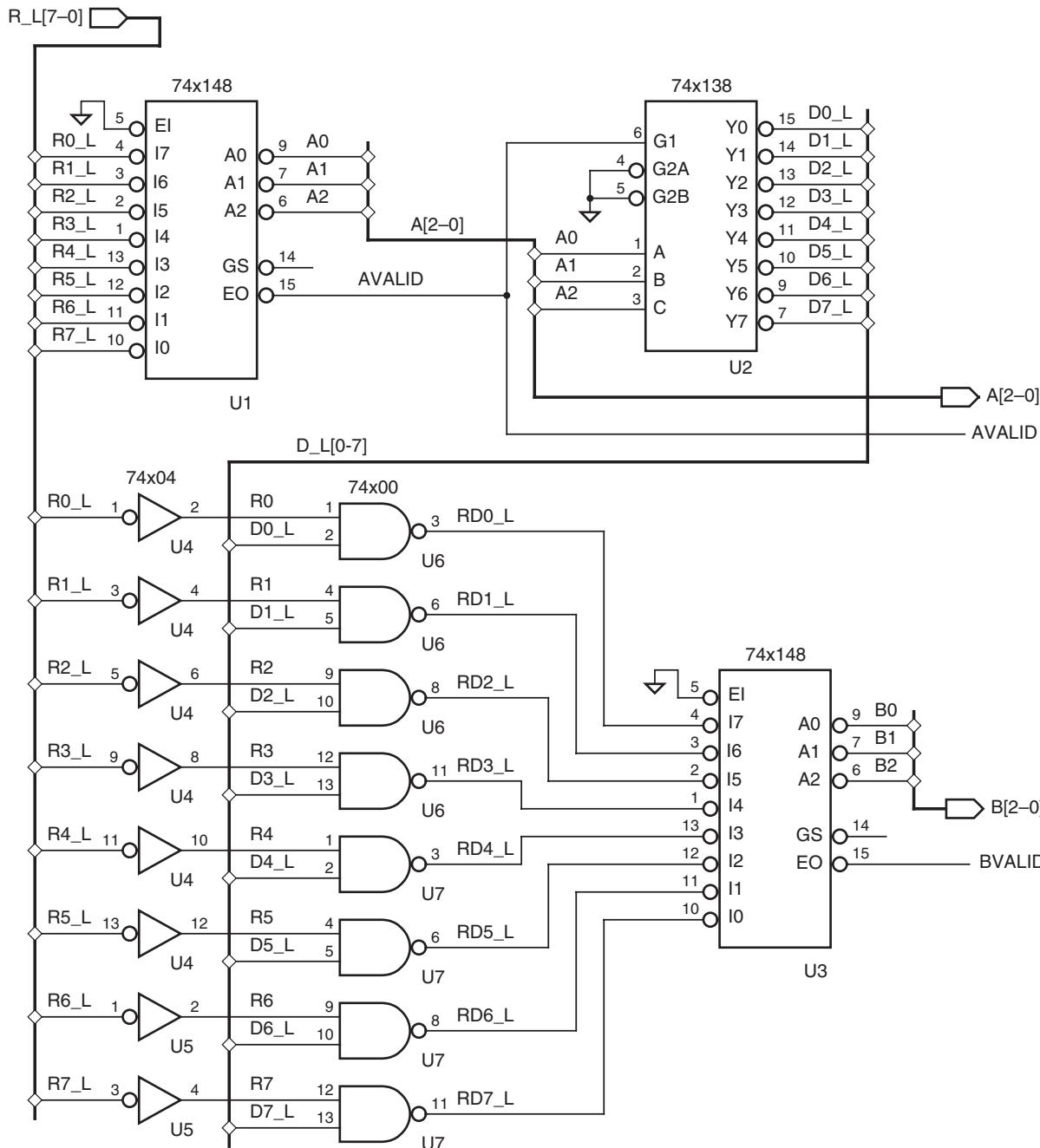
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3e5.49 6.54



- 3e5.50 6.55 In the circuit here, the first 'x148 finds the highest priority asserted input and puts its number on A2–A0 with AVALID HIGH. If no inputs are asserted, then AVALID is LOW. The 'x138 asserts the active-low Di\_L signal corresponding to the highest priority request. The NAND gates use the /Di signals to “mask out” the highest priority request, so the second 'x148 sees only the second-highest priority request and produces B2–B0 and BVALID as required.

Note that R0 is not really needed at the second 'x148 since R0 can never be the second-highest priority request. Therefore, one inverter and NAND gate could be omitted. Using the freed NAND gate as an inverter, one 'x04 package could be saved.



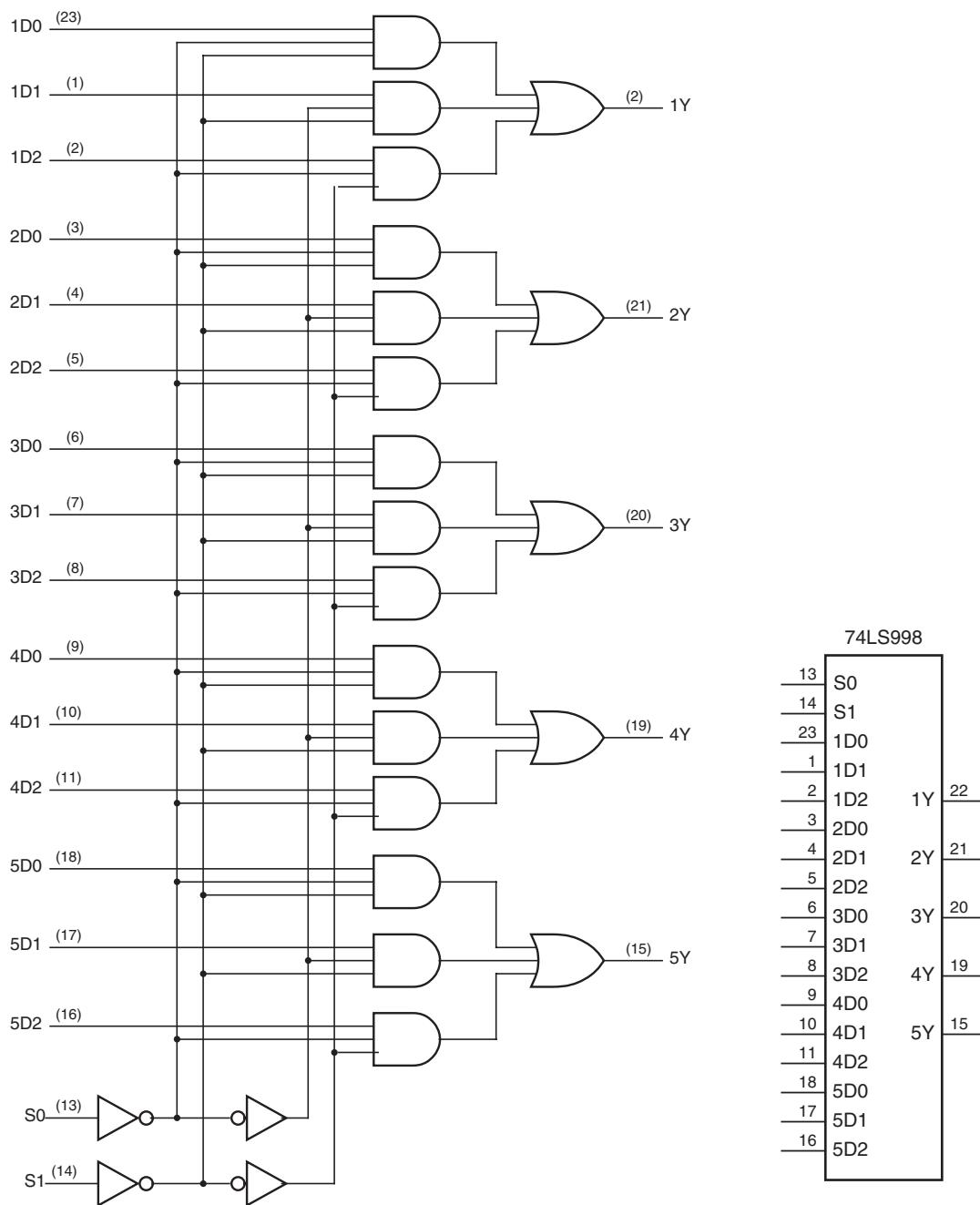
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**6.56** Please extract the source-code file `Prior8.abl` from the accompanying `.zip` file.

3e5.54

6.63 An internal logic diagram and pin assignment for the multiplexer are shown below.



A truth table and pin assignment for the mux are shown below.

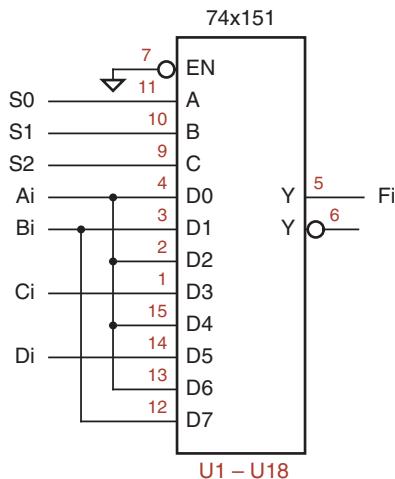
Inputs		Outputs				
S1	S0	1Y	2Y	3Y	4Y	5Y
0	0	1D0	2D0	3D0	4D0	5D0
0	1	1D1	2D1	3D1	4D1	5D1
1	0	1D2	2D2	3D2	4D2	5D2
1	1	0	0	0	0	0

The mux can be built using a single PLD, such as a GAL20V8; the pin assignment shown above is based on the GAL20V8. Source code for a corresponding ABEL program, Mux\_3x5.abel, is in the accompanying .zip file.

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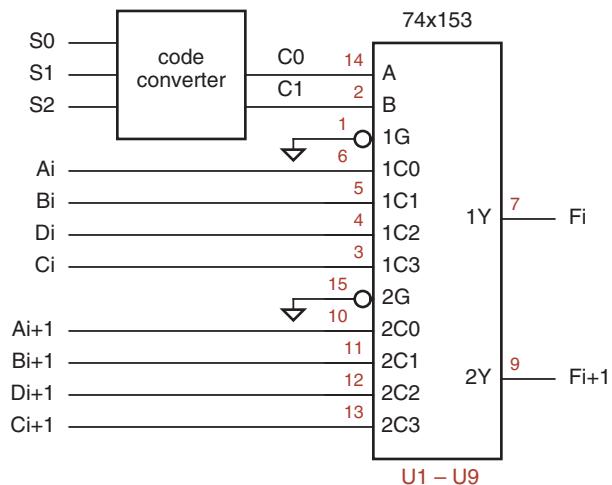
3e5 .60    6.65



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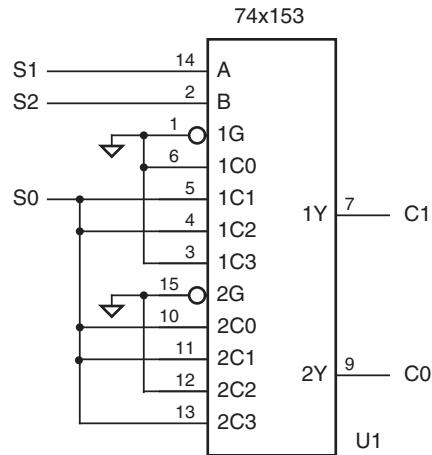
G5.261 6.66



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- G5.262 6.67 Using discrete gates, we would need to realize the equations  $C_0 = S_2' \cdot S_0 + S_1 \cdot S_0$  and  $C_1 = S_2' \cdot S_1 \cdot S_0 + S_2 \cdot S_1' \cdot S_0$ , which takes quite a few gates. This circuit can also be realized with a single 74x153 multiplexer:



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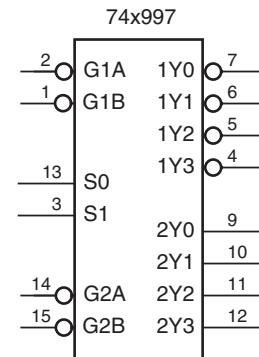
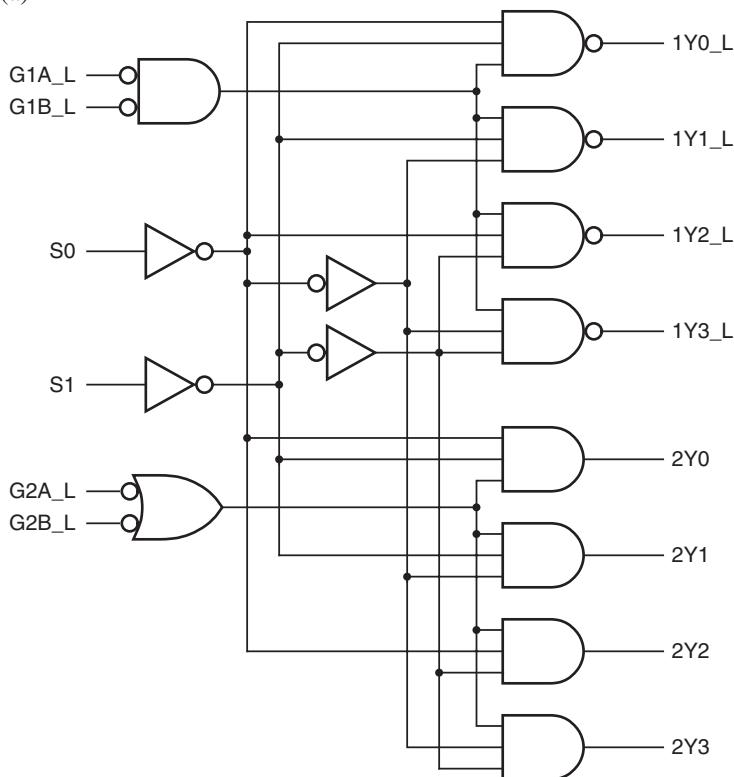
- 3e5.55 6.68 This is the actual circuit of a MUX21H 2-input multiplexer cell in LSI Logic's LCA 10000 series of CMOS gate arrays. When  $S$  is 0, the output equals  $A$ ; when  $S$  is 1, the output equals  $B$ .

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- G5.256 6.69 This is the actual circuit of an EO 2-input XOR cell in LSI Logic's LCA 10000 series of CMOS gate arrays.

3e5.57 6.70 (a)



(b) The circuit is a dual 2-to-4 decoder/demultiplexer with active-low outputs ( $1Y0\_L$ - $1Y3\_L$ ) on one section and active-high outputs ( $2Y0$ - $2Y3$ ) on the other. There is a common set of select inputs ( $S_1, S_0$ ) for both sections. Each section has a pair of active-low enable inputs, but the function is different in each section. In the first section, the selected output is asserted only if *both*  $G1A\_L$  and  $G1B\_L$  are asserted. In the second section, the selected output is asserted if *either*  $G2A\_L$  or  $G2B\_L$  is asserted.

(c) See figure in part (a).

(d) The accompanying .zip file contains three source files: *z74x997.abl*, *z74x997.vhd*, and *z74x997.v*.

(e) This part is similar to the 74x155. The active-high decoded outputs might be useful in some applications, as might be the OR'ed enable inputs. In this case, a part with all of the outputs active-high and all of the enable inputs OR'ed might be more useful. In any case, a PLD gives more flexibility. This part would probably bomb in the marketplace.

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- 3e5.64 6.71 This design can be performed entirely using multiplexers. One approach uses four 16-bit, 2-input multiplexers, each of which can be constructed using four 74x157s, for a total of 16 packages. The first mux “rotates” the input by 0 or 1 position, based on control input S0. The second mux receives the output of the first and rotates it by 0 or 2 positions, based on S1. Likewise, the third and fourth rotate the input by 0 or 4 and 0 or 8 positions, based on S2 and S3.

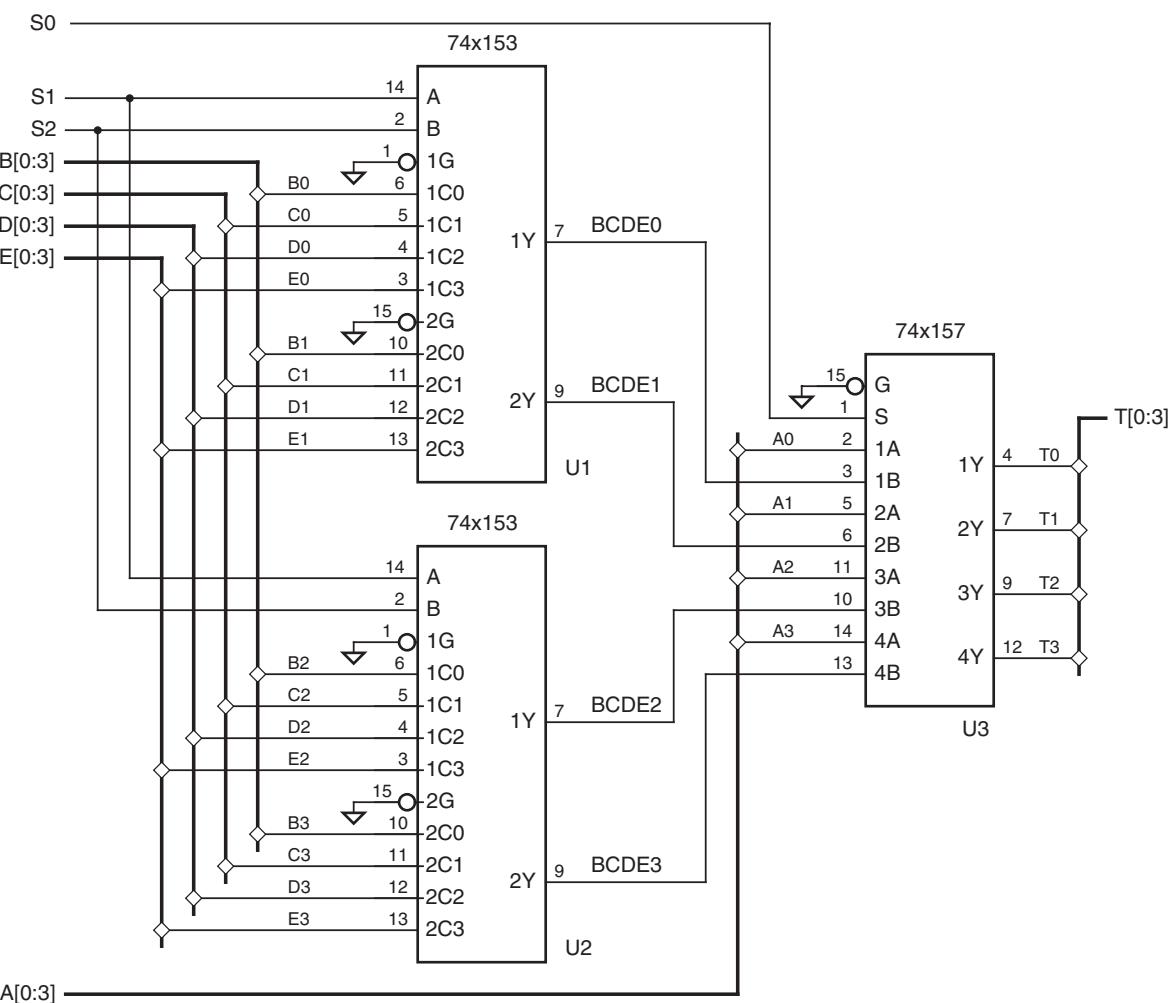
The delay through above barrel shifter is four times the delay through one 74x157. A faster barrel shifter can be built by cascading two 16-bit, four-input multiplexers, each of which looks at *two* select bits. This can be done with a total of 16 74x153s, and is probably the optimal solution to this problem in terms of cost/performance.

The fastest barrel shifter is built as a single 16-bit, 16-input multiplexer. A 1-bit, 16-input multiplexer can be built using two 74x151s or 74x251s, applying say S3 and its complement to the EN\_L inputs; with the '151s, a 2-input NAND is also required to combine the outputs. So this solution requires at least 32 packages total, but the data-path delay goes through just one package.

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3e5.91 6.77



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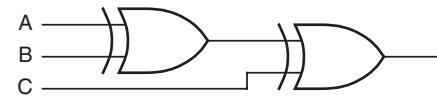
- 3e5.67 6.80 The '08 has the same pinout as the '00, but its outputs are the opposite polarity. The change in level at pin 3 of U1 is equivalent to a change at pin 4 of U2 (the input of an XOR tree), which is equivalent in turn to a change at pin 6 of U2 (the parity-generator output). Thus, the circuit simply generated and checked odd parity instead of even.

The change in level at pin 6 of U1 changed the active level of the ERROR signal.

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- 3e5.73 6.81 This is the actual circuit of an EO3 3-input XOR cell in LSI Logic's  
LCA 10000 series of CMOS gate arrays.



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- 3e5.68 6.82 The generally preferred structure is a tree, as in Figure 6–70(b). The worst-case delay for this structure is  $n$  XOR-gate delays. Note that *all* of the inputs have the same delay path to the output. This structure is preferred when all inputs arrive at about the same time, and delay must be minimized.

The second structure is a linear cascade, as in Figure 6–70(a). Its worst-case delay  $2^n - 1$  XOR-gate delays, which is greater than  $n$  for  $n > 1$  (and the structures are identical for  $n = 1$ ). Notice that some of the inputs (ones connected closer to the output gate) have a much shorter delay path to the output. This structure is preferred if one or a few ( $< n$ ) inputs arrive much later than the others, and the delay from their arrival until the output is valid must be minimized.

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- 3e5 .69    6.90 This problem is answered in Section 6.9.3 of the text, right before Figure 6-77, which makes it an easy answer for anyone who is paying attention.

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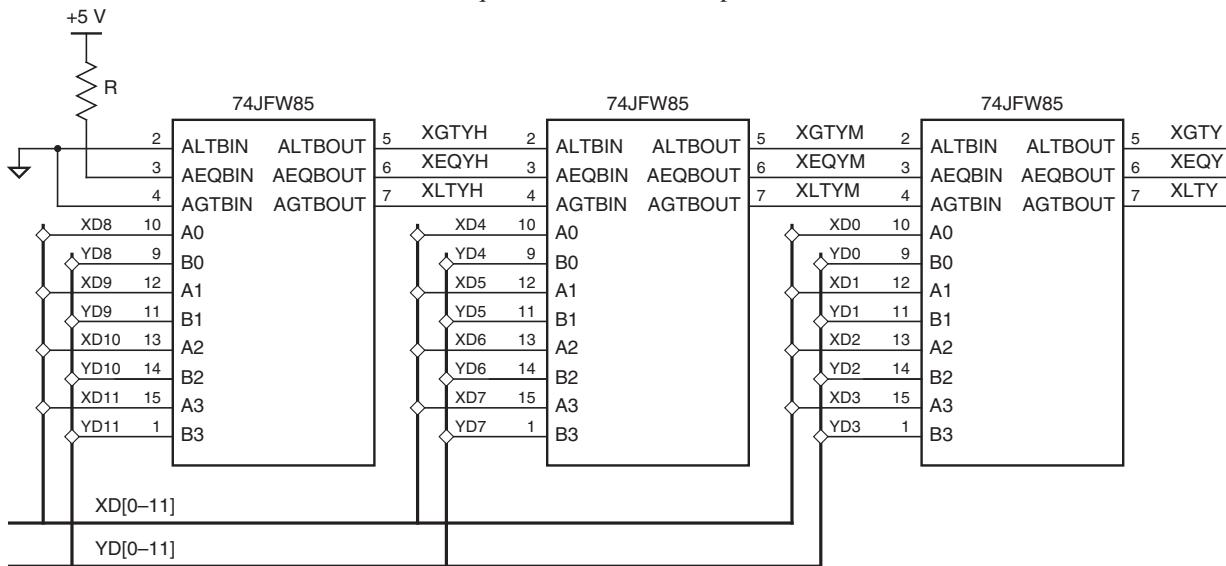
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- G5.271 6.92 The basic idea for this sort of design and some additional tricks are shown in the “application data” for the 74LS85 in the TI TTL Logic Data Book. The basic idea is to use the PGTQ\_L and PEQQ\_L outputs of 'LS682s at the first level into data inputs at the second level, which works out fine according to the following table:

Condition	First-level outputs		Second-level inputs	
	PGTQ_L	PEQQ_L	P <sub>i</sub>	Q <sub>i</sub>
impossible	0	0	d	d
P>Q	0	1	1	0
P<Q	1	1	0	1
P=Q	1	0	0	0

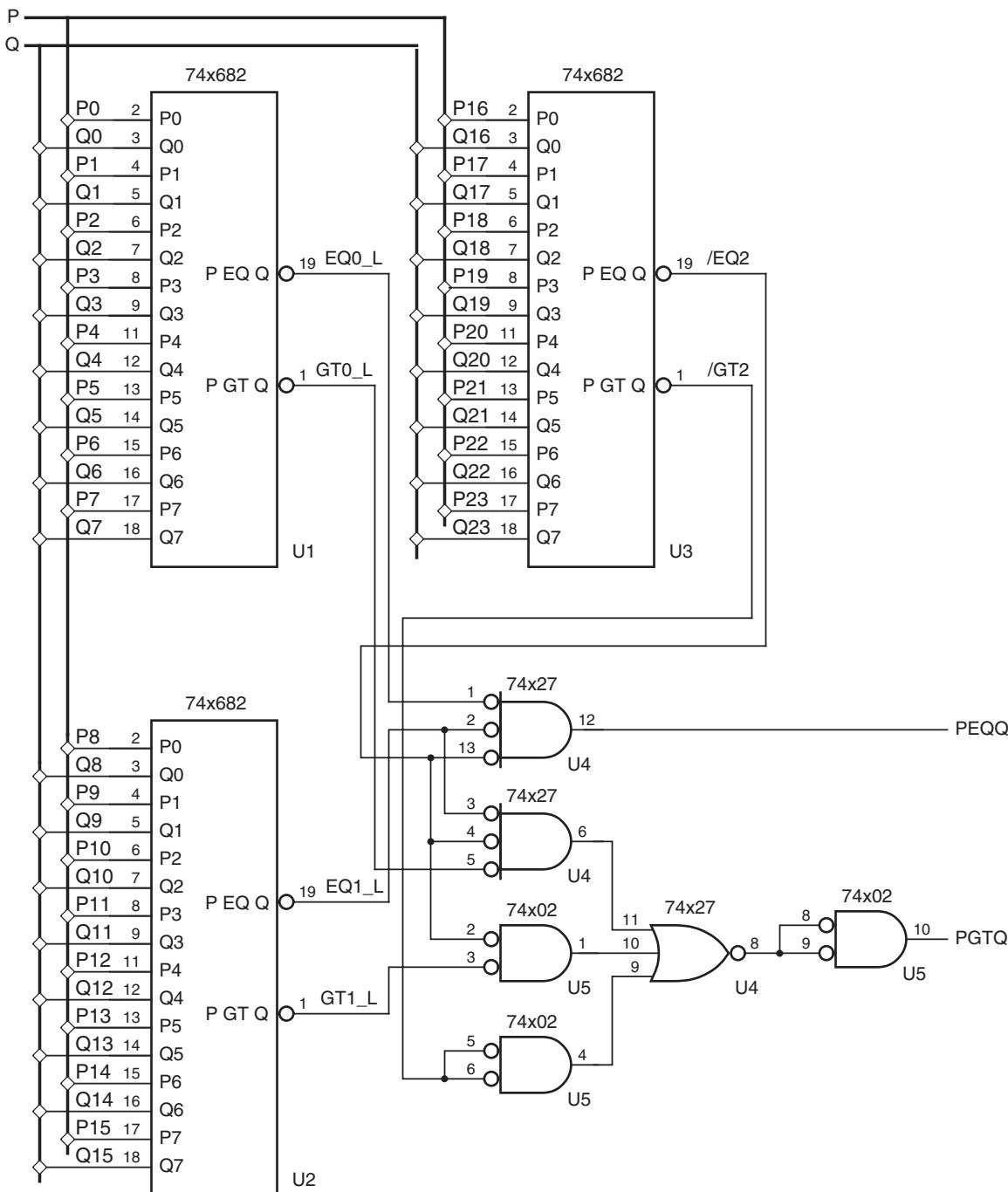
So, the outputs of the first-level 'LS682's need a little massaging before being applied to the inputs of the second-level 'LS682:  $P_i = \overline{PGTQ\_L}$ ' and  $Q_i = PGTQ\_L \cdot PEQQ\_L$ .

3e5.74 6.95 A truth table and the interconnection required for a 12-bit comparison are shown below.



Cascading inputs			Comparing inputs				Outputs		
AGTBIN	ALTBIN	AEQBIN	A3, B3	A2, B2	A1, B1	A0, B0	AGTBOUT	ALTBOUT	AEQBOUT
1	x	x	x	x	x	x	1	0	0
0	1	x	x	x	x	x	0	1	0
0	0	1	A3>B3	x	x	x	1	0	0
0	0	1	A3<B3	x	x	x	0	1	0
0	0	1	A3=B3	A2>B2	x	x	1	0	0
0	0	1	A3=B3	A2<B2	x	x	0	1	0
0	0	1	A3=B3	A2=B2	A1>B1	x	1	0	0
0	0	1	A3=B3	A2=B2	A1<B1	x	0	1	0
0	0	1	A3=B3	A2=B2	A1=B1	A0>B0	1	0	0
0	0	1	A3=B3	A2=B2	A1=B1	A0<B0	0	1	0
0	0	1	A3=B3	A2=B2	A1=B1	A0=B0	0	0	1
0	0	0	x	x	x	x	0	0	0

3e5.75 6.96



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- 3e5.93 6.97 The obvious solution is to use a 74FCT682, which has a maximum delay of 11 ns to its  $\overline{PEQQ}$  output. However, there are faster parts in Table 5–3. In particular, the 74FCT151 has a delay of only 9 ns from any select input to  $Y$  or  $\overline{Y}$ . To take advantage of this, we use a '138 to decode the SLOT inputs statically and apply the resulting eight signals to the data inputs of the '151. By applying GRANT[2–0] to the select inputs of the '151, we obtain the MATCH\_L output (as well as an active-high MATCH, if we need it) in only 9 ns!

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3e5.76 6.98 The worst-case delay is the sum of three numbers:

- (a) In U1–U4, the worst-case delay from any  $A_i, B_i$  to  $/G$  or  $/P$  (33 ns).
- (b) In U5, the worst-case delay from any  $/G_i$  or  $/P_i$  to any  $C_i$  (7 ns).
- (c) In U1–U4, the worst-case delay from  $CIN$  to any function output (27 ns).

Thus, the total worst-case delay is 67 ns.

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G5.276 6.99 The worst-case delay is the sum of three numbers:

- (a) In U1–U4, the worst-case delay from any  $A_i, B_i$  to  $/G$  or  $/P$  (33 ns).
- (b) In U5, the worst-case delay from any  $/G_i$  or  $/P_i$  to GALL\_L (10.5 ns).
- (c) In U5, the worst-case delay from any  $/P_i$  to PALL\_L (10 ns).
- (d) Thus, the total worst-case delay is 43.5 ns.

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G5.277 6.100

$$\begin{aligned} hs_3 &= g_3' \cdot p_3 \\ &= (A3' + B3') \cdot (A3 + B3) \\ &= A3 \oplus B3 \\ c_3 &= p_2 \cdot (p_1 + g_2) \cdot (p_0 + g_2 + g_1) \cdot (g_2 + g_1 + g_0) \text{ (Assuming } c_0 = 0) \\ &= p_2 \cdot p_1 \cdot (g_1 + g_0 \cdot p_0) + p_2 \cdot g_2 \\ &\quad (A2 + B2) \cdot (A1 + B1) \cdot [(A1 \cdot B1) + (A0 \cdot B0) \cdot (A0 + B0)] + (A2 + B2) \cdot (A2 \cdot B2) \\ &= (A2 + B2) \cdot (A1 + B1) \cdot [(A1 \cdot B1) + (A0 \cdot B0)] + (A2 \cdot B2) \\ &= (A2 + B2) \cdot (A1 + B1) \cdot (A1 \cdot B1) + (A2 + B2) \cdot (A1 + B1) \cdot (A0 \cdot B0) + (A2 \cdot B2) \\ &= (A2 + B2) \cdot (A1 \cdot B1) + (A2 + B2) \cdot (A1 + B1) \cdot (A0 \cdot B0) + (A2 \cdot B2) \\ &= (A2 + B2) \cdot (A1 \cdot B1 + A1 \cdot A0 \cdot B0 + B1 \cdot A0 \cdot B0) + A2 \cdot B2 \\ S3 &= hs_3 \oplus c_3 \\ &= A3 \oplus B3 \oplus [(A2 + B2) \cdot (A1 \cdot B1 + A1 \cdot A0 \cdot B0 + B1 \cdot A0 \cdot B0) + A2 \cdot B2] \end{aligned}$$

Substituting X's and Y's for A's and B's, this matches the result in Exercise 6.29.

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- 3e5.79 6.101 The function has 65 inputs, and the worst 65-input function (a 65-input parity circuit) has  $2^{65} - 1$  terms in the minimal sum-of-products expression. Our answer can't be any worse than this, but we can do better.

The expression for  $c_1$  has 3 product terms:  $c_1 = c_0 \cdot x_0 + c_0 \cdot y_0 + x_0 \cdot y_0$

The expression for  $c_2$  is  $c_2 = c_1 \cdot x_1 + c_1 \cdot y_1 + x_1 \cdot y_1$

If we substitute our previous expression for  $c_1$  in the equation above and "multiply out," we get a result with  $3 + 3 + 1 = 7$  product terms. Let us assume that no further reduction is possible.

Continuing in this way, we would find that the expression for  $c_3$  has  $7 + 7 + 1 = 15$  product terms and, in general, the expression for  $c_i$  has  $2^{i+1} - 1$  product terms.

Thus, the number of terms in a sum-of-products expression for  $c_{32}$  is no more than  $2^{33} - 1$ , fewer if minimization is possible.

With this encoding, we can determine that  $C0 = S2' + S1'$  and  $C1 = S1' + S0'$ ; thus, each can be realized with a single 2-input NAND gate.

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- G7 .201 7.1 (1) Bowling is the first sport that comes to mind. Have you ever watched a bowler's physical contortions "encourage" a metastable pin to find a horizontal stable state, instead of a vertical one?
- (2) Basketball games frequently have rim shots where the ball balances precariously on the rim, causing the crowd to scream:  
"Metastable ball! Help us win!"  
"Resolve your instability by falling in!"
- (3) Pass receivers in football invariably end up doing a little metastable dance as they run down the sideline.

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- 7.2 In ancient rome there was a poem  
About a dog who found two bones  
He picked at one  
He licked the other  
He went in circles  
He dropped dead

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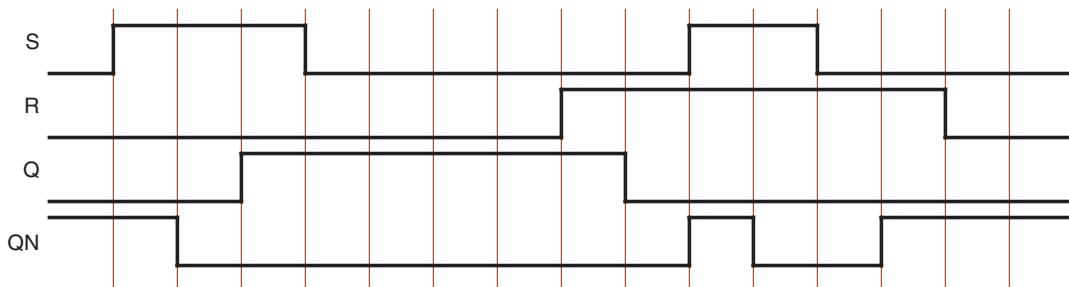
### 7.3 “Did You Ever Have To Make Up Your Mind”

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3e7.2

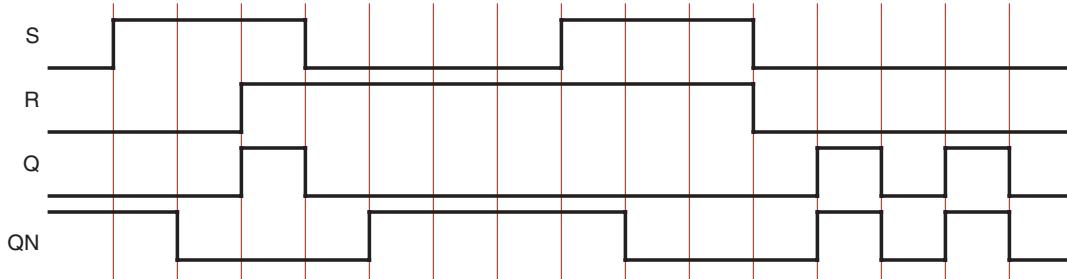
7.4



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- 3e7.3 7.5 The latch oscillates if S and R are negated simultaneously. Many simulator programs will exhibit this same behavior when confronted with such input waveforms.

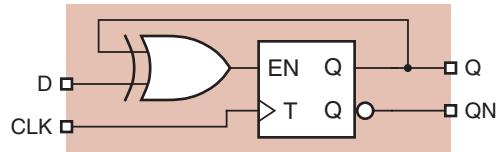


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3e7 .4

7.6

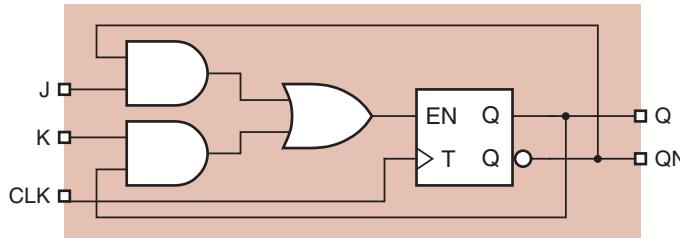


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3e7.5

7.7



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3e7 .6      7.8    Hook up S\_L and R\_L to the  $\overline{PR}$  and  $\overline{CLR}$  inputs, respectively. Ground CLK and D.

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- G7 .207 7.9 A master-slave flip-flop requires “one’s catching” during the time the C input is 1, but external combinational logic cannot perform this function (if it can, then it is not combinational). The student might be tempted to gate the clock before applying it to the 74x74 clock input, but that would cause the state to change immediately, instead of only at the rising edge of the clock.

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- 7.10 A master-slave flip-flop requires “one’s catching” during the time the C input is 1, but external combinational logic cannot perform this function (if it can, then it is not combinational). The student might be tempted to gate the clock before applying it to the 74x74 clock input, but that would cause the state to change immediately, instead of only at the rising edge of the clock.

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3e7.8

7.11 Just tie the J and  $\bar{K}$  inputs together and use as the D input.

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3e7.9 7.12 Excitation and output equations:

$$D_1 = Q_1' + Q_2$$

$$D_2 = Q_2' \cdot X$$

$$Z = Q_1 + Q_2'$$

Excitation/transition table; state/output table:

		EN		EN		
Q1	Q2	0	1	S	0	1
00		10	11	A	C	D
01		10	10	B	C	C
10		00	01	C	A	B
11		10	10	D	C	C
Q1* Q2*		S*				

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G7 .210 7.13 Excitation and output equations:

$$D_1 = Q_1' \cdot Q_2$$

$$D_2 = Q_2' + X'$$

$$Z = Q_1 \cdot Q_2'$$

Excitation/transition table; state/output table:

		X		X			
Q1	Q2	0	1	S	0	1	Z
00	01	01		A	B	B	0
01	11	10		B	D	C	0
10	01	01		C	B	B	1
11	01	00		D	B	A	0
		Q1*	Q2*	S*			

With respect to the original state table, the encodings have now been complemented. The observable behavior change is that the output has been complemented. One could say that it is complemented only when X=0, since the output appears to be a 1-0 sequence in both cases when X=1.

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3e7.15 7.18 Excitation equations:

$$D_2 = (Q_1 \oplus Q_0) \oplus (Q_1' \cdot Q_2')$$

$$D_1 = Q_2$$

$$D_0 = Q_1$$

Excitation/transition table; state table:

Q2	Q1	Q0	Q2*	Q1*	Q0*	S	S*
000			100			A	E
001			000			B	A
010			101			C	F
011			001			D	B
100			010			E	C
101			110			F	G
110			111			G	H
111			011			H	D

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G7.216 7.19 Excitation equations:

$$D_1 = X$$

$$D_2 = (Q_1 + Y) \cdot Q_3'$$

$$D_3 = Q_2' \cdot Y + Q_1'$$

Excitation/transition table; state table:

			X Y				X Y				
Q1	Q2	Q3	00	01	11	10	S	00	01	11	10
000	001	011	101	111			A	B	D	F	H
001	001	001	101	101			B	B	B	F	F
010	001	011	101	110			C	B	D	F	G
011	001	001	101	101			D	B	B	F	F
100	010	011	110	111			E	C	D	G	H
101	000	001	101	101			F	A	B	F	F
110	010	010	110	110			G	C	D	G	G
111	000	000	101	100			H	A	A	F	E
			Q1*	Q2*	Q3*						S*

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**3e7.19 7.20** Excitation and output equations:

$$EN1 = Y$$

$$EN2 = X' \cdot Y \cdot Q1$$

$$Z = X' \cdot Q2'$$

Note that the characteristic equation for a T flip-flop is  $Q^* = EN \cdot Q' + EN' \cdot Q$ . Thus, we obtain the following transition equations:

$$Q1^* = Y \cdot Q1' + Y1' \cdot Q1$$

$$Q2^* = X' \cdot Y \cdot Q1 \cdot Q2' + (X + Y' + Q1') \cdot Q2$$

Transition/output table; state/output table:

		XY						XY			
Q1	Q2	00	01	10	11	S	00	01	10	11	
00	00, 1	10, 1	00, 0	10, 0		A	A, 1	C, 1	A, 0	C, 0	
01	01, 0	11, 0	01, 0	11, 0		B	B, 0	D, 0	B, 0	D, 0	
10	10, 1	01, 1	10, 0	00, 0		C	C, 1	B, 1	C, 0	A, 0	
11	11, 0	00, 0	11, 0	01, 0		D	D, 0	A, 0	D, 0	B, 0	
		Q1*, Q2*, Z				S*, Z					

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- G7 .220 7.21 This can be done algebraically. If all of the input combinations are covered, the logical sum of the expressions on all the transitions leaving a state must be 1. If the sum is not 1, it is 0 for all input combinations that are uncovered. For double-covered input combinations, we look at all possible pairs of transitions leaving a state. The product of a pair of transition equations is 1 for any double-covered input combinations.
- (a) State B,  $Y = 0$  is uncovered, and state C,  $Y = 1$  is uncovered.
  - (b) State A,  $(X + Y) = 0$  is uncovered. State B,  $(W + X' + Y + Z') = 0$  is uncovered;  $(W \cdot Y + W \cdot Z' + X' \cdot Y + X' \cdot Z') = 1$  is double-covered. State C,  $(X + Y) = 0$  is uncovered;  $Y = 1$  is double covered. State D,  $(X \cdot Y' + W \cdot Z) = 0$  is uncovered;  $X \cdot Y' \cdot Z' = 1$  is double-covered;
  - (c) State A,  $(X' + Y + Z) = 0$  is uncovered;  $(X' \cdot Z + Y \cdot Z) = 1$  is double-covered. State C,  $(X + Y' + Z) = 0$  is uncovered;  $(X \cdot Z + Y' \cdot Z) = 1$  is double-covered. State D,  $(X + Y' + Z) = 0$  is uncovered;  $X \cdot Y' \cdot Z' = 1$  is double-covered.
  - (d) State A,  $(X + Y + Z) = 0$  is uncovered. State B,  $W' \cdot X \cdot Z' = 1$  is double-covered. State C,  $X' \cdot Y' \cdot Z = 1$  is double-covered. State D,  $(W + Y + Z) = 0$  is uncovered.

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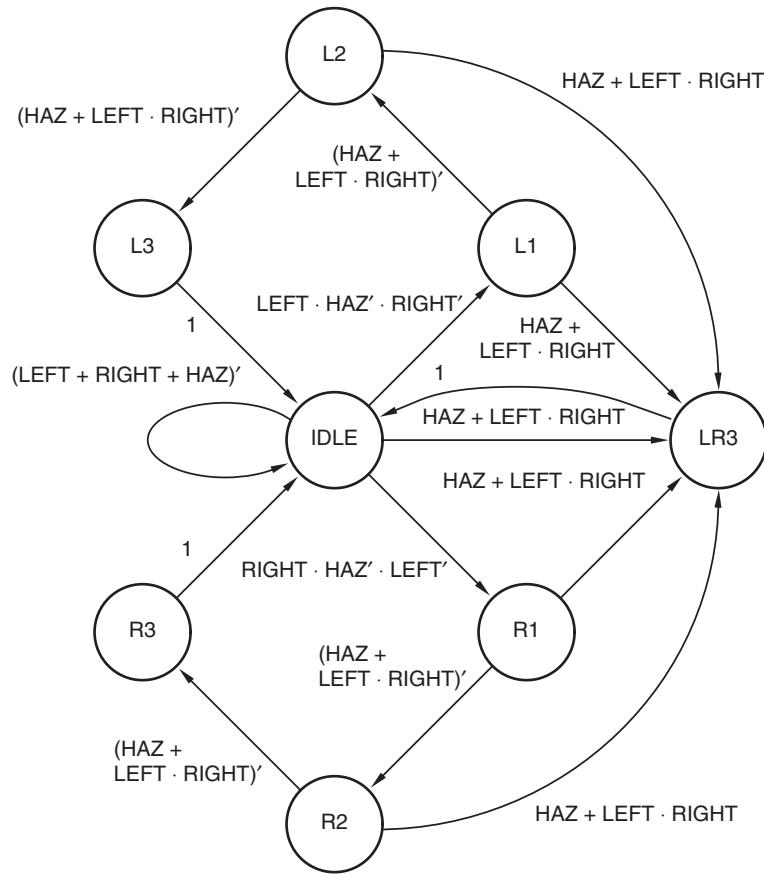
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**3e7 .21** **7.22** Table 9–4 on page 804 shows an output-coded state assignment. Here is a corresponding transition list:

S	L3Z	L2Z	L1Z	R1Z	R2Z	R3Z	Transition expression	S*	L3Z*	L2Z*	L1Z*	R1Z*	R2Z*	R3Z*
IDLE	0	0	0	0	0	0	(LEFT + RIGHT + HAZ)'	IDLE	0	0	0	0	0	0
IDLE	0	0	0	0	0	0	LEFT · HAZ' · RIGHT'	L1	0	0	1	0	0	0
IDLE	0	0	0	0	0	0	HAZ + LEFT · RIGHT	LR3	1	1	1	1	1	1
IDLE	0	0	0	0	0	0	RIGHT · HAZ' · LEFT'	R1	0	0	0	1	0	0
L1	0	0	1	0	0	0	HAZ'	L2	0	1	1	0	0	0
L1	0	0	1	0	0	0	HAZ	LR3	1	1	1	1	1	1
L2	0	1	1	0	0	0	HAZ'	L3	1	1	1	0	0	0
L2	0	1	1	0	0	0	HAZ	LR3	1	1	1	1	1	1
L3	1	1	1	0	0	0	1	IDLE	0	0	0	0	0	0
R1	0	0	0	1	0	0	HAZ'	R2	0	0	0	1	1	0
R1	0	0	0	1	0	0	HAZ	LR3	1	1	1	1	1	1
R2	0	0	0	1	1	0	HAZ'	R3	0	0	0	1	1	1
R2	0	0	0	1	1	0	HAZ	LR3	1	1	1	1	1	1
R3	0	0	0	1	1	1		IDLE	0	0	0	0	0	0
LR3	1	1	1	1	1	1		IDLE	0	0	0	0	0	0

The excitation equations and circuit diagram follow directly from this transition list.

G7 .223 7.24 The general shape of the state diagram does not change, but some of the transition expressions do:



S	Q2	Q1	Q0	Transition expression	S*	Q2*	Q1*	Q0*
IDLE	0	0	0	$(LEFT + RIGHT + HAZ)'$	IDLE	0	0	0
IDLE	0	0	0	$LEFT \cdot HAZ' \cdot RIGHT'$	L1	0	0	1
IDLE	0	0	0	$HAZ + LEFT \cdot RIGHT$	LR3	1	0	0
IDLE	0	0	0	$RIGHT \cdot HAZ' \cdot LEFT'$	R1	1	0	1
L1	0	0	1	$HAZ' \cdot (LEFT \cdot RIGHT)'$	L2	0	1	1
L1	0	0	1	$HAZ \cdot (LEFT \cdot RIGHT)'$	LR3	1	0	0
L1	0	0	1	$LEFT \cdot RIGHT$	IDLE	0	0	0
L2	0	1	1	$HAZ' \cdot (LEFT \cdot RIGHT)'$	L3	0	1	0
L2	0	1	1	$HAZ \cdot (LEFT \cdot RIGHT)'$	LR3	1	0	0
L2	0	1	1	$LEFT \cdot RIGHT$	IDLE	0	0	0
L3	0	1	0	1	IDLE	0	0	0
R1	1	0	1	$HAZ' \cdot (LEFT \cdot RIGHT)'$	R2	1	1	1
R1	1	0	1	$HAZ \cdot (LEFT \cdot RIGHT)'$	LR3	1	0	0
R1	1	0	1	$LEFT \cdot RIGHT$	IDLE	0	0	0
R2	1	1	1	$HAZ' \cdot (LEFT \cdot RIGHT)'$	R3	1	1	0
R2	1	1	1	$HAZ \cdot (LEFT \cdot RIGHT)'$	LR3	1	0	0
R2	1	1	1	$LEFT \cdot RIGHT$	IDLE	0	0	0
R3	1	1	0	1	IDLE	0	0	0
LR3	1	0	0	1	IDLE	0	0	0

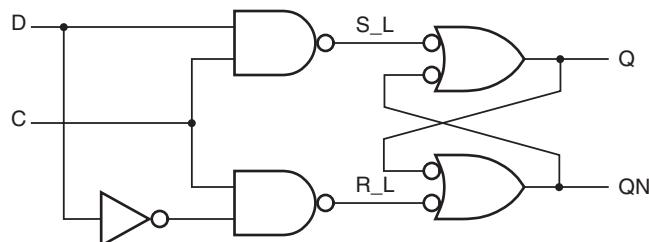
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- 3e7.24 7.38 Refer to the figure to the right. The details of metastability triggering depend on the details of the internal circuit timing.

For example, suppose that the inverter has non-zero delay, and that C and D are 1. Then when D changes from 1 to 0, both  $S_L$  and  $R_L$  will be asserted for a short time. If C changes from 1 to 0 during this time, then  $S_L$  and  $R_L$  will be negated simultaneously; this is analogous to the situation in the previous exercise.

On the other hand, let us assume for the sake of argument that the inverter has zero delay, and that C and D are 1. The feedback loop is in one of the stable states depicted in Figure 7–3. If D is changed from 1 to 0, and assuming that the delays through the NAND gates to  $S_L$  and  $R_L$  are equal, the “operating point” of the feedback loop starts moving toward the other stable state. However, if C is changed to 0 while this is happening, the circuit may stop halfway at the metastable operating point.



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- 3e7 .25 7.39 The minimum setup time is the clock period times the duty cycle. That is, the minimum setup time is the time that the clock is 1.

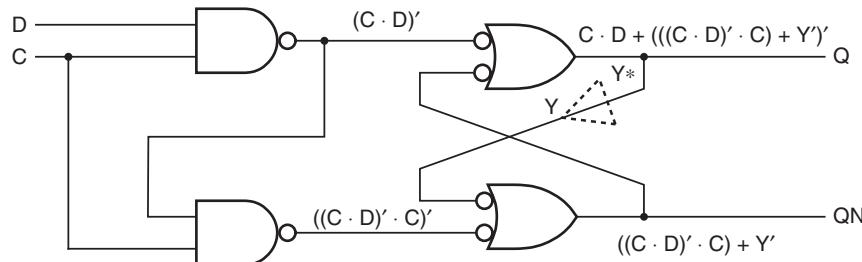
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3e7 .26 7.40 If both PR\_L and CLR\_L are asserted simultaneously, both Q and QN will be 1.

3e7.27 7.41 As shown in Section 7.9.1, the excitation equation for the latch of Figure 7-72 is  $Y^* = C \cdot D + C' \cdot Y + D \cdot Y$

Below, we analyze Figure X7.27 in the same way:



The feedback equation is

$$\begin{aligned}
 Y^* &= C \cdot D + (((C \cdot D)' \cdot C) + Y')' \\
 &= (C \cdot D) + ((C \cdot D)' \cdot C)' \cdot Y \\
 &= C \cdot D + ((C \cdot D) + C') \cdot Y \\
 &= C \cdot D + (D + C') \cdot Y \\
 &= C \cdot D + D \cdot Y + C' \cdot Y
 \end{aligned}$$

The feedback equations are the same, and so the circuits have identical steady-state behavior.

The circuit in Figure X7.27 is better in two ways. It uses one less gate, and it has one less load on the D input.

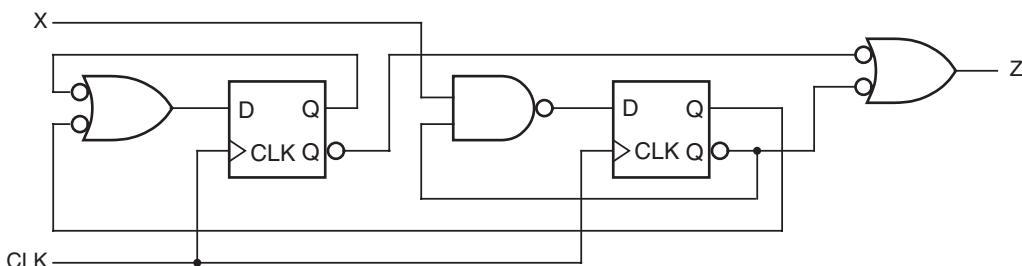
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- 3e7.29 7.42 The AND gate in the original circuit is replaced with a NAND gate. As a result, the second flip-flop stores the opposite of the value stored in the original circuit; to compensate, swap connections to its Q and QN outputs.

The OR gates in the original circuit are also replaced with NAND gates. As a result, each input must be connected to a signal of the opposite polarity as before, that is, to the complementary flip-flop output. In the case of connections to the second flip-flop, we swapped outputs twice, so the connections remain the same.

The final circuit below uses three 2-input NAND gates.



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- 3e7 .28 7.43 To simplify the problem, let us assume that the D input of a latch is stable at least at the rising edge of C. Without this assumption, we may have a situation where the D inputs for a particular clock tick stabilize *after* C goes HIGH. Although there is nothing inherent in the problem statement to exclude such a situation, analysis of this more general case is a little dicey (i.e., complicated).

At each clock tick, as soon as C goes HIGH, the latch outputs start changing and may propagate through the combinational logic back to the D inputs. Therefore, C must go LOW before this happens:

$$t_H < t_{CQ\min} + t_{F\min} - t_{hold}$$

That is, C is constrained to have a narrow HIGH-pulse width. If the minimum delay of the combinational logic or latch is not long enough, we'll be blown out of the water right here and will not be able to design a system in this way. This would typically be the case with discrete CMOS or TTL components, which is why systems are almost never designed this way!

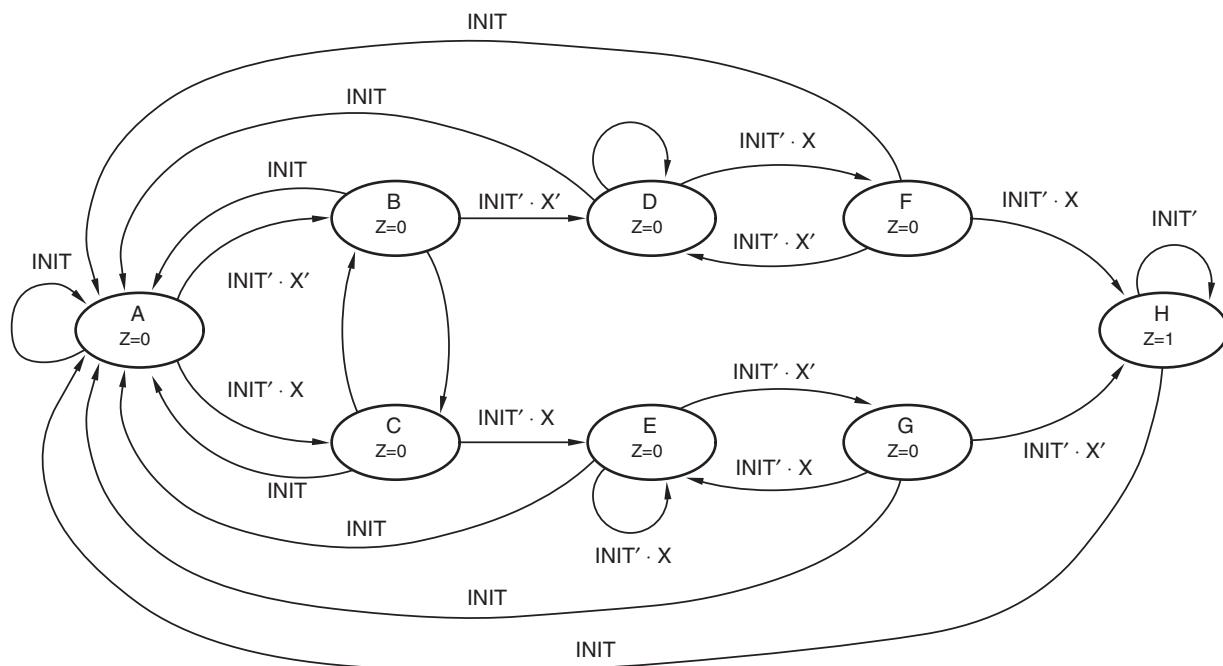
Continuing, we can write

$$\begin{aligned} \max(t_{CQ\max}, t_{DQ\max}) + t_{F\max} &< t_H + t_L \\ t_H &> t_{\text{setup}} \end{aligned}$$

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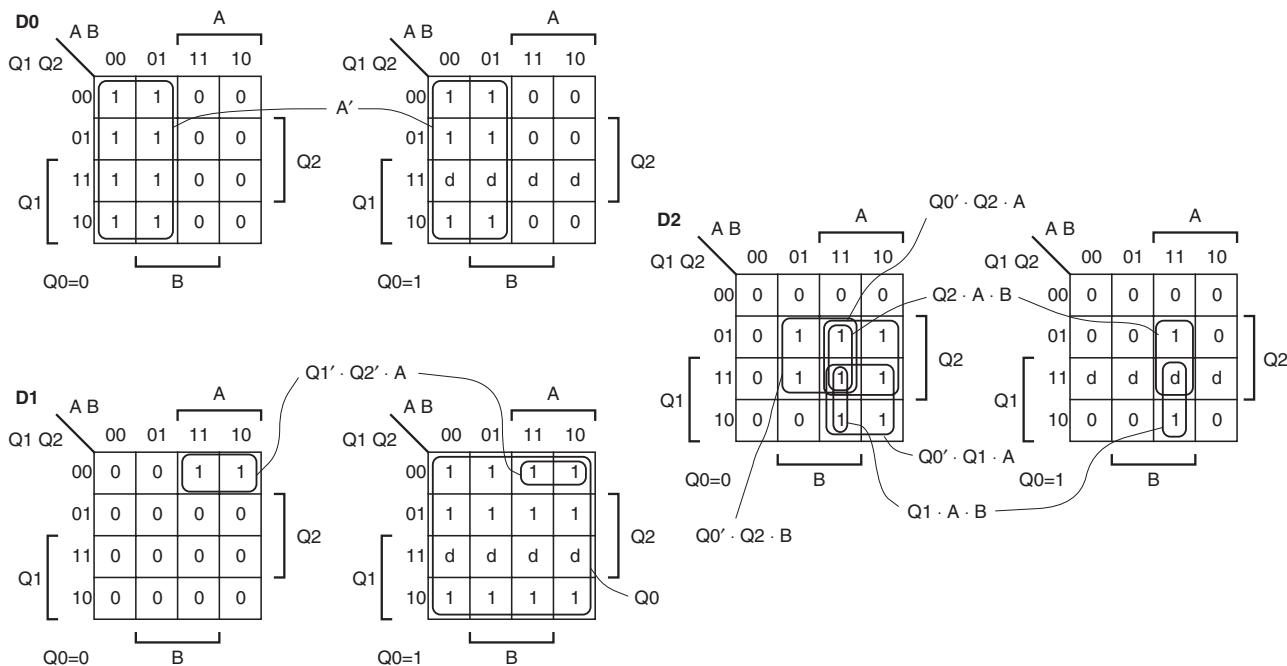
3e7 .30 7.44



3e7.45 7.50 A transition table corresponding to the state table is shown below:

			A B				
Q2 Q1 Q0			00	01	11	10	Z
		000	001	001	010	010	0
		001	011	011	010	010	0
		010	001	001	100	100	0
		011	011	011	110	010	1
		100	001	101	100	100	1
		101	011	011	110	010	1
		110	001	101	100	100	1
			Q2*	Q1*	Q0*		

This table leads to the following Karnaugh maps for the excitation logic, assuming a “minimal cost” treatment of unused states.



The resulting excitation equations are

$$D_0 = A'$$

$$D_1 = Q_1' \cdot Q_2' \cdot A + Q_0$$

$$D_2 = Q_2 \cdot A \cdot B + Q_0' \cdot Q_2 \cdot A + Q_0' \cdot Q_1 \cdot A + Q_1 \cdot A \cdot B + Q_0' \cdot Q_2 \cdot B$$

Ignoring inverters, a circuit realization with the new equations requires one 2-input gate, six 3-input gates, and one 5-input gate. This is more expensive than Figure 7–54, by four gates.

3e7 .47

- 7.51** In this application, we would have the RESET signal force the machine to state A0, and use the state table shown to the right:

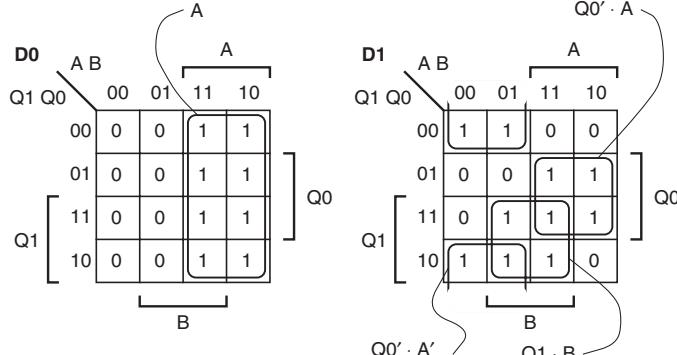
		A B				
S		00	01	11	10	Z
A0	OK0	OK0		A1	A1	0
A1	A0	A0		OK1	OK1	0
OK0	OK0	OK0		OK1	A1	1
OK1	A0	OK0		OK1	OK1	1

S\*

S	Q1	Q0
A0	0	0
A1	0	1
OK0	1	0
OK1	1	0

		A B				
Q1	Q0	00	01	11	10	Z
00	10	10	01	01	0	
01	00	00	11	11	0	
10	10	10	11	01	1	
11	00	10	11	11	1	

Q2\* Q1\* Q0\*

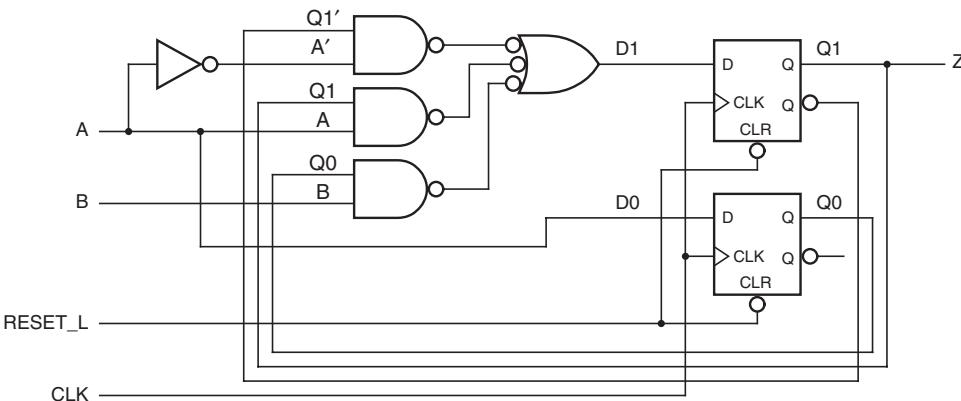


The corresponding excitation equations are

$$D_0 = A$$

$$D_1 = Q_0 \cdot A + Q_0' \cdot A' + Q_1 \cdot B$$

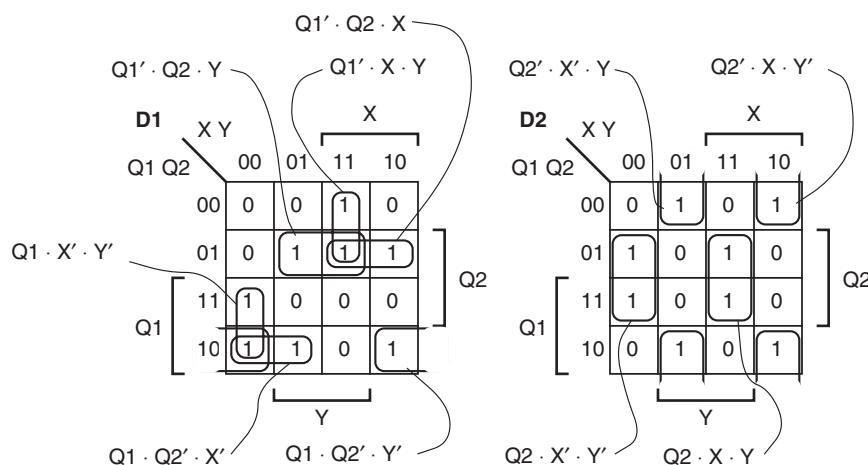
Finally, the logic diagram is:



Comparing with Figure 7–54, the cost of the excitation logic is almost the same (the difference is a 2-input gate vs. a 3-input gate). The big difference is in having one less flip-flop in the new design.

- 3e7.49 7.52 The new state assignment yields the following transition/excitation table and Karnaugh maps:

		X	Y					
		Q1	Q0	00	01	11	10	Z
		00	00	00	01	11	01	1
		01	01	01	11	10	11	0
		11	11	11	10	00	10	0
		10	10	10	00	01	00	0
				Q2*	Q1*	or D1	D2	



This yields the following excitation equations:

$$\begin{aligned} D1 &= Q1' \cdot Q2 \cdot X + Q1' \cdot Q2 \cdot Y + Q1' \cdot X \cdot Y + Q1 \cdot Q2' \cdot X' + Q1 \cdot Q2' \cdot Y' + Q1 \cdot X' \cdot Y' \\ D2 &= Q2 \cdot X \cdot Y + Q2' \cdot X \cdot Y' + Q2' \cdot X' \cdot Y + Q2 \cdot X' \cdot Y' \end{aligned}$$

Compared with the results of original state assignment, these equations require two more 3-input AND gates, plus a 6-input OR gate instead of a 4-input one. However, if we are not restricted to a sum-of-products realization, using the fact that  $D2 = Q2 \oplus X \oplus Y$  might make this realization less expensive when discrete gates are used.

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**7.56** Create a structural model for the circuit's combination logic—the output logic  $Z$  and excitation logic for the flip-flop inputs  $D1–D4$ . These are all functions of current state  $Q1–Q4$  and the inputs  $I1–I4$ . Write a test bench that instantiates this structural model. The body of the test bench includes a two nested `for` loops. The outer loop runs through all 16 possible values of  $D1–D4$ . The inner loop runs through all 16 possible values of  $I1–I4$ .

Each iteration of the inner loop simulates two clock cycles. At the first clock cycle, the current value of  $D1–D4$ , as determined by the outer-loop counter, is clocked into  $Q1–Q4$ . At the second clock cycle, the current value of  $I1–I4$ , as determined by the inner-loop counter, is applied to the structural model, along with the current value of  $Q1–Q4$ . After the clock tick, the next state appears in  $Q1–Q4$  and the value of  $Z$  is valid. These can be displayed, along with the values of the 4-bit loop counters that caused them. In this way, all 256 next-state entries and all 16 values of  $Z$  (a function of state only) can be displayed.

The method above simulates the operation of a hardware circuit that has a multiplexer on the state register's  $D$  inputs for testing purposes, taking one cycle to load a current state and another cycle to check the output of a particular state/input combination. Another approach would be to build a completely structural model that modified the state-machine circuit to include this multiplexer, and apply inputs accordingly.

But after you think about it a while, both approaches are more work than is needed. You don't need *any* flip-flops to get the information that you're looking for. All you need to do is to run the two nested four loops to create all 256 combinations of  $D1–D4$  and  $I1–I4$ ; apply the resulting sequence of 8-bit values to the structural model of the excitation and output logic; and display the resulting values.

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- 7.59 Refer to the machine's word description on page 554. The first part of the specification is a natural for finite-memory design—just use two flip-flops to keep track of the previous two values of A. If their outputs are equal, then Z should be 1.

For the second part of the specification, you might be tempted to store a bunch of previous values of B. But B may have been 1 for an arbitrarily large number of clock ticks since the last time the first condition was satisfied. So, the machine cannot be realized directly in this way as the finite-memory approach.

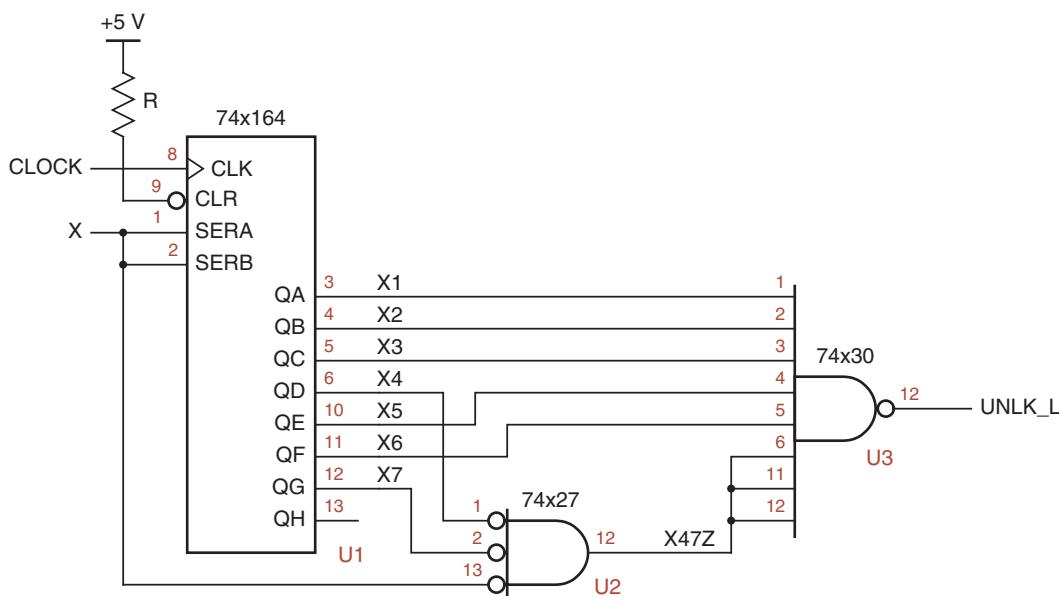
However, note that we also have the opportunity to remember past outputs. Suppose we provide two flip-flops that record the values of B and Z at the previous clock tick. According to the definition of the machine, if Z is 1, it must be so either because the previous two values of A were equal, or B had been 1 since the last time the first condition was true. Either way, if Z and B were both 1 at the previous clock edge, then it is correct to set Z to 1 in the current clock period.

So, the machine can be designed as a finite-memory machine. The complete design requires four flip-flops—two for the last two values of A, and one each for the last values of B and Z.

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- 3e7 .56 7.60 Compared to the standard state-table design in Section 7.4.6, the circuit below is a “no-brainer” to design, using a shift register to save the last seven values of X, and AND function to decode the unlocking combination. It might be preferred for that reason, even though it has more flip-flops. However, note that it only provides the UNLK output. The HINT output is a somewhat tougher to design, and is left as an exercise for the exercise-solution reader.



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3e7 .57

7.61 Here is the transition list:

S	Q2	Q1	Q0	Transition expression	S*	Q2*	Q1*	Q0*
IDLE	0	0	0	(LEFT+RIGHT+HAZ)'	IDLE	0	0	0
IDLE	0	0	0	LEFT	L1	0	0	1
IDLE	0	0	0	HAZ	LR3	1	0	0
IDLE	0	0	0	RIGHT	R1	1	0	1
L1	0	0	1	1	L2	0	1	1
L2	0	1	1	1	L3	0	1	0
L3	0	1	0	1	IDLE	0	0	0
R1	1	0	1	1	R2	1	1	1
R2	1	1	1	1	R3	1	1	0
R3	1	1	0	1	IDLE	0	0	0
LR3	1	0	0	1	IDLE	0	0	0

The transition/excitation and output equations below follow directly from the transition list.

$$\begin{aligned}
 D_2 = Q_2^* &= Q_2' \cdot Q_1' \cdot Q_0' \cdot HAZ \\
 &\quad + Q_2' \cdot Q_1' \cdot Q_0' \cdot RIGHT \\
 &\quad + Q_2 \cdot Q_1' \cdot Q_0 \\
 &\quad + Q_2 \cdot Q_1 \cdot Q_0 \\
 &= Q_2' \cdot Q_1' \cdot Q_0' \cdot (HAZ + RIGHT) + Q_2 \cdot Q_0
 \end{aligned}$$

$$\begin{aligned}
 D_1 = Q_1^* &= Q_2' \cdot Q_1' \cdot Q_0 \\
 &\quad + Q_2' \cdot Q_1 \cdot Q_0 \\
 &\quad + Q_2 \cdot Q_1' \cdot Q_0 \\
 &\quad + Q_2 \cdot Q_1 \cdot Q_0 \\
 &= Q_0
 \end{aligned}$$

$$\begin{aligned}
 D_0 = Q_0^* &= Q_2' \cdot Q_1' \cdot Q_0' \cdot LEFT \\
 &\quad + Q_2' \cdot Q_1' \cdot Q_0' \cdot RIGHT \\
 &\quad + Q_2' \cdot Q_1' \cdot Q_0 \\
 &\quad + Q_2 \cdot Q_1' \cdot Q_0 \\
 &= Q_2' \cdot Q_1' \cdot Q_0' \cdot (LEFT + RIGHT) + Q_1' \cdot Q_0
 \end{aligned}$$

Starting from the IDLE state, the following transitions may be observed:

S	Q2	Q1	Q0	LEFT	RIGHT	HAZ	Q2*	Q1*	Q0*	S*
IDLE	0	0	0	1	0	1	1	0	1	R1
IDLE	0	0	0	0	1	1	1	0	1	R1
IDLE	0	0	0	1	1	0	1	0	1	R1
IDLE	0	0	0	1	1	1	1	0	1	R1

For each input combination, the machine goes to the R1 state, because R1's encoding is the logical OR of the encodings of the two or three next states that are specified by the ambiguous state diagram.

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The behavior above is not so good and is a result of synthesis choices—state encoding and logic synthesis method. If a different state encoding were used for R1, or if a different synthesis method were used (e.g., product-of-s-terms), then the results could be different. For example, starting with the transition list given earlier, we can obtain the following set of transition equations using the product-of-s-terms method:

$$\begin{aligned} D2 = Q2^* &= (Q2 + Q1 + Q0 + LEFT + RIGHT + HAZ) \\ &\quad \cdot (Q2 + Q1 + Q0 + LEFT') \\ &\quad \cdot (Q2 + Q1 + Q0') \\ &\quad \cdot (Q2 + Q1' + Q0') \\ &\quad \cdot (Q2 + Q1' + Q0) \\ &\quad \cdot (Q2' + Q1' + Q0) \\ &\quad \cdot (Q2' + Q1 + Q0) \\ &= (Q2 + Q1 + RIGHT + HAZ) \cdot (Q2 + Q1 + LEFT') \cdot (Q2 + Q0') \cdot (Q1' + Q0) \cdot (Q2' + Q0) \end{aligned}$$

$$\begin{aligned} D1 = Q1^* &= (Q2 + Q1 + Q0 + LEFT + RIGHT + HAZ) \\ &\quad \cdot (Q2 + Q1 + Q0 + LEFT') \\ &\quad \cdot (Q2 + Q1 + Q0 + HAZ') \\ &\quad \cdot (Q2 + Q1 + Q0 + RIGHT') \\ &\quad \cdot (Q2 + Q1' + Q0) \\ &\quad \cdot (Q2' + Q1' + Q0) \\ &\quad \cdot (Q2' + Q1 + Q0) \\ &= (Q2 + Q1 + Q0) \cdot (Q1' + Q0) \cdot (Q2' + Q0) \end{aligned}$$

$$\begin{aligned} D0 = Q0^* &= (Q2 + Q1 + Q0 + LEFT + RIGHT + HAZ) \\ &\quad \cdot (Q2 + Q1 + Q0 + HAZ') \\ &\quad \cdot (Q2 + Q1' + Q0') \\ &\quad \cdot (Q2 + Q1' + Q0) \\ &\quad \cdot (Q2' + Q1' + Q0') \\ &\quad \cdot (Q2' + Q1' + Q0) \\ &\quad \cdot (Q2' + Q1 + Q0) \\ &= (Q2 + Q0 + LEFT + RIGHT) \cdot (Q2 + Q0 + HAZ') \cdot (Q1') \cdot (Q2' + Q0) \end{aligned}$$

These equations yield the following transitions:

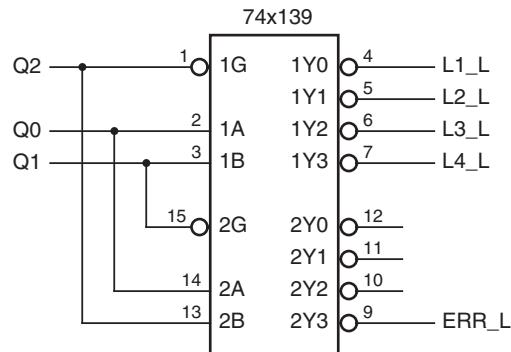
S	Q2	Q1	Q0	LEFT	RIGHT	HAZ	Q2*	Q1*	Q0*	S*
IDLE	0	0	0	1	0	1	0	0	0	IDLE
IDLE	0	0	0	0	1	1	1	0	0	LR3
IDLE	0	0	0	1	1	0	0	0	1	L1
IDLE	0	0	0	1	1	1	0	0	0	IDLE

This is obviously different and still not particularly good behavior.

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3e7 .64    7.62



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3e7 .65 7.63 Zero, One, Two, Three, Four, Five, Six

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- 3e7 .58    7.66 Let  $E(SB)$ ,  $E(SC)$ , and  $E(SD)$  be the binary encodings of states SB, SC, and SD respectively. Then  $E(SD) = E(SB) + E(SC)$  , the bit-by-bit logical OR of  $E(SB)$  and  $E(SC)$ . This is true because the synthesis method uses the logical OR of the next values for each state variable and, by extension, the logical OR of the encoded states.

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- 3e7 .59    7.67 This result is the dual of the preceding result. That is,  $E(SD) = E(SB) \cdot E(SC)$  , the bit-by-bit logical AND of  $E(SB)$  and  $E(SC)$ . This is true because  $V^* = 0$  for either state is sufficient to force a 1 in the  $V^{*'}'$  expression, so both must be 1 to get a 0 in the  $V^{*'}'$  expression (and a 1 in the resulting  $V^*$ ).

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- 3e7 .60 7.68 Since the synthesis method uses a logical OR of terms where  $V^*$  is specified to be 1, an unspecified state/input combination yields a next state of 00...0.

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3e7 .61 7.69 Once again, we get a dual result; an unspecified state/input combination yields a next state of 11...1.

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- 3e7.72    7.73 Because of the feedback loop, the adder is really a sequential circuit. For most input combinations, the output value (and state) is a function of the input only. However, when one operand is the bit-by-bit complement of the other, the output value and state depends on the last value stored in the feedback loop, and the sum output can be 0000 or 1111.

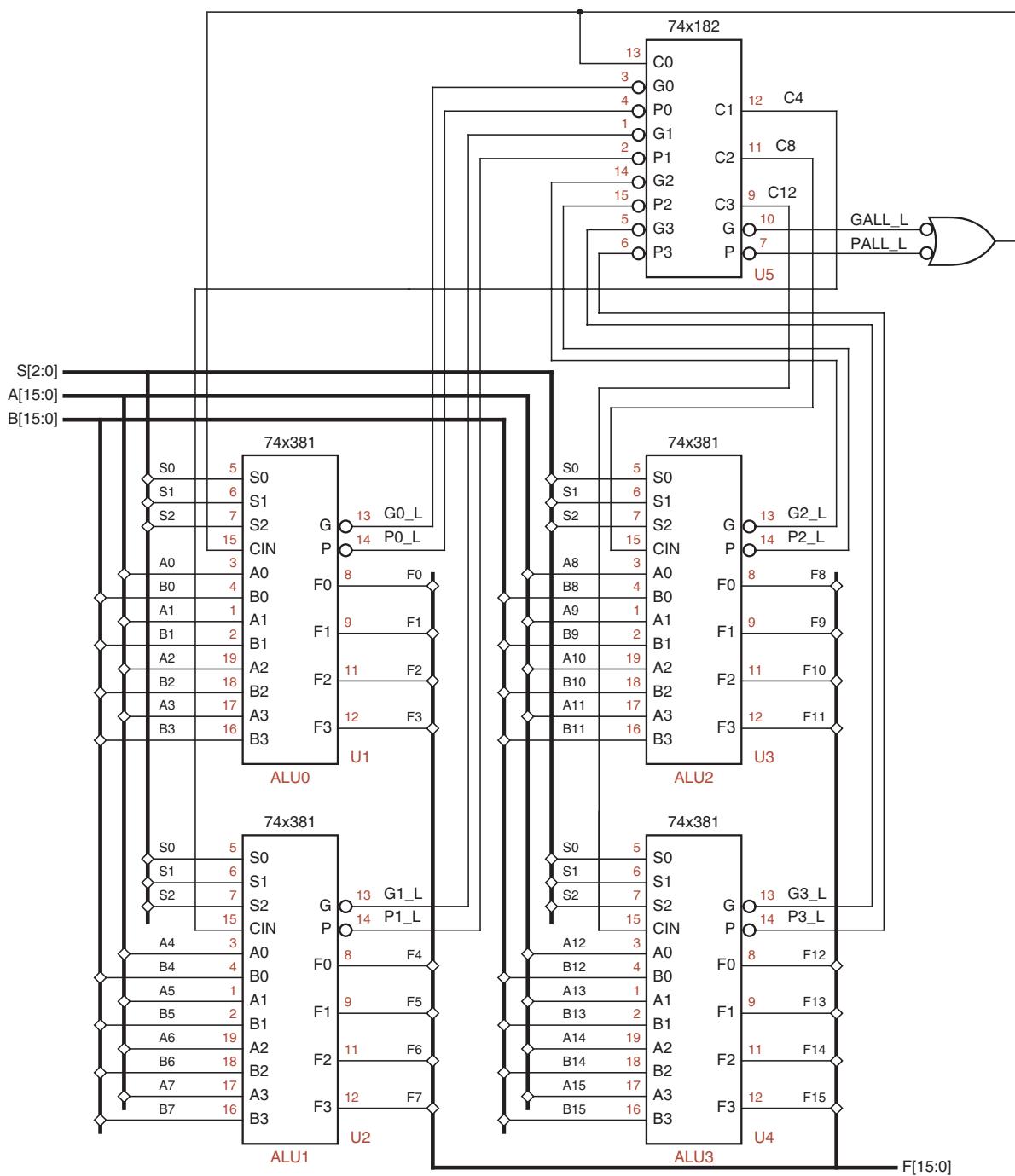
That is, suppose the operands are the bit-by-bit complements of each other, and the carry into the low-order bit of the adder is currently 0. Then the sum output is 1111, and the carry out stays at 0, so the feedback loop is stable, storing a carry of 0. Suppose, however, that the operands are the same but the carry into the low-order bit happens to be 1 (say, from the previous addition). Then that carry ripples through the adder, creating a sum output of 0000, and a carry out of 1. So the feedback loop is again stable, but this time it stores a carry of 1.

- G7 .272 7.74 This problem is derived from one of the author's old articles, "One's complement adder eliminates unwanted zero," by John F. Wakerly, *Electronics*, Vol. 49, No. 3, pp. 103-105, February 5, 1976.

The solution requires just one 2-input NAND gate, as shown below. It relies on the fact that the generate and propagate outputs of both the '181s and the '182 are unaffected by their respective carry inputs.

If the 16-bit sum, ignoring the carry into the low-order stage, is 11...11, then the '182's P output will be asserted. Similarly, the 16-bit addition would generate a carry, then the '182's G output will be asserted. The NAND gate's output is 1 in either of these cases, and forces the "end-around carry" into the low-order '181 as well as into the low-order carry input of the '182, which then creates the appropriate carries into the higher-order '181s.

It is useful to note that this adder is still slower than a two's complement adder built from the same components, since the carry inputs into '181s are now delayed by the additional delay on the C0 input of the '182—the time for its G and P outputs to be stable and propagate through the NAND gate.



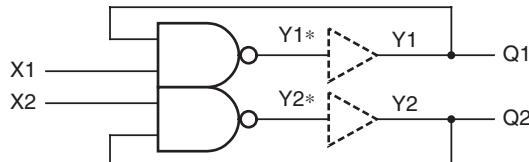
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3e7.74

7.76 Such a circuit would oscillate when the forcing term is 0 and the holding term is 1.

- 3e7 .68 7.77 As far as I know, I was the first person to propose BUT-flops, and Glenn Trewitt was the first person to analyze them, in 1982. To analyze, we break the feedback loops as shown in the figure to the right.



The excitation and output equations are

$$\begin{aligned}Y_1 &= [(X_1 \cdot Y_1) \cdot (X_2 \cdot Y_2)']' \\&= X_1' + Y_1' + X_2 \cdot Y_2\end{aligned}$$

$$\begin{aligned}Y_2 &= [(X_2 \cdot Y_2) \cdot (X_1 \cdot Y_1)']' \\&= X_2' + Y_2' + X_1 \cdot Y_1\end{aligned}$$

$$Q_1 = Y_1$$

$$Q_2 = Y_2$$

The corresponding transition/state table is

		X <sub>1</sub> X <sub>2</sub>			
Y <sub>1</sub>	Y <sub>2</sub>	00	01	11	10
00	11	11	11	11	11
01	11	11	10	10	11
11	11	(11)	10	(11)	01
10	11	11	01	01	01

Y <sub>1</sub> *	Y <sub>2</sub> *
Y <sub>1*</sub>	Y <sub>2*</sub>

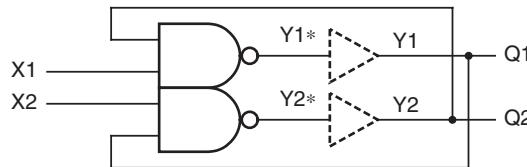
The two stable total states are circled. Notice that state 00 is unreachable.

When  $X_1 X_2 = 00$  or  $11$ , the circuit generally goes to stable state  $11$ , with  $Q_1 Q_2 = 11$ . The apparent oscillation between states  $01$  and  $10$  when  $X_1 X_2 = 11$  may not occur in practice, because it contains a critical race that tends to force the circuit into stable state  $11$ .

When  $X_1 X_2 = 01$  or  $10$ , the  $Q$  output corresponding to the HIGH input will oscillate, while the other output remains HIGH.

Whether this circuit is useful is a matter of opinion.

G7.269 7.78 Break the feedback loops as shown in the figure to the right.



The excitation and output equations are

$$\begin{aligned}Y_1 &= [(X_1 \cdot Y_1) \cdot (X_2 \cdot Y_1)]' \\&= X_1' + Y_1' + X_2 \cdot Y_1 \\&= X_1' + Y_1' + X_2 \\Y_2 &= [(X_2 \cdot Y_1) \cdot (X_1 \cdot Y_1)]' \\&= X_2' + Y_1' + X_1 \cdot Y_1 \\&= X_2' + Y_1' + X_1 \\Q_1 &= Y_1 \\Q_2 &= Y_2\end{aligned}$$

The corresponding transition/state table is

		X1 X2			
Y1	Y2	00	01	11	10
00		11	11	11	11
01		11	11	11	11
11		(11)	10	(11)	01
10		11	(10)	11	01
		Y1* Y2*			

The stable total states are circled. Notice that state 00 is unreachable. State 01 is reachable when the input is 10, but then it oscillates with State 11. State 11 is reached whenever the inputs are equal (00 or 11). State 10 is reached whenever the input is 01.

This circuit is an excellent “simultaneous change detector”, should one be in the market for such a device. If the inputs are 00, 01, or 11, then output is stable and strictly a function of the input. However, the gate has the unique property that if the input is 10, the state oscillates between 01 and 11. If either input is changed, the state goes to 11. BUT! If both inputs are changed simultaneously, the state goes to 10, thus indicating that the inputs changed at the same moment.

- (1) Starting with the inputs at 1 and the latch in stable state 01 or 10, the circuit can get stuck in stable state 11 if a short 0-pulse is applied to either input.
- (2) Starting with the inputs at 0 and the latch in stable state 11, the circuit can remain stuck in stable state 11 if the inputs are changed to 1 simultaneously.

Interestingly, these are both situations that could send a normal  $\overline{S}$ - $\overline{R}$  latch into the metastable state, but the race conditions in this circuit may send it to a stable state (note that metastability can still occur in other ways).

- G7.270 7.79 There is a feedback loop in this circuit, so it is really a sequential circuit. For most input combinations, the output value (and state) is a function of the input only. However, when all of the inputs are 1, the output oscillates. A proper BUT gate (Is a BUT gate ever proper??) gives a 00 output in this case.

- 7.80 The output of a D latch may become metastable if too short a positive pulse is applied to the C input, and the D input is the opposite of the current Q output. This creates a condition where too short of a set or reset pulse is applied to the internal S-R latch. The C input must be asserted for at least a minimum time, usually specified as the “minimum pulse width” for C.

3e7.71 7.87 When  $X=1$ , the circuit was supposed to “count” through its eight states in Gray-code order. When  $X=0$ , it remains in the current state. If this were the case, I suppose it could be used as a 3-bit random number generator. However, I messed up on the logic diagram, and the circuit actually does something quite different and completely useless, compared to what I intended when I wrote the problem. Someday I may fix this problem, but since very few readers study feedback sequential circuits, I feel no urgency to do so. Metastability may occur when  $X$  is changed from 1 to 0.

3e7.90 7.98 Either this exercise is a joke, or a correct answer is much too dangerous to publish. Nevertheless, Earl Levine offers two possible answers:

- (Stable output) Was the last answer to this question “yes”?
- (Oscillating output) Was the last answer to this question “no”?

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- 3e8.1    8.2 The new expression describes exactly the input combinations in which the 8 high-order bits of ABUS are 00000001<sub>2</sub>, the same as the original expression using don't-cares.

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- 3e8.3 8.3 There are  $64 \times 32 = 2048$  fuses in the AND array (for example, see Figure 8–18). Each of the eight macrocells has one fuse to control the output polarity and one fuse to select registered vs. combinational configuration in the 16V8R, or to assert the output-enable in the 16V8S. There are also two global fuses to select the overall configuration (16V8C, 16V8R, or 16V8S). The total number of fuses is therefore  $2048 + 16 + 2 = 2066$ . A real 16V8 (depending on the manufacturer) has at least 64 additional fuses to disable individual product terms, 64 user-programmable fuses that do nothing but store a user code, and a security fuse. (Once the security fuse is programmed, the rest of the fuse pattern can no longer be read.)

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- 3e8.4 8.4 There are  $132 \times 44 = 5808$  fuses in the AND array (see Figure 8–19). Each of the ten macrocells has one fuse to control the output polarity and one fuse to select registered vs. combinational configuration. The total number of fuses is therefore  $5808 + 20 = 5828$ .

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3e8.5

8.5 The  $f_{maxE}$  column below gives the answers in MHz.

Part numbers	Suffix	$t_{PD}$	$t_{CO}$	$t_{CF}$	$t_{SU}$	$t_H$	$f_{maxE}$	$f_{maxI}$
PAL16L8, PAL16Rx, PAL20L8, PAL20Rx	-5	5	4	—	4.5	0	117.7	117.7
PAL16L8, PAL16Rx, PAL20L8, PAL20Rx	-7	7.5	6.5	—	7	0	74.1	74.1
PAL16L8, PAL16Rx, PAL20L8, PAL20Rx	-10	10	8	—	10	0	55.6	55.6
PAL16L8, PAL16Rx, PAL20L8, PAL20Rx	B	15	12	—	15	0	37.0	37.0
PAL16L8, PAL16Rx, PAL20L8, PAL20Rx	B-2	25	15	—	25	0	25.0	25.0
PAL16L8, PAL16Rx, PAL20L8, PAL20Rx	A	25	15	—	25	0	25.0	25.0
PALCE16V8, PALCE20V8	-5	5	4	—	3	0	142.9	142.9
GAL16V8, GAL20V8	-7	7.5	5	3	5	0	100.0	125.0
GAL16V8, GAL20V8	-10	10	7.5	6	7.5	0	66.7	74.1
GAL16V8, GAL20V8	-15	15	10	8	12	0	45.5	50.0
GAL16V8, GAL20V8	-25	25	12	10	15	0	37.0	45.5
PALCE22V10	-5	5	4	—	3	0	142.9	142.9
PALCE22V10	-7	7.5	4.5	—	4.5	0	111.1	111.1
GAL22V10	-10	10	7	2.5	7	0	71.4	105.3
GAL22V10	-15	15	8	2.5	10	0	55.6	80.0
GAL22V10	-25	25	15	13	15	0	33.3	35.7

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3e8.6 8.6 The  $f_{maxI}$  column above gives the answers in MHz.

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3e8.7 8.7 See the ABEL program Z74x374 in the accompanying .zip file.

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- G8.208 8.8 Among the devices offered, only a 22V10 can realize the 74x175's functionality, because of the need for an asynchronous clear. See the ABEL program Z74x175 in accompanying .zip file. Four flip-flops are used for the Q outputs, and combinational logic is used to realize QN outputs. One might be tempted to use registered outputs for the QN outputs. If do this, you must be careful to provide the correct functionality when the CLR\_L input is asserted. This is done in the Z74x175R program in accompanying .zip file using istype statements to force the correct usage of the flip-flops. Actually, to be on the safe side, you should do this in the Z74x175 program as well (to prevent the compiler from using the reverse-polarity equations).

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- 3e8.9 8.9 In Figure 8-15, the delay from G to Q is 8.5 ns, and the 16V8 decoder delay is 10 ns, for a total of 18.5 ns. In Figure 8-16, the delay from G to the decoded outputs is just one pass through the 16V8, or 10 ns.

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- 3e8.10 8.10 If EN or CLK is 0, the output will be stable. If both are 1, the results are unpredictable, since they depend on circuit timing. It is certain that the circuit's output will be unstable as long as this condition is true.

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- 3e8.11 8.11 The counter is modified to return to a count of 0 when count 9 is reached. See the ABEL program Z74x162 in the accompanying .zip file.

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- 8.12 The CLR input is changed to asynchronous. Since the 74x161 needs an asynchronous clear, the design no longer fits in a 16V8 and we need to move to a 22V10. See the ABEL program Z74X161 in the accompanying .zip file.

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- 3e8.13 8.13 The counting direction is controlled by QD: count up when QD=1, count down when QD=0. A load occurs when the counter is in the terminal state, 1111 when counting up, 0000 when counting down. The MSB is complemented during a load and the other bits are unchanged.

Let us assume that the counter is initially in one of the states 0000–0111. Then the counter counts down (QD=0). Upon reaching state 0000, it loads 1000 and subsequently counts up (QD=1). Upon reaching state 1111, the counter loads 0111, and subsequently counts down, repeating the cycle.

If the counter is initially in one of the states 1000–1111, the same cyclic behavior is observed. The counting sequence has a period of 16 and is, in decimal,

$$8, 9, 10, 11, 12, 13, 14, 15, 7, 6, 5, 4, 3, 2, 1, 0, 8, 9, \dots$$

If only the three LSBs are observed, the sequence is

$$0, 1, 2, 3, 4, 5, 6, 7, 7, 6, 5, 4, 3, 2, 1, 0, 0, 1, \dots$$

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G8.216 8.14 The counting sequence is 0, 1, 2, 3, 4, 5, 8, 9, 10, 0, 1, 2, 3, 4, 5, 8 ....

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- 3e8.17 8.15 The path from the Q1 counter output (B decoder input) to the Y2\_L output has 10 ns more delay than the Q2 and Q0 (C and A) paths. Let us examine the possible Y2\_L glitches in Figure 8–43 with this in mind:
- 3→4 (011→100) Because of the delay in the Q1 path, this transition will actually look like 011→110→100. The Y6\_L output will have a 10-ns glitch, but Y2\_L will not.
- 7→0 (111→000) Because of the delay in the Q1 path, this transition will actually look like 111→010→000. The Y2\_L output will have a 10-ns glitch, but the others will not.

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- G8.218 8.16 Although the problem requested only the first 10 states are required, here is the entire sequence:  
00001, 10000, 01000, 00100, 10010, 01001, 10100, 11010, 01101, 00110, 10011, 11001, 11100, 11110, 11111,  
01111, 00111, 00011, 10001, 11000, 01100, 10110, 11011, 11101, 01110, 10111, 01011, 10101, 01010, 00101,  
00010, 00001, (repeats)

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- 3e8.20 8.19 The synchronizer fails if META has not settled by the beginning of the setup-time window for FF2, which is 5 ns before the clock edge. Since the clock period is 40 ns, the available metastability resolution time is 35 ns. The MTBF formula is

$$\text{MTBF}(t_r) = \frac{\exp(t_r/\tau)}{T_0 \cdot f \cdot a}$$

Substituting the proper values of  $\tau$  and  $T_0$  for the 'F74, and of  $f$  and  $a$  for the problem, we calculate

$$\text{MTBF}(35\text{ns}) = \frac{\exp(35/0.4)}{2.0 \cdot 10^{-4} \cdot 10^6 \cdot 10^6} \approx 2 \cdot 10^{28}\text{s}$$

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- G8.221 8.20 In this circuit, FF3 is a divide-by-two counter, and the clock frequency applied to FF1 and FF2 is only 15 MHz. With a 66.7-ns clock period and a 10-ns setup time requirement on FF2, the available metastability resolution time is 56.7 ns. Thus, we calculate

$$MTBF(70\text{ns}) = \frac{\exp(56.7/1.0)}{8.7 \cdot 10^{-6} \cdot 15 \cdot 10^6 \cdot 2 \cdot 10^6} \approx 1.6 \cdot 10^{16} \text{s}$$

Note that the propagation delay of the 'ALS74 is not relevant to the MTBF calculation. It does, however, affect the delay of SYNCIN relative to other signals in the synchronous system that are clocked directly by CLOCK.

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- 3e8.22 8.21 For TTL, refer to the sample data sheet on page 168 of the text: "Not more than one output should be shorted at a time; duration of short-circuit should not exceed one second." In the switch debounce circuit, the short lasts only for a few tens of *nanoseconds*, so it's OK. High-current-drive CMOS families, such as AC and ACT, recommend against even momentary shorting of the outputs.

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- 3e8.23 8.22 CMOS outputs can “latch up” under certain conditions. According to the Motorola *High-Speed CMOS Logic Data* book (1988 edition, pp. 4–10), a 74HCT output can latch up if a voltage outside the range  $-0.5 \leq V_{out} \leq V_{CC} + 0.5V$  is forced on the output by an external source. In a switch debounce circuit using 74HCT04s, the switch connection to ground is an external source, but the voltage (0 V) is within the acceptable range and should not be a problem.

Another potential problem is excessive short-circuit current, but again the data book indicates that shorting the output briefly is not a problem, as long as “the maximum package power dissipation is not violated” (i.e., the short is not maintained for a long time).

Similar considerations apply to 74AC and 74ACT devices, but in the balance, such devices are *not* recommended in the switch-debounce application, as we’ll explain. On one hand, typical 74AC/74ACT devices are even less susceptible to latch-up than 74HCT devices. (For example, see the Motorola *FACT Data* book, 1988 edition, pp. 2–9.) On the other hand, 74AC/74ACT’s high performance may create noise problems for *other* devices in a system. In particular, when the 74AC/74ACT HIGH output is shorted to ground, it may momentarily drag the local 5 V power-supply rail down with it, especially if the decoupling capacitors are small, far away, or missing. This will in turn cause incorrect operation of the other, nearby logic devices.

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- 3e8.24 8.23 There's no timing-independent way to distinguish a bounce from a true release. Therefore, the time dimension must somehow be incorporated—the circuit must measure the duration of the release, and assume at some point that it's a true release and not a bounce. Microcomputer-controlled keyboards typically use software to measure this duration, which is typically in the range of several to tens of milliseconds.

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- 3e8.25 8.24 TTL inputs require significant current, especially in the LOW state. The bus holder cannot supply enough current unless the series resistor is made much smaller, which then creates a significant load on the bus.

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- 3e8.26 8.25 Please see the VHDL program `latch_decode.vhd` in the accompanying `.zip` file. This program was kindly written and contributed by Xilinx application engineering, but it has not been further checked for correctness and coding style.

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- G8.229 8.26 The trick to building a down counter is simply to use the Q instead of the QN (inverted) output of each stage to clock the next stage, so a rising edge is obtained on a 0-to-1 transition of Q. Alternatively, build the counter the same way as an up counter, but look at the QN outputs instead of the Q outputs.

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- 3e8.29 8.27 The trick to building a down counter is simply to use the Q instead of the QN (inverted) output of each stage to clock the next stage, so a rising edge is obtained on a 0-to-1 transition of Q. Alternatively, build the counter the same way as an up counter, but look at the QN outputs instead of the Q outputs.

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- 3e8.30 8.29 The speed is limited only by the maximum toggling frequency of the LSB flip-flop, assuming the higher-order flip-flops are almost as fast, because they toggle much less frequently. Of course, you may never be able to take a snapshot of the theoretical count in this kind of a design.

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- 3e8.31 8.30 The maximum clock-to-output delay for a 74HCT74 is 44 ns, and the setup time is 15 ns. Therefore, the minimum clock period for toggling is 59 ns, and the maximum frequency is about 17 MHz. For the 74AHCT74, the corresponding numbers are 10 ns, 5 ns, 15 ns, and 66.6 MHz, and for the 74LS74 they are 40 ns, 20 ns, 60 ns, and 16.6 MHz.

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3e8.32 8.31

$$t_{\text{period(min)}} = t_{\text{pTQ}} + 3t_{\text{AND}} + t_{\text{setup}}$$
$$f_{\text{max}} = 1/t_{\text{period(min)}}$$

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3e8.33 8.32

$$t_{\text{period(min)}} = t_{\text{pTQ}} + t_{\text{AND}} + t_{\text{setup}}$$
$$f_{\text{max}} = 1/t_{\text{period(min)}}$$

The synchronous parallel binary counter can run faster because the enable information propagates through the AND gates in parallel.

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3e8.34 8.33

$$t_{\text{period(min)}} = t_{\text{pTQ}} + (n - 1) \cdot t_{\text{AND}} + t_{\text{setup}}$$
$$f_{\text{max}} = 1/t_{\text{period(min)}}$$

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3e8.35 8.34

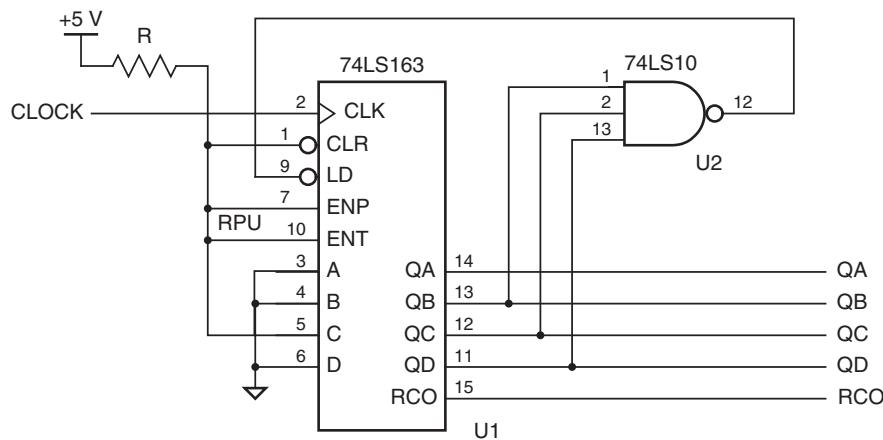
$$t_{\text{period(min)}} = t_{\text{pTQ}} + t_{\text{AND}} + t_{\text{setup}}$$
$$f_{\text{max}} = 1/t_{\text{period(min)}}$$

The maximum frequency is independent of  $n$ . However, the formula is not valid when  $n+1$  exceeds the number of inputs available on a single AND gate. In such a case, two or more levels of gates must be cascaded. Still, assuming the availability of gates with a reasonable number of inputs (say, 4), the maximum frequency of a large synchronous parallel counter is substantially better than that of a like-sized synchronous serial counter.

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G8.236 8.35



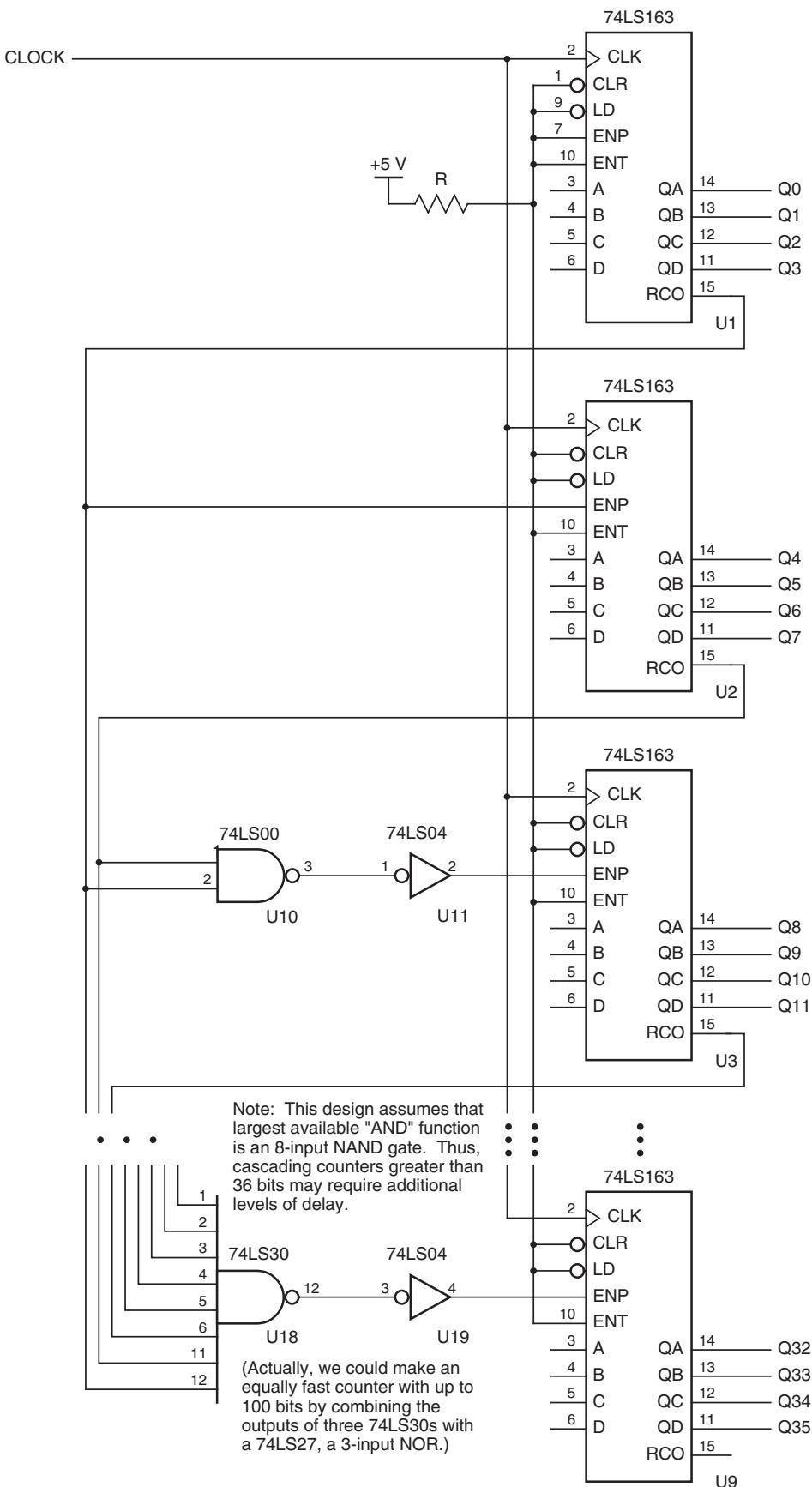
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3e8.37 8.36

Inputs				Current state				Next state			
CLR_L	LD_L	ENT	ENP	QD	QC	QB	QA	QD*	QC*	QB*	QA*
0	x	x	x	x	x	x	x	0	0	0	0
1	0	x	x	x	x	x	x	D	C	B	A
1	1	0	x	x	x	x	x	QD	QC	QB	QA
1	1	x	0	x	x	x	x	QD	QC	QB	QA
1	1	1	1	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	1	0	0	1	0
1	1	1	1	0	0	1	0	0	0	1	1
1	1	1	1	0	0	1	1	0	1	0	0
1	1	1	1	0	1	0	0	0	1	0	1
1	1	1	1	0	1	0	1	0	1	1	0
1	1	1	1	0	1	1	0	0	1	1	1
1	1	1	1	0	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0	1	0	0	1
1	1	1	1	1	0	0	1	0	0	0	0
1	1	1	1	1	1	0	0	0	1	0	0
1	1	1	1	1	1	1	0	1	1	0	1
1	1	1	1	1	1	0	1	0	1	0	0
1	1	1	1	1	1	1	0	0	1	0	0
1	1	1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0

3e8.38 8.37



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The minimum clock period is the sum of:

- (a) The delay from the clock edge to any RCO output (35 ns).
- (b) The delay from any RCO output to any ENP input, that is, two gate delays ( $2 \cdot 15 = 30$  ns ).
- (c) The setup time to the next clock edge required by the ENP inputs (20 ns).

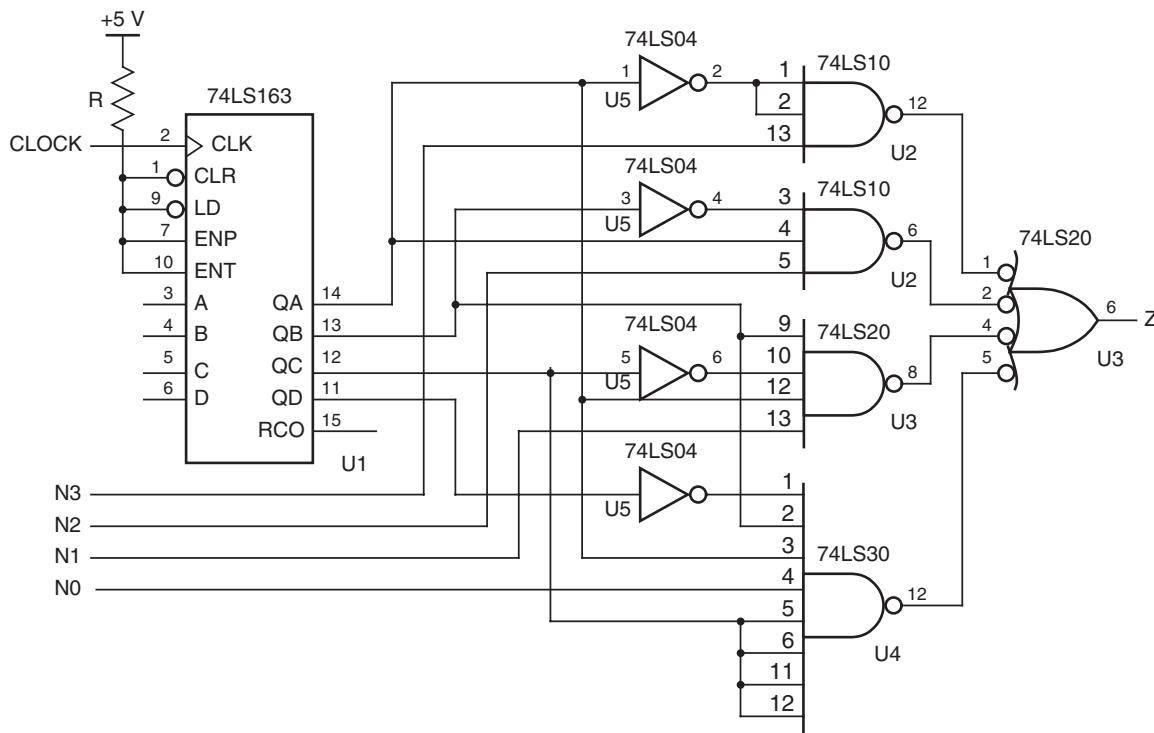
Thus, the minimum clock period is 85 ns, and the corresponding maximum clock frequency is 11.76 MHz.

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- G8.239 8.38 Hook up the two '163s as a free-running counter, as in Figure Cntr-5 at [DDPPonline](#), and connect the Q7 signal to the LOAD\_L input signal. Connect D0 through D6 to GND, and connect D7 high. The resulting counting sequence is 0, 128, 129, 130, ..., 254, 255, 0, 128, 129, 130, ....

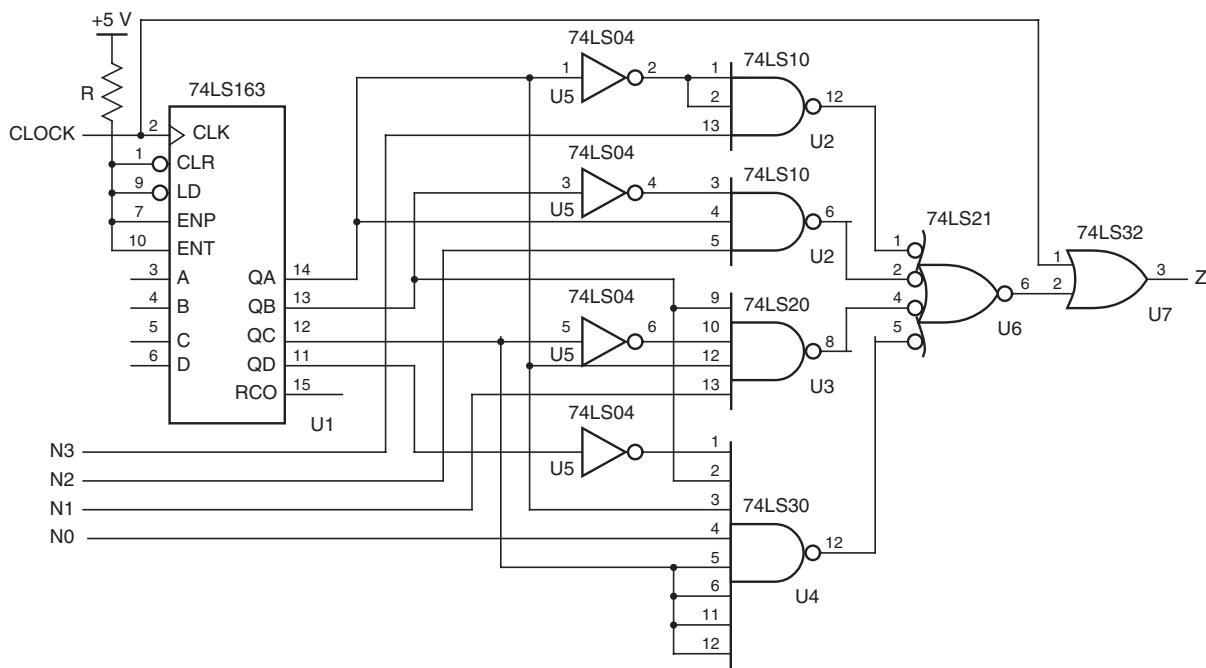
- 3e8.41 8.42 To get even spacing, the strategy is for the MSB (N3) to select half the states, the ones where QA is 0. The next bit down (N2) selects one-fourth of the states, the ones where QB is 0 and the less significant counter bits (i.e., QA) are all 1. Likewise, N1 selects the one-eighth of the states where QC is 0 and QB and QA are 1, and N0 selects the state where QD is 0 and QC, QB, and QA are all 1. In this way, each non-1111 counter state is assigned to one input bit.



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3e8.42 8.43



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- 3e8.44 8.45 Please see the VHDL program `bin_rate_multiplier.vhd` in the accompanying `.zip` file. This program was kindly written and contributed by Xilinx application engineering, but it has not been further checked for correctness and coding style. A corresponding Verilog program has not been written yet.

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- 3e8.46 8.46 The key in solving this problem is to notice that the 169's RCO\_L output can be used to detect the states from which "nonstandard" transitions should be made, 0 to 8 while counting down and 15 to 7 while counting up. Furthermore the most significant bit of the count indicates whether we are counting up or down. Therefore, RCO\_L is connected to LD\_L, and QD is connected to UP/DN. To obtain the proper next states at the non-standard transitions, inputs A-C are connected to QA-QC, respectively, while D is connected to QD through an inverter.

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- 3e8.50 8.48 Please see the VHDL program counter.vhd in the accompanying .zip file. This program was kindly written and contributed by Xilinx application engineering, but it has not been further checked for correctness and coding style. A corresponding Verilog program has not been written yet.

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- 3e8.53 8.53 Please see the VHDL program v74x163s.vhd in the accompanying .zip file. This program was kindly written and contributed by Chris Dunlap of Xilinx application engineering, but it has not been further checked for correctness and coding style.

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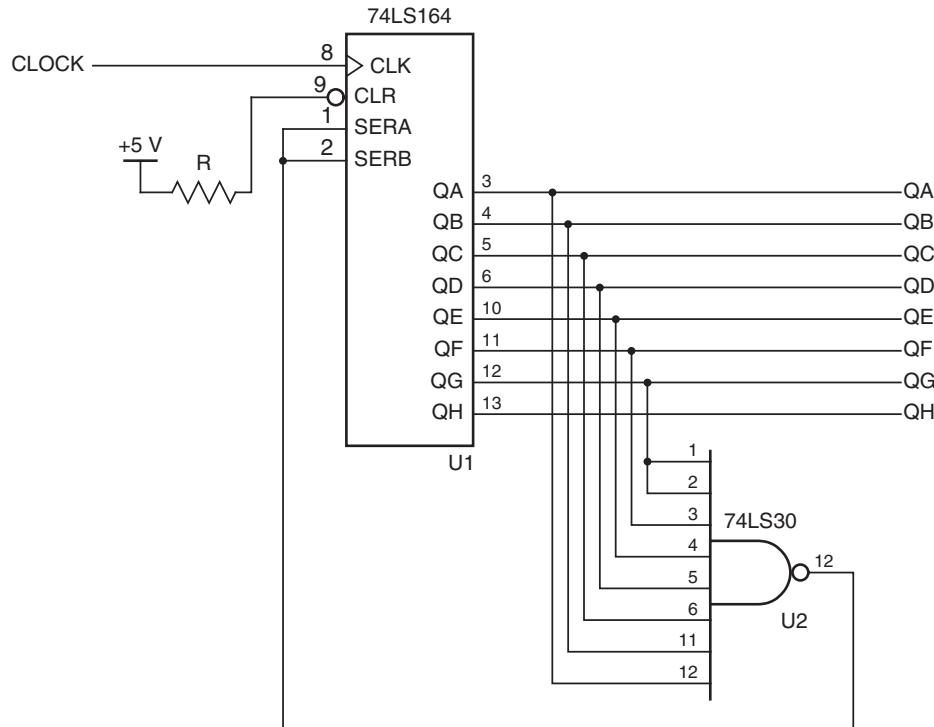
For exclusive use of adopters of the book *Digital Design Principles and Practices*, Fourth Edition, by John F. Wakerly,  
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- 3e8.58 8.54 Arithmetic operations such as addition, subtraction, and comparison are basic to the operation of a computer. A serial comparator can be designed either way, looking at the LSBs or the MSBs first. However, adders and subtractors must propagate carries and borrows from the LSB to the MSB; therefore, a serial adder must process the LSBs first. So we would design the serial computer to transmit and process the LSB first.

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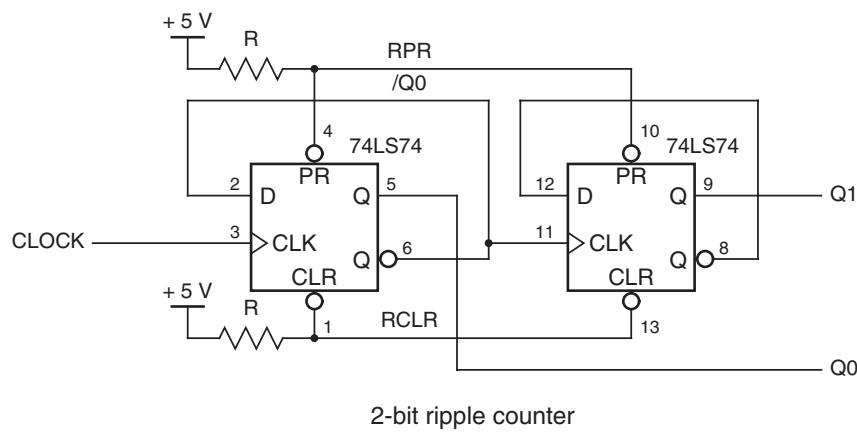
- 3e8.59 8.55 Please see the figure below. A corresponding the VHDL program *counter8.vhd* appears in the accompanying .zip file. This program was kindly written and contributed by Vikram Pasham of Xilinx application engineering, but it has not been further checked for correctness and coding style.



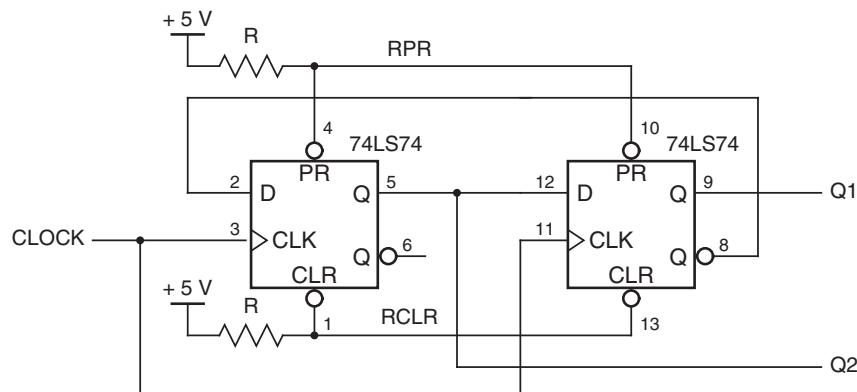
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3e8.60 8.57

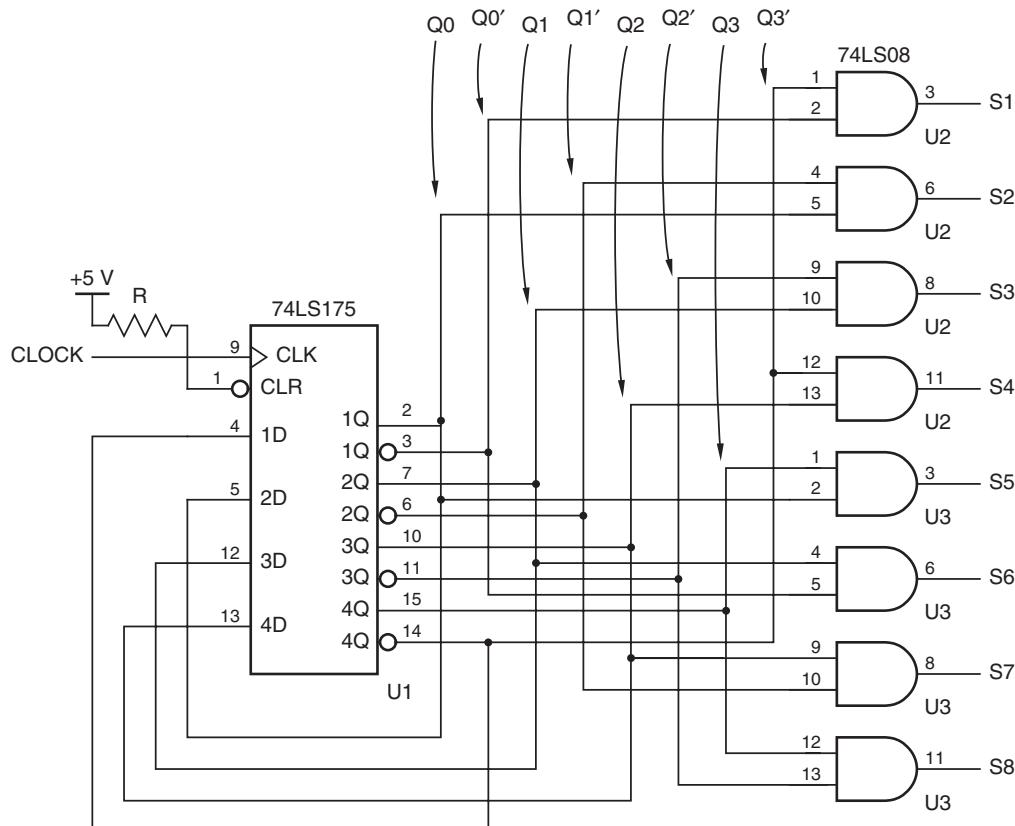


2-bit ripple counter



2-bit Johnson counter

- 3e8.61 8.58 Please see the figure below. A corresponding the VHDL program *Johnson.vhd* appears in the accompanying .zip file. This program was kindly written and contributed by Vikram Pasham of Xilinx application engineering, but it has not been further checked for correctness and coding style.



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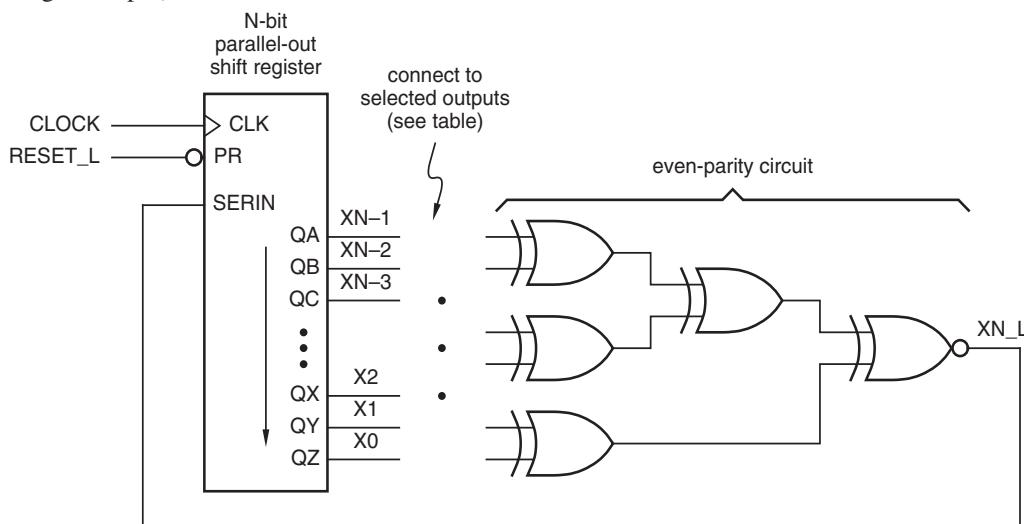
- 3e8.62 8.60 Regardless of the number of shift-register outputs connected to the odd-parity circuit, its output in state 00...00 is 0, and the 00...00 state persists forever. However, suppose that an odd number of shift-register outputs are connected. Then the output of the odd-parity circuit in state 11...11 is 1, and the 11...11 state also persists forever. In this case, the number of states in the “maximum-length” sequence can be no more than  $2^n - 2$ , since two of the states persist forever. Therefore, if an LFSR counter generates a sequence of length  $2^n - 1$ , it must have an even number of shift-register outputs connected to the odd-parity circuit.

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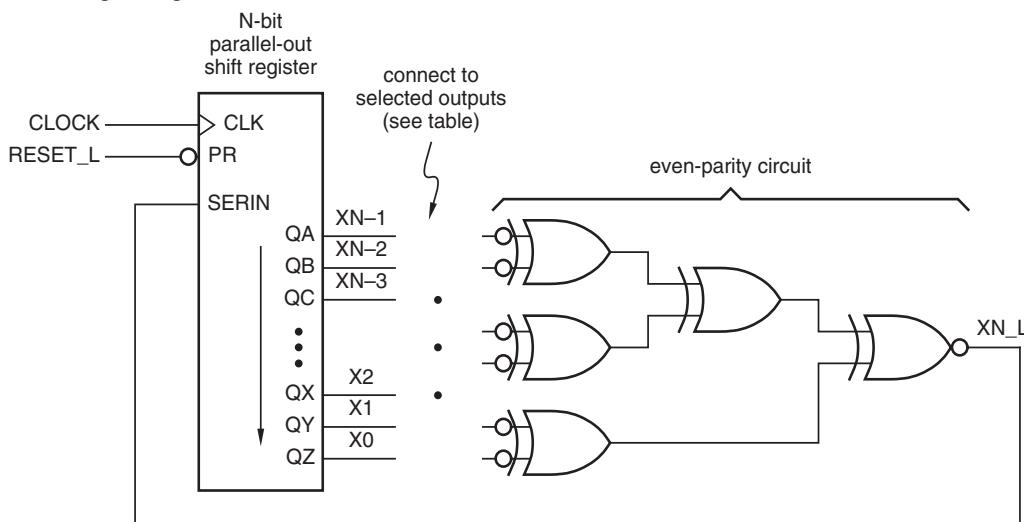
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- 3e8.63 8.61 If  $X_0$  is not included, then every pair of states  $xx\dots xx0$  and  $xx\dots xx1$  have the same next state, and the state diagram cannot contain a maximum-length cycle with  $2^n - 1$  states.

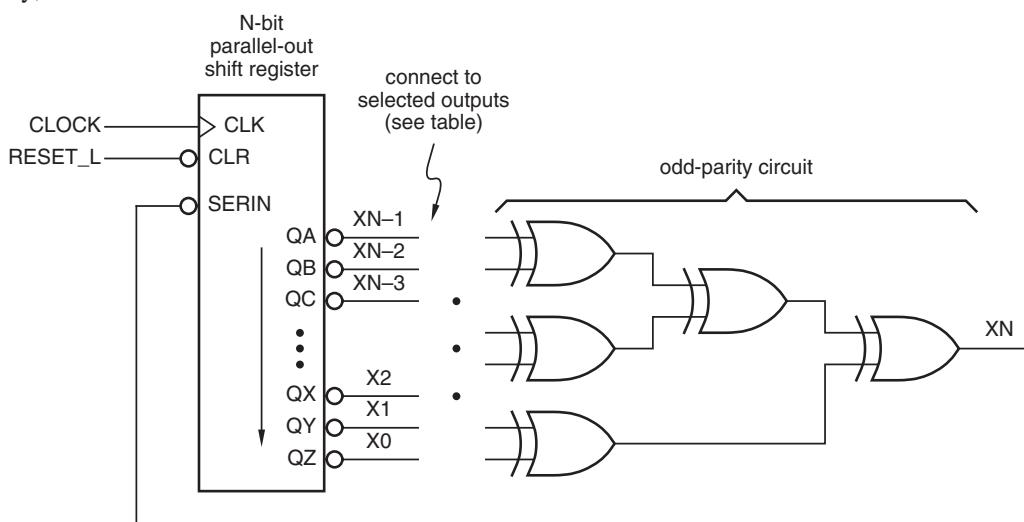
- 3e8.64 8.62 The figure below shows the effect of physically changing the odd-parity circuit to an even-parity circuit (i.e., inverting its output).



From Exercise 8.60, we know that an even number of shift-register outputs are connected to the parity circuit, and we also know that complementing two inputs of an XOR gate does not change its output. Therefore, we can redraw the logic diagram as shown below.



Finally, we can move the inversion bubbles as shown below.



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This circuit has exactly the same structure as Figure 8–51, except that the shift register stores complemented data. When we look at the external pins of the shift register in the first figure in this solution, we are looking at that complemented data. Therefore, each state in the counting sequence of the even-parity version (our first figure) is the complement of the corresponding state in the odd-parity version (Figure 8–51). The odd-parity version visits all states except 00...00, so the even-parity version visits all states except 11...11.

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- G8.265 8.63 According to Exercise 8.60, we know that there must be an even number of shift-register outputs connected to the odd-parity circuit, and based on Exercise 8.61 we know that  $X_0$  must be one of them. Therefore, only four possible feedback equations give maximum-length sequences:  $X_4 = X_3 \oplus X_2 \oplus X_1 \oplus X_0$  ,  $X_4 = X_3 \oplus X_0$  ,  $X_4 = X_2 \oplus X_0$  and  $X_4 = X_1 \oplus X_0$  (the one given in Table 8–26).

Starting with state 001, the counting sequence obtained with the first equation is 001, 100, 110, 111, 011, 101, 010, 001, .... The counting sequence obtained with the second equation is 001, 100, 010, 101, 110, 111, 011, 001, .... Both are maximum-length sequences.

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- 3e8.66 8.64 According to Exercise 8.61,  $X_0$  must appear in the feedback equation for any LFSR that generates a maximum length sequence. Therefore, the states produced at the “end” of the sequence are 00...01, 10...00.

For all the possible states of the shift register, the NOR gate produces a 1 output only in states 00...01 and 00...00, and through the extra XOR gate causes the new MSB to be the opposite of what would normally be loaded. Thus, the modified circuit inserts state 00...00 into the sequence as follows: 00...01, 00...00, 10...00.

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- 3e8.67 8.65 This problem can be analyzed in a manner similar to Exercise 8.62. That is, we can propagate the bubble on the NAND-gate output through the XOR gate and to the shift register input, and create bubbles on the shift register outputs, to show that the new circuit generates the complement of the original circuit's state sequence.

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- 3e8.68 8.69 The order of bit transmission does not matter for parity checking. A VHDL program `Parity_Check.vhd` is contained in the accompanying `.zip` file. This program was kindly written and contributed by Johnny West of Xilinx application engineering, but it has not been further checked for correctness and coding style. The second part of the program (instantiating the individual modules) clearly can be done more concisely using a generate statement.

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- 3e8.71 8.71 The S0 output requires 8 product terms. The remaining outputs each require 3 product terms. The design fits in a PAL16R8.

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- 3e8.72 8.72 The program in Table 8–32 does not specify the next-state behavior for any of the “unused” states. This will normally default to state “00...00” with most ABEL compilers. That state is itself unspecified, so if the machine ever gets into an unused state, it will end up in state “00...00” as a “trap” state. The program in Table 8–31 doesn’t do so well in illegal states either, but it behaves differently. Since it hasn’t been designed with “self-synchronizing” ring-counter behavior, any illegal state just shifts forever, like the illegal states in Figure 8–44.

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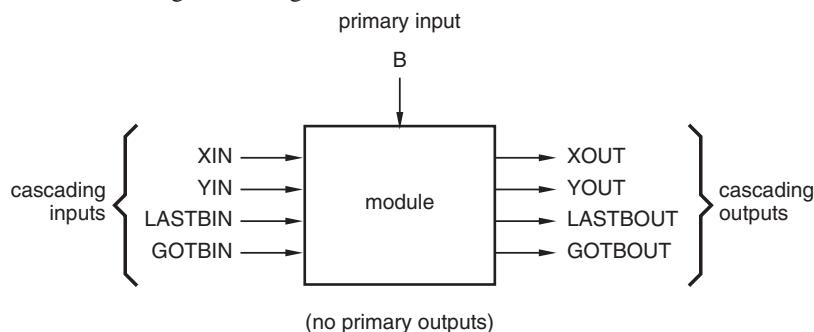
- 3e8.75 8.76 Please see the ABEL program TIMEGEN6.abl in the accompanying .zip file. In this design, RESET is not recognized until the end of phase 6. RESTART is still recognized at the end of any phase; otherwise it would have no real use (i.e., only going back to phase 1 after the end of phase 6, which happens anyway.) Presumably, RESTART would be used only with great care or in unusual circumstances (e.g., during debugging).

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- 3e8.79 8.80 A VHDL program Vtmeagn6.vhd appears in the accompanying .zip file. This program was kindly written and contributed by Johnny West of Xilinx application engineering, but it has not been further checked for correctness and coding style. Also, a test bench and a Verilog version have not been written yet.

- 3e8.80 8.81 An iterative circuit that performs the specified function requires a total of four cascading signals between modules, as shown in the following block diagram:



The following equations define the outputs of each module:

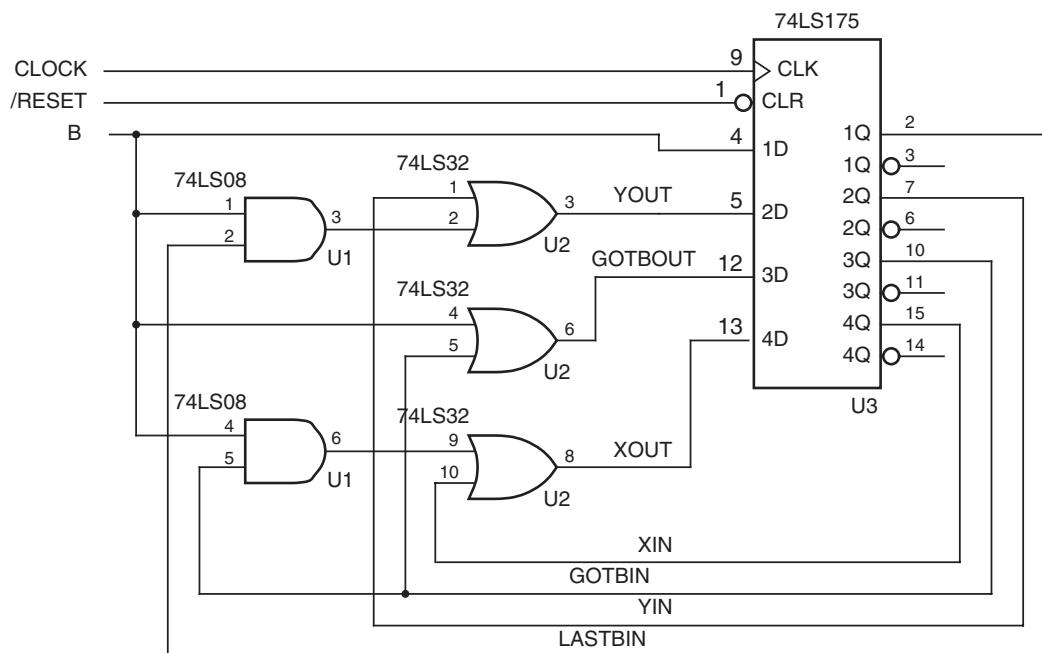
$$\text{LASTBOUT} = B$$

$$\text{GOTBOUT} = \text{GOTBIN} + B$$

$$\text{XOUT} = \text{XIN} + \text{GOTBIN} \cdot B$$

$$\text{YOUT} = \text{YIN} + \text{LASTBIN} \cdot B$$

A sequential-circuit version of the iterative circuit, that looks at B inputs serially, one tick at a time, is shown below:



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- 3e8.90 8.82 Transitions on SYNCIN occur a maximum of 20 ns after the rising edge of CLOCK. Given a 40-ns clock period and a 10-ns setup-time requirement for the other 'ALS74s, 10 ns is the maximum propagation delay of the combinational logic.

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- G8.291 8.83 The minimum clock period is constrained by the delay from clock to output through FF3, and subsequently from clock to output through FF2; the period must be long enough for the setup time of FF4 to be met. Thus, the minimum clock period is  $9 + 9 + 5 = 23\text{ ns}$ , and the maximum clock frequency is 43.5 MHz.

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- 3e8.92 8.84 In this circuit, FF3 is a divide-by-two counter, and the clock frequency applied to FF1 and FF2 is only half of CLOCK's frequency, or 26.3 MHz. With a 38-ns clock period and a 5-ns setup time requirement on FF2, the available metastability resolution time is 33 ns. Thus, we calculate

$$\text{MTBF}(33\text{ns}) = \frac{\exp(33/0.4)}{0.2 \cdot 10^{-3} \cdot 26.3 \cdot 10^6 \cdot 4 \cdot 10^6} \approx 3.2 \cdot 10^{25}\text{s}$$

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- 3e8.93 8.85 First, we calculate the probability that SYNCIN is ever metastable. Given a 25-ns clock period, we have  $2 \cdot 25 - 5 = 45$  ns available for metastability resolution. Thus, we calculate

$$\text{MTBF}(45\text{ns}) = \frac{\exp(45/0.4)}{0.2 \cdot 10^{-3} \cdot 20 \cdot 10^6 \cdot 4 \cdot 10^6} \approx 4.5 \cdot 10^{38} \text{s}$$

The MTBF is much better already, since the clock period is longer.

In this circuit, FF2 is clocked  $25 - 7 = 18$  ns before the next rising edge of CLOCK. Since FF4 has a setup-time requirement of 5 ns, DSYNCIN may be metastable (and true synchronizer failure occurs) only if SYNCIN is metastable  $18 - 5 = 13$  ns after FF2 is clocked. That is, FF2 is allowed for metastability resolution 6 ns more than its normal maximum propagation delay.

Calculating the probability that FF2's output is metastable after 13 ns is tricky, since the conditions of the problem don't match the standard MTBF formula. That is, the problem we must solve may be formulated as follows:

Suppose we repeat an experiment in which the D input of a 74F74 flip-flop is at a metastable, non-logic voltage (between 0.8 and 2.0 volts) at some time during the setup-time window of the device.

In what fraction of cases will the device output be metastable 13 ns after the clock edge?

Although the empirical and theoretical studies of metastable behavior that I'm familiar with don't discuss this case, we can still get a handle on the situation if we're willing to extrapolate the "standard" test conditions and MTBF formula.

Suppose the period of a 74F74's clock is only 5 ns (the setup time of the device); the clock frequency is 200 MHz. Let us suppose that the asynchronous transition rate is also 200 MHz, which means that an asynchronous transition occurs during *every* clock period. Now suppose that under these conditions we were able to look at the 'F74 output after 13 ns (pretending that subsequent clock edges never occurred); we would calculate

$$\text{MTBF}(13\text{ns}) = \frac{\exp(13/0.4)}{0.2 \cdot 10^{-3} \cdot 200 \cdot 10^6 \cdot 200 \cdot 10^6} \approx 16 \text{s}$$

Since we are "synchronizing" 200,000,000 ( $2 \cdot 10^8$ ) times per second, evidently only one in  $32 \cdot 10^8$  synchronizations under these conditions results in a metastability resolution time of 13 ns or longer. Therefore, our previous MTBF result of  $4.5 \cdot 10^{38}$  may be multiplied by  $32 \cdot 10^8$ , giving a net MTBF of  $1.44 \cdot 10^{48}$ .

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- 3e8.97 8.86 The problem is that the flip-flop may come out of metastability on its own, and begin to settle to the HIGH state, just as METACLR\_L is beginning to clear it to the LOW state. This may drive it back to the metastable state, or cause a sustained oscillation, as shown in the figure below.

