Chapter 2 Bits, Data Types and Operations

2.1 Logic Arithmetic

NOT, AND, OR

Mask: a & 1 = a, a OR 0 = a,

DeMorgan's Law: $\overline{\overline{A} \wedge \overline{B}} = A \vee B$

2.2 Floating Number (Continue)

IEEE 754 Standard

sign - exponent - fraction

Decimal: $(-1)^{sign} * (1.fraction_{(2)})^{exponent-bias}$

16bits

sign: 1 bit

exponent: 5 bits ($[0, 2^6 - 1]$) bias: $2^{6-1} - 1 = 31$

fraction: 10 bits

32bits

sign: 1 bit

exponent: 8 bits ($[0, 2^8 - 1]$) bias: $2^{8-1} - 1 = 127$

fraction: 23 bits

64bits

sign: 1 bit

exponent: 11 bits ($[0, 2^1 1 - 1]$) bias: $2^{11-1} - 1 = 1023$

fraction: 52 bits

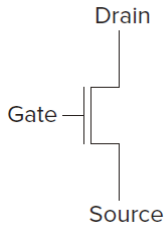
Special Rules:

Meaning	Exponent	Fraction
0	0	0
+INF(sign = 0)	11...1	0
-INF(sign = 1)	11...1	0
NaN(Not a Number)	11...1	Not Zero

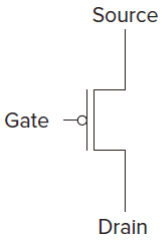
Chapter 3 Digital Logic Structures

3.1 Transistors

N-Type

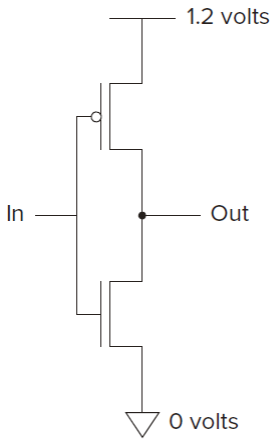


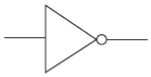
P-Type



3.2 Logic Gates

3.2.1 NOT

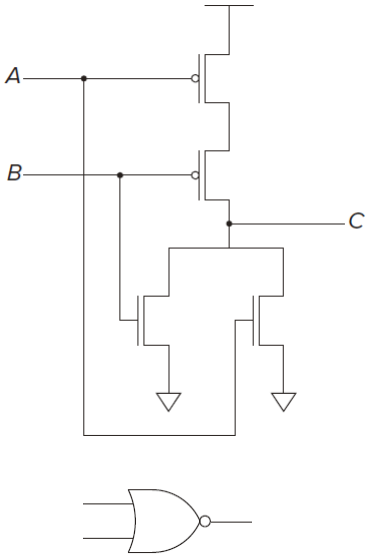




(a) Inverter

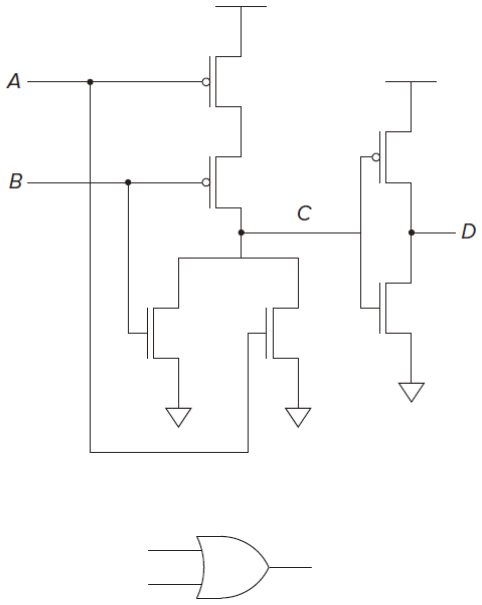
3.2.2 NOR OR

NOR:



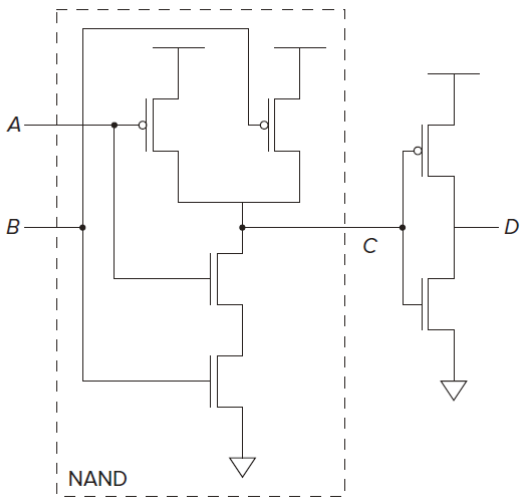
(e) NOR gate

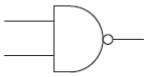
OR:



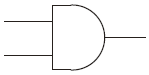
(c) OR gate

3.2.3 NAND AND





(d) NAND gate



(b) AND gate

3.2.4 Recommend Reading

3.2.3 Why We Can't Simply Connect P-Type to Ground

3.2.5 Gates with More Than Two Inputs

3.3 Combinational Logic Circuits

3.3.1 Decoder

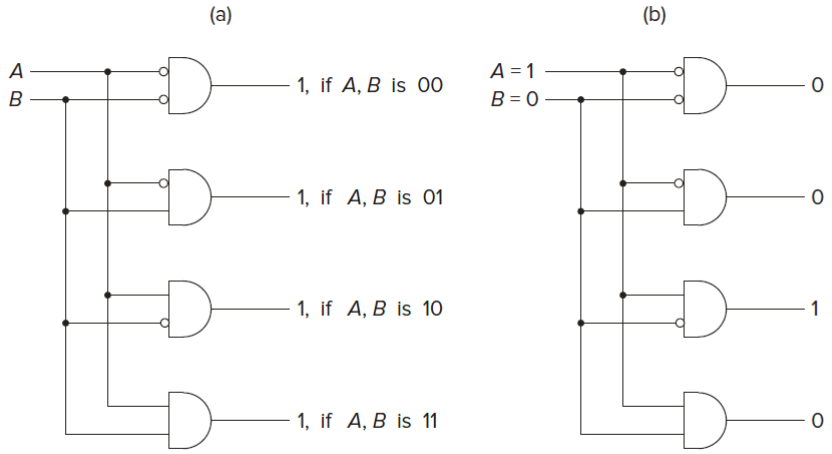


Figure 3.11 A two-input decoder.

3.3.2 Mux

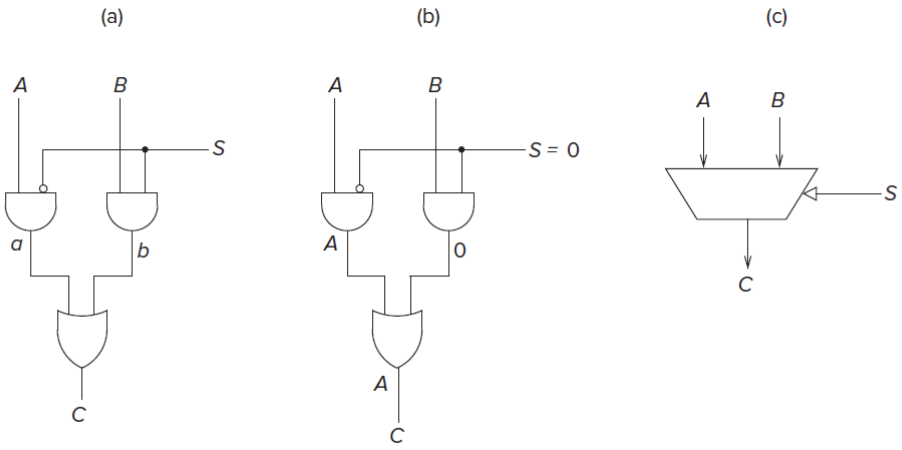


Figure 3.12 A 2-to-1 mux.

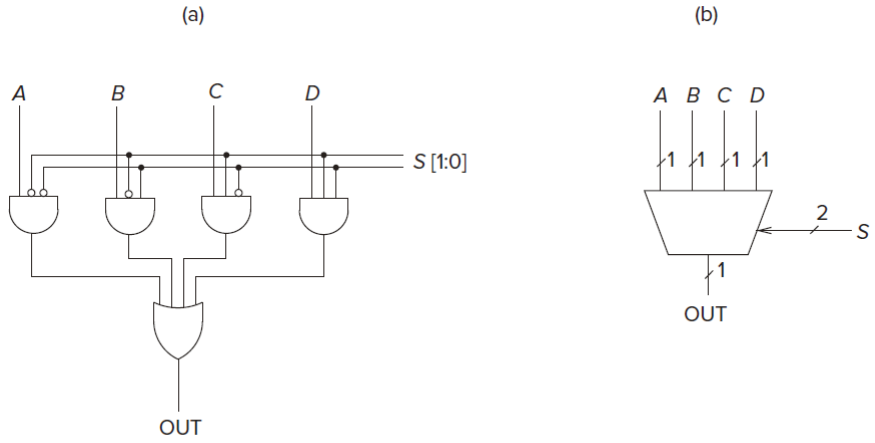


Figure 3.13 A four-input mux.

3.3.3 1-bit Adder

A_i	B_i	C_i	C_{i+1}	S_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

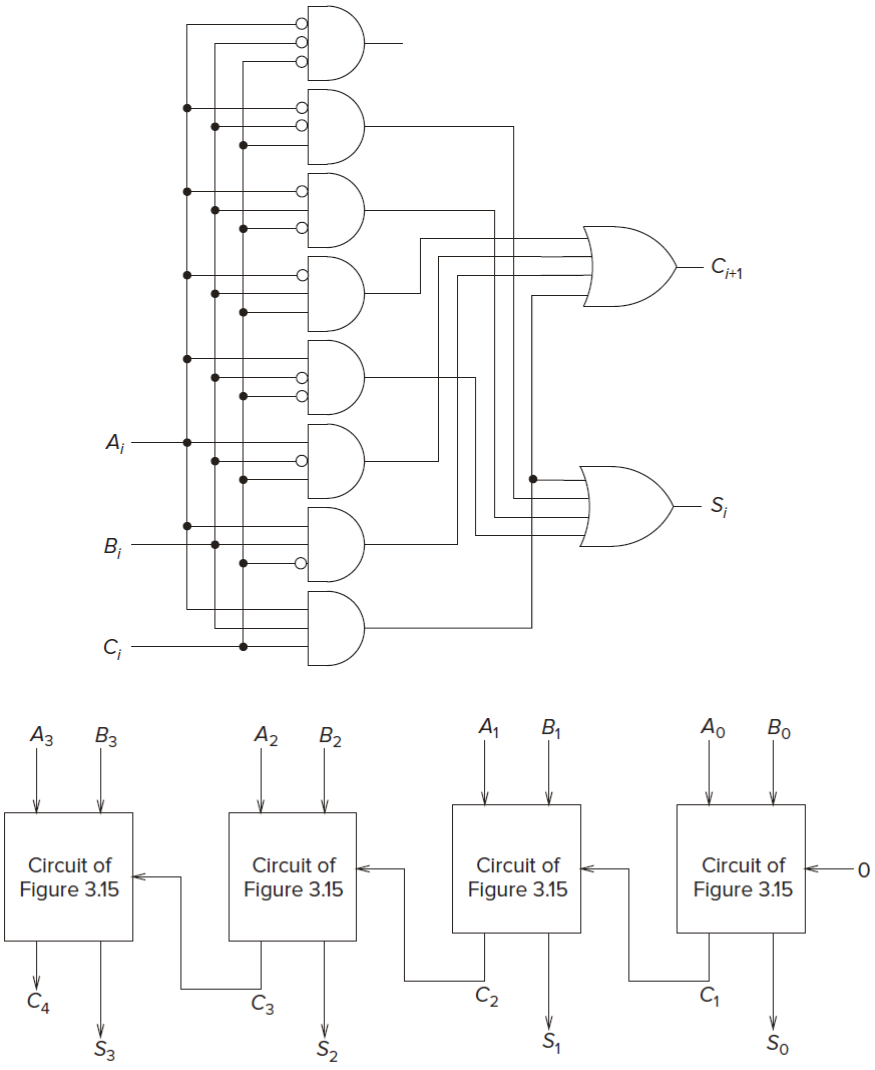


Figure 3.16 A circuit for adding two 4-bit binary numbers.

3.3.4 PLA

Read the book for more details.

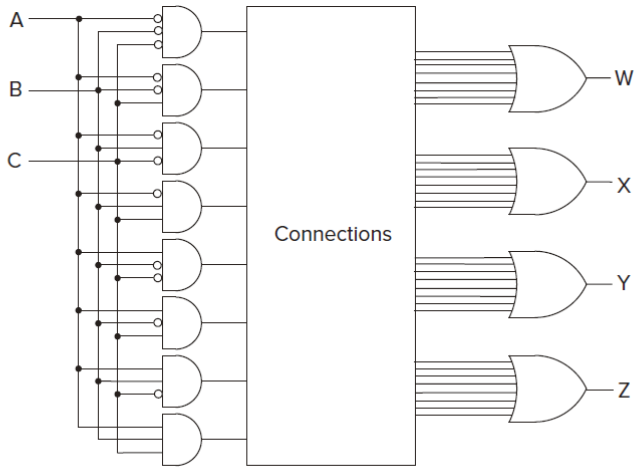


Figure 3.17 A programmable logic array.

3.3.5 Logic Completeness

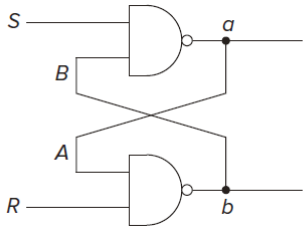
Read the book for more details.

{AND, OR, NOT}

3.4 Basic Storage Elements

3.4.1 The R-S Latch

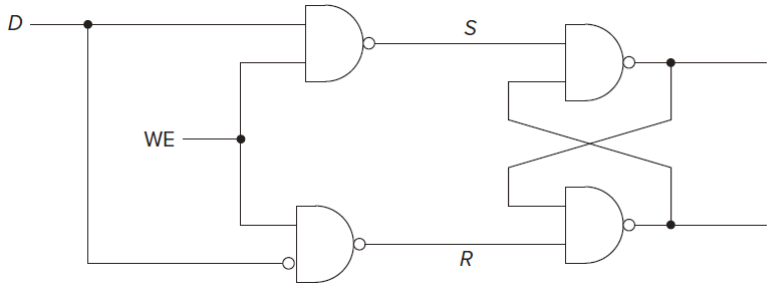
Q for a and $\overline{Q}$ for b



R	S	Q	$\overline{Q}$	Comment
0	0	?	?	Stored state unknown
0	1	1	0	"Set" Q to 1
0	0	1	0	Now Q "remembers" 1
1	0	0	1	"Reset" Q to 0
0	0	0	1	Now Q "remembers" 0
1	1	0	0	Both go low
0	0	?	?	Unstable!

3.4.2 The Gated D Latch

Q for a and $\overline{Q}$ for b



C	D	Q	Comment
0	X	No change	No change
1	0	0	Clear Q
1	1	1	Set Q

3.5 The Concept of Memory

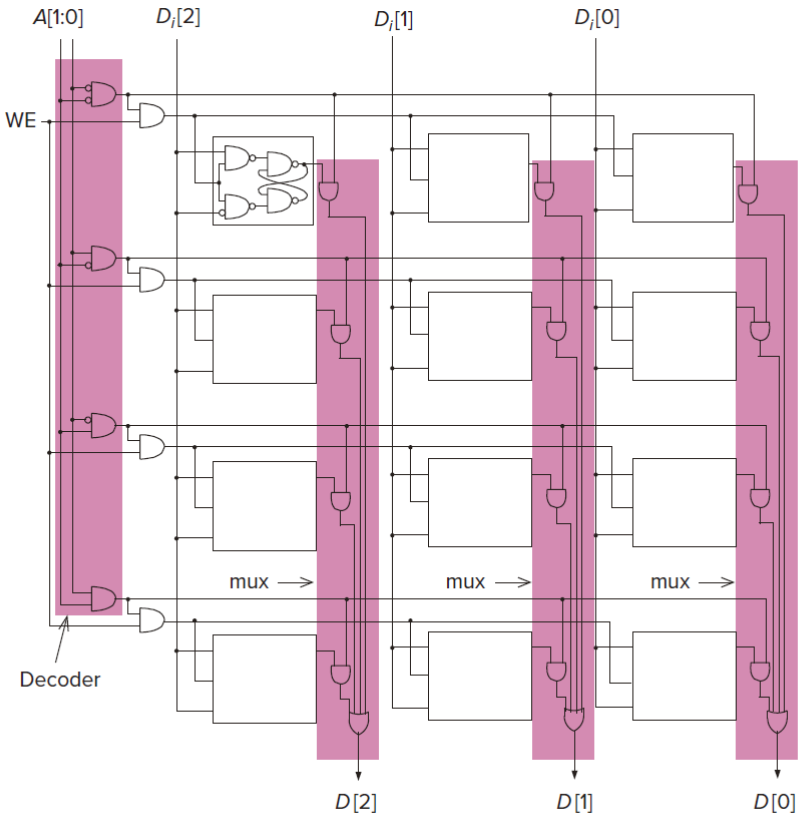


Figure 3.20 A 2^2-by-3-bit memory.

3.5.1 Address Space

We refer to the unique identifier associated with each memory location as its **address.**

We refer to the total number of uniquely identifiable locations as the memory's **address space.**

3.5.2 Addressability

We refer to the number of bits of information stored in each location as its **addressability**.

For A $2^n - by - m - bit$ Memory, its Address Space is 2^n and its Addressability is m.

3.6 Sequential Logic Circuits

3.6.1 The Concept of State

The state of a system is a snapshot of all the relevant elements of the system at the moment the snapshot is taken.

3.6.2 Finite State Machine

A finite state machine consists of five elements:

1. a finite number of states
2. a finite number of external inputs
3. a finite number of external outputs
4. an explicit specification of all state transitions
5. an explicit specification of what determines each external output value.

State Diagram:

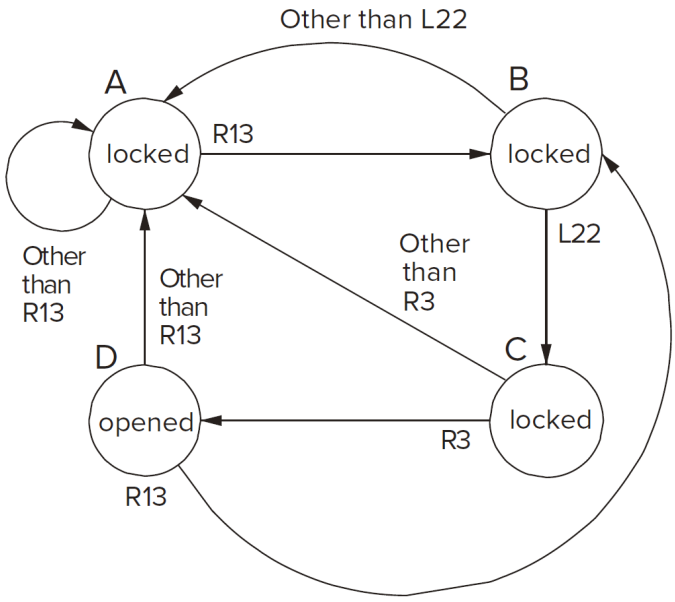


Figure 3.26 State diagram of the combination lock of Figure 3.23a.