**Freescale Semiconductor**

Product Brief

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# MPC560xB/C Microcontroller Family Product Brief

The 32-bit MPC560xB/C automotive microcontrollers are a family of System-on-Chip (SoC) devices designed to be central to the development of the next wave of central vehicle body controller, smart junction box, front module, peripheral body, door control and seat control applications.

Jointly developed by Freescale Semiconductor and ST Microelectronics™, the MPC560xB/C family is one of a series of next-generation automotive microcontrollers based on the Power Architecture™ Book E architecture and designed specifically for embedded applications.

This document describes the features of the MPC560xB/C family and highlights important electrical and physical characteristics of the devices.

**Contents**

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# 1 Introduction

The MPC560xB/C microcontrollers operate at speeds up to 64 MHz and offer high performance processing with low power consumption. They are compatible with the existing development infrastructure of current Power Architecture™ devices and are supported with software drivers, operating systems and configuration code to assist with application development. Refer to Section 5, "Developer Support" for more information.

The MPC560xB/C family is compatible with Freescale's MPC5500 family. It includes all features of the MPC5500 family plus many new features coupled with high performance 90 nm CMOS technology to provide substantial reduction of cost per feature and significant performance improvement.

On-chip modules include:

- Single issue, 32-bit Power Architecture™ e200z0 CPU core complex
  - Includes Freescale Variable Length Encoding (VLE) enhancements for code size reduction
- On-chip ECC flash memory with flash controller
  - Up to 512 KB program flash—single module with prefetch buffer and 128-bit data access port
  - 64 KB data flash—single module with prefetch buffer and 128-bit data access port
- Up to 32 KB on-chip ECC RAM with RAM controller
  - Up to 24 KB primary RAM and 8 KB backup
  - Can be accessed by byte, 16-bit halfword or 32-bit word
- Memory Protection Unit (MPU) provides basic memory access permission and ensures separation between different codes and data
- Boot assist module (BAM) with 8 KB dedicated ROM for embedded boot code
- Frequency modulated phase locked loop (FMPLL)
- Interrupt controller (INTC) with 149 peripheral interrupt sources, including 16 external interrupts
- 10-bit analog-to-digital converter (ADC) with a minimum conversion time of 2 µs
  - 16 internal channels
  - 20 extended channels, 4 being expandable to up to 32 external channels
- Two 28-channel enhanced modular Input Output System (eMIOS) provide ability to generate or measure time events
  - 16-bit counter width
  - Configurable—can implement:
    - Up to 56 IC/OC channels
    - Up to 48 pulse width modulation (PWM) channels
    - Up to 8 modulus counter
- Four Local Interconnect Network (LIN) controller modules capable of autonomous message handling (master), autonomous header handling (slave mode), and UART support. Compliant with LIN protocol rev 2.1
- Three DSPI (Deserial Serial Peripheral Interface) modules for full-duplex, synchronous, communications with external devices

- Inter-integrated circuit ($I^2C$) module with master/slave bus Interface.
- Six Controller Area Network (FlexCAN) modules compliant with the CAN protocol version 2.0 C. The bit rate can be programmed up to 1 Mb/s.
- System Timers:
  — Four Software Timer Module (STM) timers
  — Six Peripheral Interrupt Timer (PIT) timers (including ADC trigger)
  — One Real Time Counter (RTC) timer
- Cross Trigger Unit Lite (CTUL)—a collection of 9-bit down counters with an exponential prescaler able to generate a trigger event for an ADC conversion.
- Crossbar switch architecture for concurrent access to peripherals, flash, or RAM from multiple bus masters
- System Integration Unit Lite (SIUL) manages resets, external interrupts, GPIO and pad control.
- The System Status and Configuration Module (SSCM) provides information for identification of the device, last boot mode, or debug status. It also provides an entry point for censorship password mechanism.
- Clock Generation Module (CGM) generates system clock sources and provides a unified register interface, enabling access to all clock sources.
- Clock Monitor Unit (CMU) monitors the integrity of the main crystal oscillator and the PLL and acts as a frequency meter, measuring the frequency of one clock source vs. a reference clock.
- Mode Entry Module (MEM) controls the System-on-Chip (SoC) mode, i.e., RUN, HALT, STOP, or STANDBY, and mode transition sequences. Also manages power control, voltage regulator, clock generation and clock management modules.
- Power Control Unit (PCU) implements standby mode entry/exit and controls connections to power domains.
- Reset Generation Module (RGM) manages reset assertion and release to the device at initial power-up.
- On-chip voltage regulator controller for regulating 5 V down to 1.2 V for core logic
- JTAG (IEEE 1149.1)/Nexus port: for application development. Optional Nexus 2+ trace port.

# 2    Block Diagram

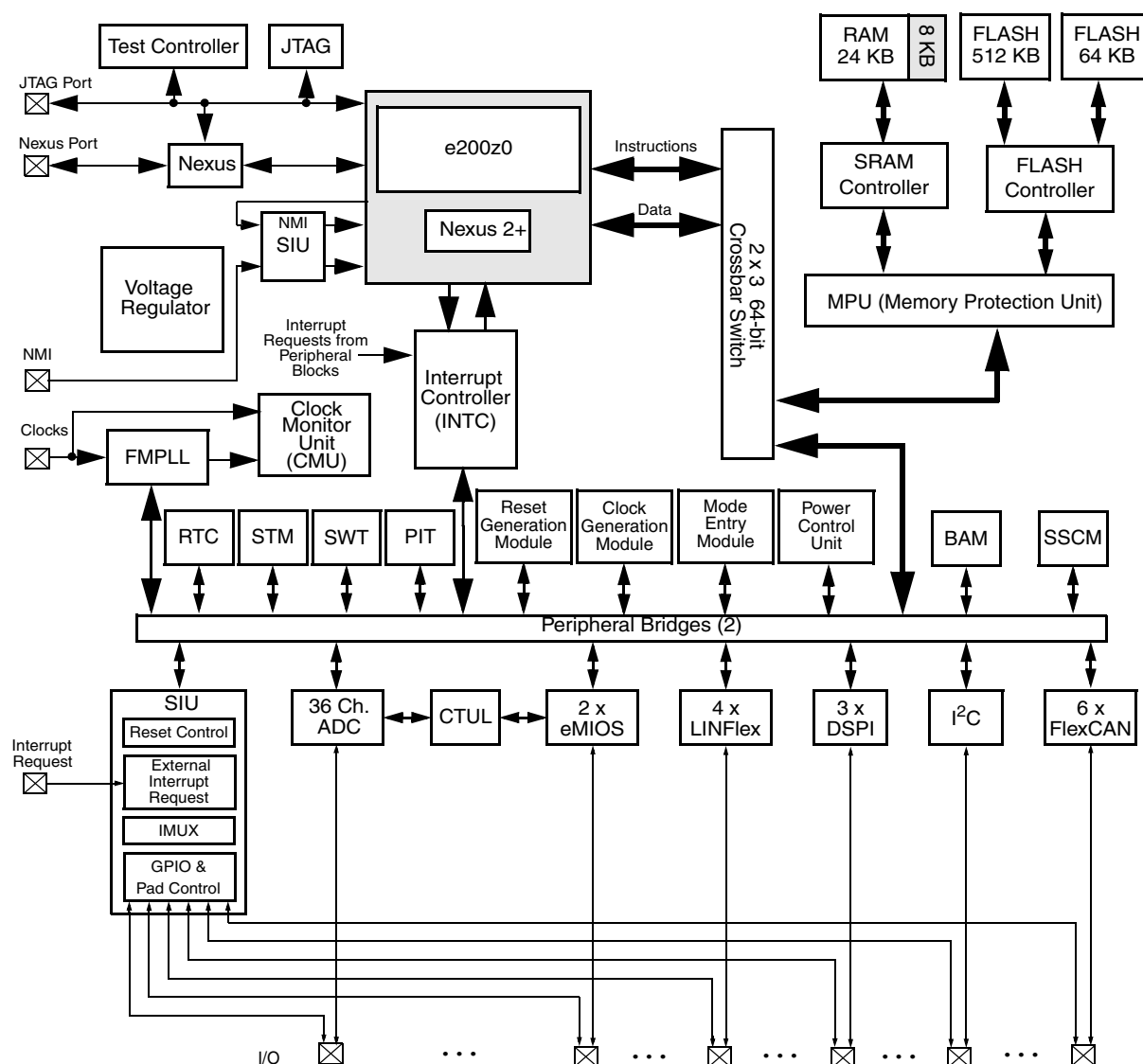Figure 1 shows a top-level block diagram of the MPC560xB/C.

**Figure 1. MPC560xB/C Block Diagram**

# 3   Overview of the MPC560xB/C Family

The following sections provide high-level descriptions of the features found on the MPC560xB/C family of devices.

## 3.1  Device Summary

**Table 1. MPC560xB/C Device Comparison[1]**

| Feature | MPC5602B | | MPC5602C | MPC5603B | | MPC5603C | MPC5604B | | | MPC5604C |
|---|---|---|---|---|---|---|---|---|---|---|
| **CPU** | e200z0 | | | | | | | | | |
| **Execution Speed[2]** | Static - 64 MHz | | | | | | | | | |
| **Flash** | 256 KB | 256 KB | 256 KB | 384 KB | 384 KB | 384 KB | 512 KB | 512 KB | 512 KB | 512 KB |
| **Data Flash Block** | 4×16 KB | | | | | | | | | |
| **RAM** | 24 KB | 24 KB | 32 KB | 28 KB | 28 KB | 32 KB | 32 KB | 32 KB | 32 KB | 32 KB |
| **MPU** | 8 entry | | | | | | | | | |
| eDMA | No | | | | | | | | | |
| ADC | 28 ch, 10-bit | 36 ch, 10-bit | 28 ch, 10-bit | 28 ch, 10-bit | 36 ch, 10-bit | 28 ch, 10-bit | 28 ch, 10-bit | 36 ch, 10-bit | 36 ch, 10-bit | 28 ch, 10-bit |
| CTU | Yes | | | | | | | | | |
| **Total Timer I/O[3] eMIOS200** | 28 ch, 16-bit | 56 ch, 16-bit | 28 ch, 16-bit | 28 ch, 16-bit | 56ch, 16-bit | 28 ch, 16-bit | 28 ch, 16-bit | 56 ch, 16-bit | 56 ch, 16-bit | 28 ch, 16-bit |
| PWM + MC + IC/OC[4] | 4 ch | 5 ch | 5 ch | 4 ch | 10 ch | 5 ch | 5 ch | 10 ch | 10 ch | 5 ch |
| PWM + IC/OC[4] | 20 ch | 20 ch | 20 ch | 20 ch | 40 ch | 20 ch | 20 ch | 40 ch | 40 ch | 20 ch |
| IC/OC[4] | 0 ch | 3 ch | 3 ch | 0 ch | 3 ch | 3 ch | 3 ch | 6 ch | 6 ch | 3 ch |
| **SCI (LINFlex)** | 3 | 3 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| **SPI (DSPI)** | 3 | | | | | | | | | |
| **CAN (FlexCAN)** | 2 | 2 | 6 | 3 | 3 | 6 | 3 | 3 | 6 | 6 |
| **FlexRay** | No | | | | | | | | | |
| Ethernet | No | | | | | | | | | |
| **I$^2$C** | 1 | | | | | | | | | |
| LCD | No | | | | | | | | | |
| 32 kHz Oscillator | Yes | | | | | | | | | |
| **GPIO[5]** | 77 | 121 | 77 | 77 | 121 | 77 | 77 | 121 | 121 | 77 |
| **Debug** | JTAG | JTAG | JTAG | JTAG | JTAG | JTAG | JTAG | JTAG | Nexus2+ | JTAG |
| **Package** | 100 TQFP | 144 TQFP | 100 TQFP | 100 TQFP | 144 TQFP | 100 TQFP | 100 TQFP | 144 TQFP | 208 BGA | 100 TQFP |

NOTES:
[1] Feature set dependent on selected peripheral multiplexing—table shows example implementation
[2] Based on 105°C ambient operating temperature
[3] Refer to eMIOS200 section for information on the channel configuration and functions
[4] IC - Input Capture; OC - Output Compare; PWM - Pulse Width Modulation; MC - Modulus counter
[5] Estimated I/O count for proposed packages based on multiplexing with peripherals

## 3.2    Feature List

- Operating Parameters
  - Fully static operation, 0 MHz - 64 MHz
  - -40 °C - 105 °C junction temperature operating range
- Power management features
  - Four user-configurable RUN modes in which the entire device is powered but different clocks and power configurations can be supported with respect to each other. Switching run modes can be done quickly and easily
  - HALT mode in which the core clocks are stopped but user selected peripheral tasks can continue to run
  - STOP mode in which all clocks are stopped
  - STANDBY mode in which clocks to the entire device are halted and power to the majority of modules is off
  - Software-controlled clock gating of peripherals
  - Fast wake-up using the on-chip 16 MHz internal RC oscillator allows rapid execution from RAM on exit from low power modes.
- High performance, low cost e200z0 core processor
  - Single issue, 32-bit CPU core complex (e200z0)
  - Compliant with the Power Architecture™ embedded category
  - Includes an instruction set enhancement allowing variable length encoding (VLE) for code size footprint reduction. With the optional encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction.
- Fabricated in 90 nm process results in more features at lower cost
- 1.2 V internal logic for low power consumption
- Single power supply with 5.0 V ± 10% (4.5 V to 5.5 V) with internal regulator to provide 1.2 V for the core
- Designed with EMI reduction techniques
  - Phase-locked loop
  - Frequency modulation of system clock frequency
  - On-chip bypass capacitance
- Advanced microcontroller bus architecture (AMBA) crossbar switch (XBAR) provides concurrent access to peripherals, flash and SRAM
  - Two master ports, three slave ports
    - Masters: CPU instruction bus; CPU data bus
    - Slave: flash and SRAM via MPU; peripheral bridges (2)
- 32-bit internal address bus, 64-bit internal data bus
- On-chip ECC flash memory with flash controller
  - Up to 512 KB program flash—single module with prefetch buffer and 128-bit data access port

— 64 KB data flash—single module with prefetch buffer and 128-bit data access port
- Up to 32 KB on-chip ECC RAM with RAM controller
  — Up to 24 KB primary RAM and 8 KB backup
  — Can be accessed by byte, 16-bit halfword or 32-bit word
- Boot assist module (BAM) with 8 KB dedicated ROM for embedded boot code
  — Supports internal flash programming via a serial link (CAN or SCI)
- System Timers:
  — Four Software Timer Module (STM) timers
    – 32-bit up counter with 8-bit prescaler
    – Clocked from system clock
    – Four-channel timer compare hardware
    – Each channel can generate a unique interrupt request
    – Designed to address AUTOSAR task monitor function
  — Six Peripheral Interrupt Timer (PIT) timers (including ADC trigger)
    – 32-bit counter resolution
  — System watchdog timer
    – 32-bit timer
    – Clocked by system clock or crystal clock
    – Can generate either system reset or non maskable interrupt followed by system reset
    – Enabled out of reset
  — Real Time Counter (RTC) with clock source from internal 128 KHz or 16 MHz oscillator supporting autonomous wake-up with 1 mS resolution with max timeout of 2 seconds.
    – Optional support for Real Time Counter (RTC) with clock source from external 32 KHz crystal oscillator, supporting wake-up with 1-sec. resolution and max timeout of 1 hour.
- Safety and integrity features:
  — Clock Monitor Unit (CMU) for safe oscillator/PLL control using internal RC oscillator reference
  — Watchdog with time window for reload
  — Memory Protection Unit (MPU): eight regions with 32-bit granularity
  — Protected accesses to critical peripherals
- Interrupt controller (INTC) with 149 peripheral interrupt sources, including 16 external interrupts
- 10-bit analog-to-digital converter (ADC) with a minimum conversion time of 2 μs
  — 16 internal channels
  — 20 extended channels, 4 being expandable to up to 32 external channels
- Two 28-channel enhanced modular Input Output System (eMIOS) modules provide ability to generate or measure time events
  — 16-bit counter width
  — Configurable—can implement:

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    – Up to 56 IC/OC channels

    – Up to 48 pulse width modulation (PWM) channels

    – Up to 8 modulus counters

- Four Local Interconnect Network (LIN) controller modules capable of autonomous message handling (master), autonomous header handling (slave mode), and UART support. Compliant with LIN protocol rev. 2.1

- Three DSPI (Deserial Serial Peripheral Interface) modules for full-duplex, synchronous, communications with external devices

- Inter-integrated circuit ($I^2C$) module with master/slave bus interface

- Six Controller Area Network (FlexCAN) modules compliant with the CAN protocol version 2.0 C. The bit rate can be programmed up to 1 Mb/s

- Frequency modulated phase-locked loop (FMPLL)

- Up to 121 (77 in 100 TQFP package and 121 in 144 TQFP package) configurable general purpose pins supporting input and output operations (package dependent)

- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class Two Plus

- Device/board boundary scan testing supported with per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)

- MPC560xB/C family members are offered in the following package types:

    — 100-pin TQFP, 0.5mm pitch, 14 mm x 14 mm outline

    — 144-pin TQFP, 0.5mm pitch, 20 mm x 20 mm outline

## 3.3 Feature Details

### 3.3.1 Low Power Operation

MPC560xB/C devices have two dynamic power modes—RUN and HALT—and two static low-power modes—STANDBY and STOP.

Both low power modes use clock gating to halt the clock for all or part of the device. The STOP mode also uses power gating to automatically turn off the power supply to parts of the device to minimize leakage.

RUN modes are the main operating mode where the entire device can be powered and clocked. Four dynamic RUN modes are supported—RUN0 - RUN3. The ability to configure and select different RUN modes enables different clocks and power configurations to be supported with respect to each other and to allow switching between different operating conditions. The necessary peripherals, clock sources, clock speed and systems clock prescalers can be independently configured for each of the four RUN modes of the device.

HALT mode is a reduced activity, low power mode intended for moderate periods of lower processing activity. In this mode the core system clocks are stopped but user-selected peripheral tasks can continue to run. It can be configured to provide more efficient power management features (switch-off PLL, flash memory, main regulator, etc.) at the cost of longer wake up latency. The system returns to RUN mode as soon as an event or interrupt is pending.

STOP mode maintains power to the entire device allowing the retention of all on-chip registers and memory, and providing a faster recovery low power mode than the lowest STANDBY mode. There is no need to reconfigure the device before executing code. The clocks to the core and peripherals are halted and can be optionally stopped to the oscillator or PLL at the expense of a slower start-up time.

STOP is entered from RUN mode only. Wake-up from STOP mode is triggered by an external event or by the internal periodic wake-up, if enabled.

STANDBY mode halts the clock to the entire device and turns off the power to the majority of the chip to offer the lowest power consumption mode.

The device can be awakened from STANDBY mode via from any of up to 18 I/O pins, a reset or from a periodic wake-up using a low power oscillator. If required, it is possible to enable the internal 16 MHz or 128 KHz RC oscillator or external 32 KHz oscillator.

In STANDBY mode the contents of the cores, on-chip peripheral registers and potentially some of the volatile memory are not held.

- STANBDY2 mode retains the full contents of the on-chip RAM
- STANDBY1 mode retains 8K of the on-chip RAM

## Table 2. Operating Mode Summary[1,2]

| Operating Modes | SOC Features | | | | Clock Sources | | | | Periodic Wake-up | Wake-up input | VREG mode | Wake-up Time[3] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Core | Peripherals | Flash | RAM | PLL | 16MHz IRC | X OSC | 128KHz IRC | | | | VREG start-up | IRC Wake-up | Flash Recovery | OSC Stabilization | PLL Lock | S/W Reconfig | Mode switch over |
| RUN | On | OP | OP | On | OP | On | OP | On | — | — | FP | — | — | — | — | — | — | — |
| HALT | CG | OP | OP | On | OP | On | OP | On | OP | OP | FP | — | — | — | — | — | — | TBD |
| STOP | CG | CG | CG | On | CG | OP | OP | On | OP | OP | LP | 20 µs | 8 µs | >125 µs | 8 mS | 200 µs | — | 24 µs |
| STANDBY | Off | Off | Off | CG[4] | Off | OP | Off | OP | OP | OP | LP | 20 µs | 8 µs | >125 µs | 8 mS | 200 µs | Var | 28 µs |
| | Off | Off | Off | 8K[5] | Off | OP | Off | OP | OP | OP | LP | 20 µs | 8 µs | >125 µs | 8 mS | 200 µs | Var | 28 µs |
| POR | | | | | | | | | | | | 250 µs | 8 µs | >125 µs | 8 mS | 200 µs | | BAM |

NOTES:

[1] The values in this table are preliminary and subject to change without notice.

[2] Table Key:

   On- Powered and clocked

   OP- Optionally configurable to be enabled or disabled (clock gated)

   CG- Clock Gated, Powered but clock stopped

   Off- Powered off and clock gated

   FP- VREG Full Performance mode

   LP- VREG Low Power mode, reduced output capability of VREG but lower power consumption

   Var- Variable duration, based on the required reconfiguration and execution clock speed

   BAM- Boot Assist Module Software and Hardware used for device start-up and configuration

[3] A high level summary of some key durations that need to be considered when recovering from low power modes. This does not account for all durations at wake up. Other delays will be necessary to consider including, but not limited to the external supply start-up time.

   IRC Wake-up time must not be added to the overall wake-up time as it starts in parallel with the VREG.

   All other wake-up times must be added to determine the total start-up time, e.g. out of STANDBY if flash is needed the total wake-up time will be >125 µs.

[4] All RAM content is retained, but not accessible in STANDBY mode

[5] 8 KB of the RAM content is retained, but not accessible in STANDBY mode

## 3.3.2    e200z0 Core Processor

The e200z0 processor is similar to other processors in the e200zx series but supports only the VLE instruction set and does not include the signal processing extension for DSP applications or a floating point unit.

The e200z0 processor utilizes a four stage in-order pipeline for instruction execution. The Instruction Fetch (stage 1), Instruction Decode/Register file Read/Effective Address Calculation (stage 2), Execute/Memory Access (stage 3), and Register Writeback (stage 4) stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

The integer execution unit consists of a 32-bit Arithmetic Unit (AU), a Logic Unit (LU), a 32-bit Barrel shifter (Shifter), a Mask-Insertion Unit (MIU), a Condition Register manipulation Unit (CRU), a Count-Leading-Zeros unit (CLZ), an 8x32 Hardware Multiplier array, result feed-forward hardware, and a hardware divider.

Most arithmetic and logical operations are executed in a single cycle with the exception of the divide and multiply instructions. A Count-Leading-Zeros unit operates in a single clock cycle. The Instruction Unit contains a PC incrementer and a dedicated Branch Address adder to minimize delays during change of flow operations. Sequential prefetching is performed to ensure a supply of instructions into the execution pipeline. Branch target prefetching is performed to accelerate taken branches. Prefetched instructions are placed into an instruction buffer capable of holding two instructions.

Conditional branches not taken execute in a single clock. All other taken branches have an execution time of two clocks.

Memory load and store operations are provided for byte, halfword, and word (32-bit) data with automatic zero or sign extension of byte and halfword load data as well as optional byte reversal of data. These instructions can be pipelined to allow effective single cycle throughput. Load and store multiple word instructions allow low overhead context save and restore operations. The load/store unit contains a dedicated effective address adder to allow effective address generation to be optimized. Also, a load-to-use dependency does not incur any pipeline bubbles for most cases.

The Condition Register unit supports the condition register (CR) and condition register operations defined by the Power Architecture. The condition register consists of eight 4-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching.

Vectored and autovectored interrupts are supported. Vectored interrupt support is provided to allow multiple interrupt sources to have unique interrupt handlers invoked with no software overhead.

The CPU includes support for Variable Length Encoding (VLE) instruction enhancements. This allows the classic Power Architecture instruction set to be represented by a modified instruction set made up from a mixture of 16 bit and 32 bit instructions. This results in a significantly smaller code size footprint without affecting performance noticeably.

The CPU core has an additional 'Wait for Interrupt' instruction that is used in conjunction with low power STOP mode. When Low Power Stop mode is selected, this instruction is executed to allow the system clock to be stopped. An external interrupt source or the system wake-up timer is used to restart the system clock and allow the CPU to service the interrupt.

### 3.3.3 Crossbar

The XBAR multi-port crossbar switch supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows for three concurrent transactions to occur from the master ports to any slave port; but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. Requesting masters will be treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- Two master ports:
  - e200z0 core instruction port
  - e200z0 core complex data port
- Three slave ports
  - Flash and SRAM memory (via the Memory Protection Unit)
  - Peripheral bridge 0 (MCM, STM, SWT INTC)
  - Peripheral bridge 1 (BAM, SIUL, I$^2$C, and FlexCAN, LINFlex, DSPI, eMIOS, FMPLL, PIT, CTU Lite, ADC, SSCM, RTC)
- 32-bit internal address, 64-bit internal data paths

### 3.3.4 Interrupt Controller (INTC)

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC allows interrupt request servicing from up to 149 interrupt sources, including 16 external interrupts and 8 software interrupts..

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

Multiple processors can assert interrupt requests to each other through software setable interrupt requests. These same software setable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software setable interrupt request to finish the servicing in a lower priority ISR. Therefore these software setable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS.

The INTC provides the following features:

- 149 peripheral interrupt request sources (includes 16 external interrupts)
- Eight software setable interrupt request sources
- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register
- Each interrupt source can be programmed to one of 16 priorities
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency - three clocks from receipt of interrupt request from peripheral to interrupt request to processor

## 3.3.5 FMPLL

The FMPLL enables the user to generate high speed system clocks from a 4 MHz to 20 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 20 MHz
- Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz, resulting in system clock frequencies from 16 MHz to 80 MHz with granularity of 4 MHz or better
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Three modes of operation—the default mode is PLL off in DRUN system mode
  — Bypass mode with PLL off
  — Bypass mode with PLL running (default mode out of reset)
  — PLL normal mode
- Each of the three modes may be run with a crystal oscillator or an external clock reference
- Programmable frequency modulation
  — Modulation enabled/disabled through software
  — Triangle wave modulation up to 100 kHz modulation frequency
  — Programmable modulation depth (0% to 2% modulation depth)
  — Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Monitor Unit

— detects the quality of the crystal clock and cause interrupt request or system reset if error is detected
— detects the quality of the PLL output clock. If an error is detected, causes a system reset or switches the system clock to the crystal clock and causes an interrupt request.

- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation

## 3.3.6     System Integration Unit Lite (SIUL)

The SIUL controls reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the $\overline{\text{RSTOUT}}$ pin. The SIU is accessed by the e200z0 core through the peripheral bridge and crossbar switch. The SIU provides the following features:

- System configuration
  — Critical register configuration protected against change with soft lock for temporary guard or hard lock to prevent modification until next reset.
  — MCU reset configuration via external pins
  — Pad configuration control for each pad
- System reset monitoring and generation
  — Power-on reset support
  — Reset status register provides last reset source to software
  — Glitch detection on reset input
  — Glitch filtering (no detection for glitch below 40 ns)
  — Software controlled reset assertion
- External interrupt
  — Sixteen external interrupt requests
  — Rising or falling edge event detection
  — Programmable digital filter for glitch rejection
  — Critical Interrupt request (configurable on the wake-up unit module)
  — Non Maskable Interrupt request
- GPIO
  — Centralized general purpose input output (GPIO) control of up to 121 input/output pins (121 pins on the 144-pin package and 77 pins on the 100-pin package)
  — Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
  — All peripheral pins can be alternatively configured as both general purpose input or output pins except ADC channels which support alternative configuration as general purpose inputs, with selected pins able to also support outputs.

— Direct readback of the pin value supported on all digital output pins through the SIU

— Configurable digital input filter that can be applied to up to 16 general purpose input pins for noise elimination on external interrupts

— Dedicated input and output registers for setting each GPIO & Virtual GPIO pin

— All GPIO pins can be independently configured to support pull-up pull-down, or no pull (no pull-up or pull-down on ADC precision channels)

- Internal Multiplexing

— Up to four levels of internal pin multiplexing, allowing exceptional flexibility in the allocation of device functions for each package

### 3.3.7    Flash

The MPC560xB/C provides up to 512 KB of programmable, non-volatile flash memory for programs and 64 KB for data. Each flash module includes a Fetch Accelerator that optimizes the performance of the flash array to match the CPU architecture and provides single cycle random access to the flash at 64 MHz. The flash modules interface to the system bus via a dedicated flash memory array controller and memory protection unit. For CPU loads and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains a four-entry, 128-bit prefetch buffer and a prefetch controller which prefetches sequential lines of data from the flash array into the buffer. Prefetch buffer hits allow no-wait responses. Normal flash array accesses are registered and are forwarded to the system bus on the following cycle, incurring three wait-states. Prefetch operations may be automatically controlled, and are restricted to instruction fetch.

The on-chip flash memory provides the following features:

- 64-bit data bus for instruction fetch and CPU loads. Byte, halfword, word and doubleword reads are supported. Only aligned doubleword writes are supported.
- Fetch Accelerator
    — Architected to optimize the performance of the flash with the CPU to provide single cycle random access to the flash up to 64 MHz system clock speed
    — Configurable read buffering and line prefetch support
    — Four line read buffers (128 bits wide) and a prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0-31 additional cycles) allowing use for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (4 words)
- ECC with single-bit correction, double-bit detection
- ECC single bit error corrections are visible to software

- Minimum program size is two consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Embedded hardware program and erase algorithm
- Erase suspend program
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

### 3.3.8    SRAM

The MPC560xB/C SRAM module provides up to a general-purpose 24 KB memory block and an 8 KB backup block. The SRAM controller includes these features:

- Supports read/write accesses mapped to the SRAM memory from any master
- Byte, halfword and word addressable for optimal use of memory
- ECC performs single bit correction, double bit detection on 32 bit data element
- User transparent ECC encoding and decoding for byte, half word, and word accesses
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait-state for 8- and 16-bit writes if back to back with a read to same memory block
- Separate internal power domain applied to 24 KB RAM block and 8 KB RAM block during STANDBY modes to retain contents during low power mode

### 3.3.9    Memory Protection Unit (MPU)

The MPU provides eight region descriptors and 32-byte granularity. Features include:

- Support for overlapping regions
- Protection attributes can optionally include process ID
- Protection offered for three concurrent read ports
- Read and write attributes for all masters
- Execute and supervisor/user mode attributes for processor masters

### 3.3.10    Boot Assist Module (BAM)

The BAM is a block of read-only memory that is programmed once by Freescale and is identical for all MPC560xB/C MCUs. The BAM program is executed every time the MCU is powered-on or reset. During execution, BAM code searches for user-supplied boot code and, if none is found, executes the BAM boot code resident in device ROM. The BAM supports two different modes of booting:

- Booting from internal flash memory
- Serial boot loading (A program is downloaded into RAM via LINFlex or FlexCAN and then executed)

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the MPC560xB/C hardware accordingly. The BAM provides the following features:

- Detection of user boot code

- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus with or without auto baud rate sensing
- Supports censorship protection for internal flash memory
- Provides an option to enable the core watchdog timer

### 3.3.11    eMIOS

The two eMIOS modules provides the functionality to generate or measure events. Each module has 28 channels and a 16-bit counter width. The modules are software-configurable and can implement up to 56 IC/OC channels, up to 48 pulse width modulation (PWM) channels, and up to 8 modulus counter.

### 3.3.12    DSPI

Three Deserial Serial Peripheral Interface (DSPI) blocks provide a synchronous serial bus for communication between the MCU and external peripheral devices. Each DSPI module operates as a basic SPI or as a queued SPI through the use of internal FIFOs. For queued operations the SPI queues reside in system RAM, external to the DSPI. Data transfers between the queues and the DSPI FIFOs are accomplished through host software.

#### NOTE
The MPC560xB/C does not offer DMA support and no Deserial/Serial Interface (DSI) implemented.

### 3.3.13    FlexCAN

The MPC560xB/C MCU contains six controller area network (FlexCAN) modules. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B.

The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

Each FlexCAN module in the MPC560xB/C includes two embedded memories, one for storing Message Buffers (MB) and another for storing Rx Individual Mask Registers. Support for 64 Message Buffers is provided.

It is possible to operate the bxcan bit timing logic with either system clock or external main oscillator clock (XOSCHS).

The FlexCAN modules provide the following features:

- Full Implementation of the CAN protocol specification, Version 2.0B
    — Standard data and remote frames
    — Extended data and remote frames
    — Zero to eight bytes data length

- — Programmable bit rate up to 1 Mb/sec
- 64 mailboxes, each configurable as transmit or receive
  - — Mailboxes configurable while module remains syncronised to CAN bus
- Transmit features
  - — Supports configuration of multiple mailboxes to form message queues of scalable depth
  - — Arbitration scheme according to message ID or message buffer number
  - — Internal arbitration to guarantee no inner or outer priority inversion
  - — Transmit abort procedure and notification
- Receive features
  - — Individual programmable filters for each mailbox
  - — Eight mailboxes configurable as a 6-entry receive FIFO
  - — Eight programmable acceptance filters for receive FIFO
- Programmable clock source
  - — system clock
  - — Direct oscillator clock to avoid PLL jitter
- Listen only mode capabilities

## 3.3.14 System Clocks and Clock Generation

The following list summarizes the system clock and clock generation on the MPC560xB/C microcontroller:

- System clock can be derived from the following sources
  - — External crystal oscillator
  - — FMPLL
  - — 16 MHz internal RC oscillator
- Programmable output clock divider of system clock ($\div 1$, $\div 2$, $\div 4$)
- Separate programmable peripheral bus clock divider ratio ($\div 1$, $\div 2$, $\div 4$) applied to system clock
- Frequency Modulated Phase-locked loop (FMPLL)
  - — Input clock frequency from 4 MHz to 16 MHz
  - — Selectable Clock source from external oscillator or internal 16-MHz RC oscillator
  - — Lock detect circuitry continuously monitors lock status
  - — Loss-of-clock detection for reference and feedback clocks
  - — On-chip loop filter (for improved electromagnetic interference performance and reduces number of external components required)
- On-chip crystal oscillator supports 4 MHz to 16 Mhz crystals
- Dedicated 16 MHz internal RC oscillator
  - — Used as default clock source out of reset
  - — Provides a clock for rapid start-up from low power modes

— Provides a back-up clock in the event of PLL or External oscillator clock failure

— Offers an independent clock source for the Watchdog timer

— 5% accuracy over the operating temperature range

— Trimming registers to support frequency adjustment with in-application calibration

- Dedicated internal 128 KHz internal RC oscillator for low power mode operation and self wake-up

  — 5% accuracy

  — Trimming registers to support improve accuracy with in-application calibration

  — 32 KHz low power external oscillator for low power real time clock

## 3.3.15    System Timers

The system timers include:

- System Timer Module (STM) timers
- Peripheral Interrupt Timer (PIT) timers (including ADC trigger)
- One Real Time Counter (RTC) timer

The System Timer Module (STM) is a 32-bit timer designed to support commonly required system and application software timing functions. The STM includes a 32-bit up counter and four 32-bit compare channels with a separate interrupt source for each channel. The counter is driven by the system clock divided by an 8-bit prescaler value (1 to 256).

The PIT is an array of timers that can be used to raise interrupts and trigger CTUL channels. It features the following:

- Up to six general purpose interrupt timers
- Up to two interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by system clock frequency
- 32-bit counter for real time interrupt, clocked from main external oscillator

The RTC supports wake-up from low power modes or real time clock generation

- Configurable resolution for different timeout periods

  — 1 sec resolution for >1 hour period

  — 1 ms resolution for a two second period

- Selectable clock sources from external 32 KHz crystal, internal 128 KHz RC oscillator or divided internal 16 MHz RC oscillator
- Supports continued operation through Reset, count only Reset manually or by POR

## 3.3.16    System Software Watchdog

The system software watchdog is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The system software watchdog is a 32-bit modulus

counter clocked by the system clock or the crystal clock that can provide a system reset or interrupt request, when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Selectable clock source—main system clock or internal 16 MHz RC oscillator clock
- Supports normal or windowed mode
- Configurable response on timeout: reset, interrupt, or interrupt followed by reset
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Support for protected access to Watchdog control registers with optional soft and hard locks
    — Soft lock allows temporary locking of configuration
    — Hard lock prevents any changes until after a Reset, once enabled
- Supports halting during low power modes

## 3.3.17 Inter-Integrated Circuit (I$^2$C) Module

The I$^2$C module features the following:

- Two-wire bi-directional serial bus for on-board communications
- Compatibility with I$^2$C bus standard
- Multimaster operation
- Software-programmable for one of 256 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

## 3.3.18 On-Chip Voltage Regulator (VREG)

The on-chip voltage regulator includes

The on-chip regulator in the MPC560xB/C regulates 3.3 V ±10% or 5 V ±10% input to generate all internal supplies. It is comprised of three regulators:

- High power
- Low power
- Ultra-low power

The nominal target output is 1.2 V with a full current load range 0 to 200 mA (4 ballast) provided through internal PMOS ballasts. The high power and low power regulators are switched off during standby mode to save consumption from the regulator itself. During STOP mode only the high power regulator is switched off. The ultra-low power regulator is always kept on. The regulator has 2 digital domain LVDs - one for the high power and lower power domain and one for the ultra-low power domain.

### 3.3.19   Analog to Digital Converter Module (ADC)

The ADC module contains advanced features for Normal, Injected and triggered injected conversion, along with offset cancellation and offset refresh control. It supports an interface to the cross triggering unit lite (CTUL).

There are three types of input channels available: internal precision channels, extended channels and external channels. Control registers within the ADC can be programmed to configure which channel is to be converted. External channel selection is provided through three external decode signals. A conversion timing register that allows to configure different sampling and conversion times is associated to each type of channel.

The ADC provides 10-bit conversion with a minimum conversion time of 2 μs. It features one shot/scan mode conversion, hardware chain injection mode. It also provides four watchdog channels to monitor whether signals remain within a defined range. A dedicated power-down mode is implemented to save power consumption.

The ADC features the following:

- 10-bit A/D resolution
- 0 to $V_{DD}$ common mode conversion range
- Conversions speeds up to 2 μs
- Up to 36 single-ended input channels, expandable to 64 channels with external multiplexers
- Internally multiplexed channels
  — 10-bit ± 2 counts accuracy (TUE) available for 16 channels
  — 10-bit ± 3 counts accuracy (TUE) available for up to 20 channels
  — Dedicated result register available for every internally muxed channel
- Externally multiplexed channels
  — Internal control to support generation of external analog multiplexor selection
  — Three internal channels optionally used to support externally multiplex inputs, providing transparent control for additional ADC channels
  — Each of the three channels supports up to eight externally muxed inputs
  — One result register per internal channel
- Right-aligned result format
- Support for one-shot, scan and injection conversion modes
- Independently configurable parameters for channels:
  — Offset refresh
  — Sampling

- Conversion triggering support
  — Internal conversion triggering from periodic interrupt timer (PIT) or timed I/O module (eMIOS)
- Four configurable analog comparator channels offering range comparison with triggered alarm
  – Greater than
  – Less than
  – Out of range
- All unused analog pins available as general-purpose input pins
- Selected unused analog pins available as general-purpose output pins
- Power-down mode

### 3.3.20  Nexus Port Controller

The IEEE-ISTO 5001-2003 standard defines an extensible auxiliary port which is used in conjunction with the JTAG port in the e200z0. The Nexus modules are coupled to the core and monitor a variety of signals including addresses, data, control signals, status signals, etc.

The NPC (Nexus Port Controller) block provides real-time development support capabilities for the MPC560xB/C Power Architecture-based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The development support provided includes program trace and run-time access to the MCU's internal memory map and access to the e200z0 processor core during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins.

Supported Nexus 2 Plus features include:
  — Static debug
  — Watchpoint messaging
  — Ownership trace messaging
  — Program trace messaging
  — Real time read/write of any internally memory mapped resources through JTAG pins
  — Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information
  — Watchpoint triggering, watchpoint triggers program tracing

### 3.3.21  JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format.

# 4 Application Examples

## 4.1 Body Controller Application Example

Body controller modules primarily control interior features of the car, such as:

- Comfort features—doors, seats, interior lighting
- Security/access features—passive entry, immobilizer, TPMS (Tire Pressure Monitoring System)
- Lighting—headlights, brake lights, turn lights
- Centralized diagnostic and network management

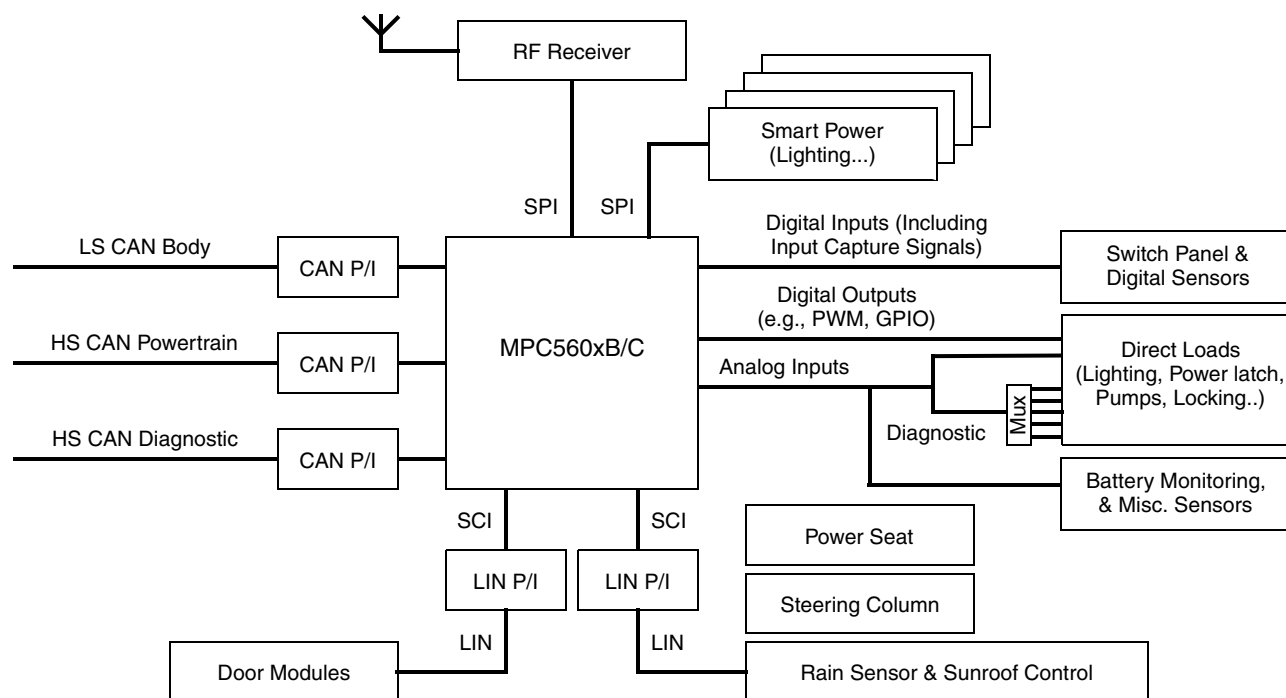Figure 2 shows the MPC560xB/C used in a typical body controller application.



**Figure 2. Body Controller Application Example**

## 4.2 Door Controller Application Example

These modules are used to locally control the functions contained within the vehicle doors that are rapidly increasing in complexity. By adding local control within the door the number of wires to the door can be significantly reduced which helps reduce the wiring harness weight, simplifies assembly and reduces fault prone connectors.

The communication with other body controllers in the main cabin compartment is often via the CAN bus, and they may also support LIN communications to other nodes such as keypads or between the front and rear door modules. Some door controllers handle the window lift function with sensors and brushed DC motors. This is often implemented to reduce the number of components, increase reliability and flexibility and minimize system cost, and normally requires the greatest level of performance to manage.

Figure 3 shows the MPC560xB/C used in a typical door controller application.
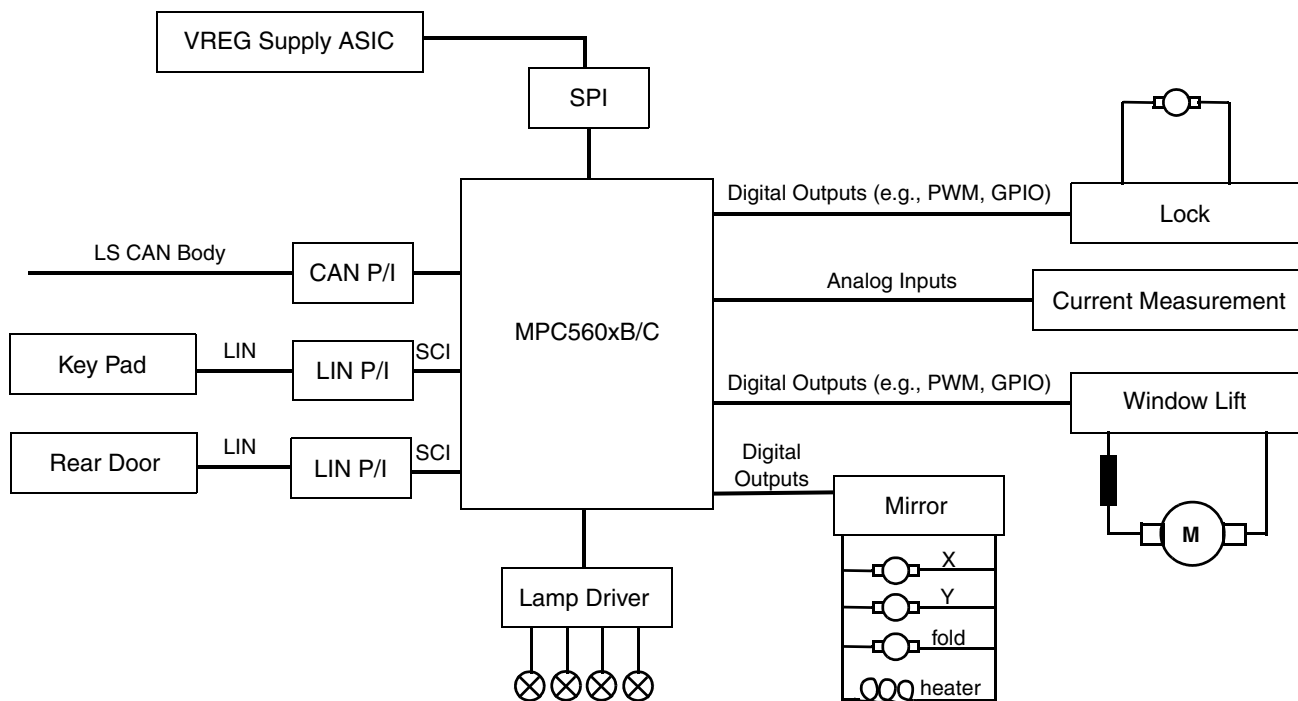


**Figure 3. Door Controller Application Example**

# 5    Developer Support

The MPC560xB/C MCU tools and third-party developers are similar to those used for the Freescale MPC5500 product family, offering a widespread, established network of tools and software vendors. It also features a high-performance Nexus debug interface.

The following development support will be available:

- Automotive evaluation boards (EVB) featuring CAN, LIN interfaces, and more
- Compilers
- Debuggers
- JTAG and Nexus interfaces

The following software support will be available:

- OSEK solutions will be available from multiple third parties
- CAN and LIN drivers
- AUTOSAR package

# 6 Orderable Parts

**Table 3. Orderable Part Number Summary**

| Part Number | Flash (KB) | SRAM (KB) | Package | Speed (MHz) |
|---|---|---|---|---|
| MPC5602B | 256 | 24 | 100 TQFP, 144 TQFP | 64 |
| MPC5602C | 256 | 32 | 100 TQFP | 64 |
| MPC5603B | 384 | 28 | 100 TQFP, 144 TQFP | 64 |
| MPC5603C | 384 | 32 | 100 TQFP | 64 |
| MPC5604B | 512 | 32 | 100 TQFP, 144 TQFP, 208 BGA | 64 |
| MPC5604C | 512 | 32 | 100 TQFP | 64 |

**Orderable Parts**

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