DAY #19

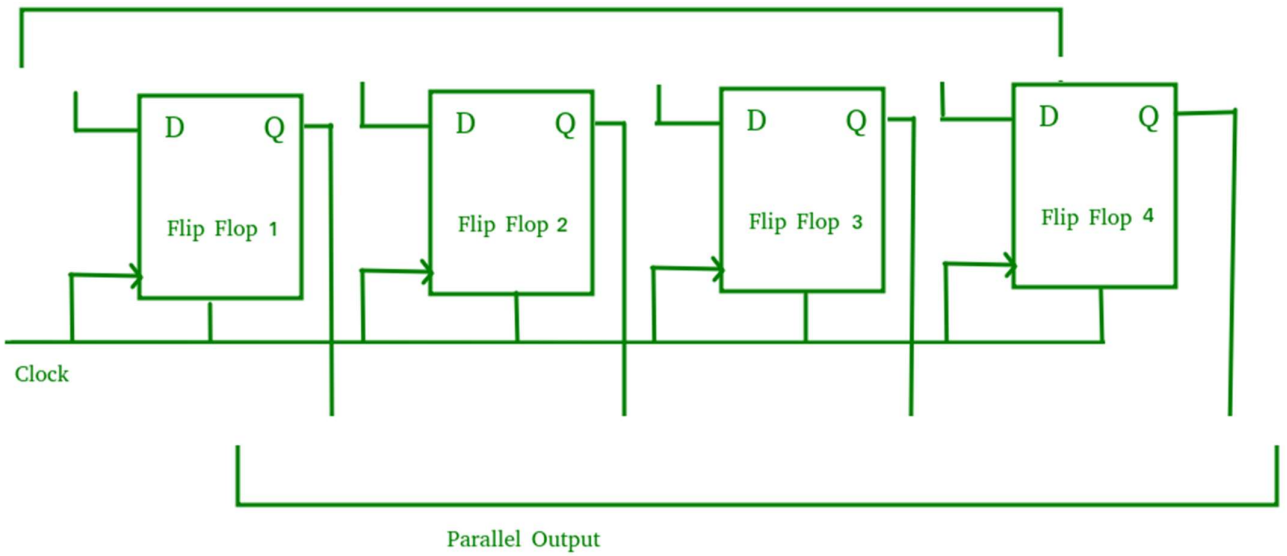
30 DAYS OF VERILOG

AIM – TO IMPLEMENT SIPOSHIFT REG.

A **Serial-In Parallel-Out (SIPO)** shift register is a sequential logic device that can store and shift data bits.

1. **Functionality**:
   - The SIPO shift register takes in data **one bit at a time** (serial input).
   - It processes the data internally.
   - Finally, it outputs the data **all at once** in parallel format.
2. **Example**:
   - Imagine you have a 4-bit SIPO shift register.
   - If you shift in four data bits via a single wire at the serial input (SI), the data becomes available simultaneously on the four outputs (QA, QB, QC, QD) after the fourth clock pulse.

SCHCEMATIC -



CODE –

```
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module sipo(input clr,clk,d, output reg [3:0]q );
reg [3:0]temp;
always @ (posedge clk)
if (clr==1)
q=4'b0000;
else
begin
temp=q>>1;
q={d,temp[2:0]};
end
endmodule
```

WAVEFORM –