DAY #15

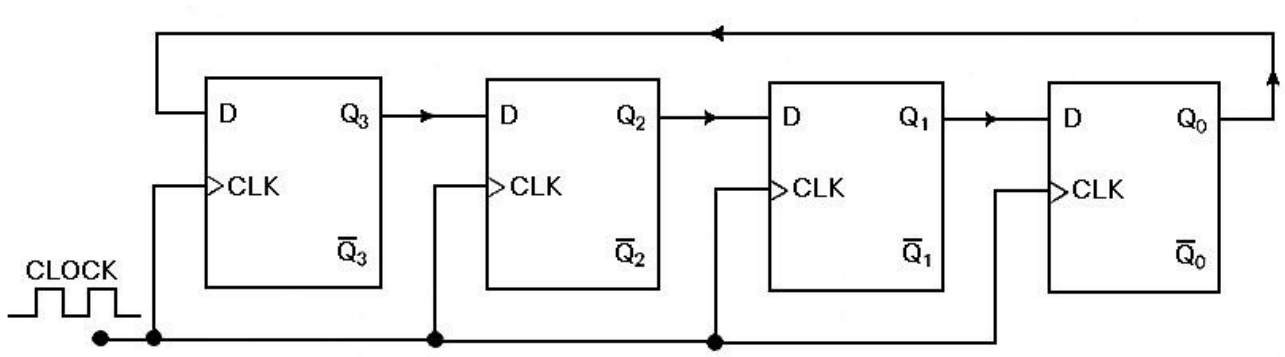
30 DAYS OF VERILOG

AIM – TO IMPLEMENT RIPPLE COUNTER

A Ripple counter is an asynchronous counter in which the aa the flip flops except the first are clocked by the output of the preceding flops.

In a ripple counter, only the first flip flop is clocked by an external clock signal. All subsequent flip flops are clocked by the output of the preceding flip-flop. Asynchronous counters are also called ripple counters because of the way the clock pulse “Ripples” through the flip-flops.

SCHEMATIC –



CODE –

```
22  module RCounter(q,clk,reset);
23      output [3:0] q;
24      input clk,reset;
25
26  Tff tff0(q[0],clk,reset);
27  Tff tff1(q[1],q[0],reset);
28  Tff tff2(q[2],q[1],reset);
29  Tff tff3(q[3],q[2],reset);
30
31  endmodule
32
33  module Tff(q,clk,reset);
34  output q;
35  input clk,reset;
36  wire d;
37
38  Dff dff0(q,d,clk,reset);
39  not n1(d,q);
40
41  endmodule
42
43  module Dff(q,d,clk,reset);
44  output q;
45  input d,clk,reset;
46  reg q;
47
48  always@(posedge reset or negedge clk)
49  if(reset)
50  q<=1'b0;
51  else
52  q<=d;
53
54  endmodule
55
```

```
54  endmodule
55
56  module stimulus;
57  reg clk,reset;
58  wire[3:0] q;
59
60  RCounter r1(q,clk,reset);
61
62  initial
63  clk=1'b0;
64
65  always
66  #5 clk=~clk; // toggle clock every 5 units
67
68  initial
69  begin
70   reset=1'b1;
71   #15 reset=1'b0;
72   #180 reset=1'b1;
73   #10 reset=1'b0;
74   #20 $finish;
75   end
76
77   initial
78   $monitor ($time, "Output q = %d",q);
79
80   endmodule
81
```

WAVEFORM –