DAY #10

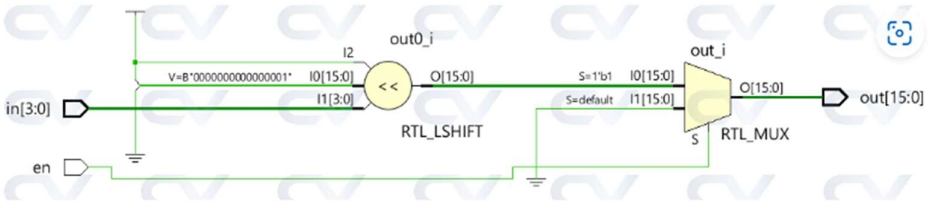
30 DAYS OF VERILOG

AIM – TO IMPLEMENT 4x16 DECODER

A **4-to-16 decoder** is a combinational circuit that takes a 4-bit binary input and produces a 16-bit output. It's commonly used in digital systems for address decoding, memory selection, and other applications.

A **decoder** circuit of the higher combination is obtained by adding two or more lower combinational circuits. 4 to 16 decoder circuit is obtained from two 3 to 8 decoder circuits or three 2 to 4 decoder circuits. When two 3 to 8 Decoder circuits are combined the enable pin acts as the input for both the decoders.

Schematic –



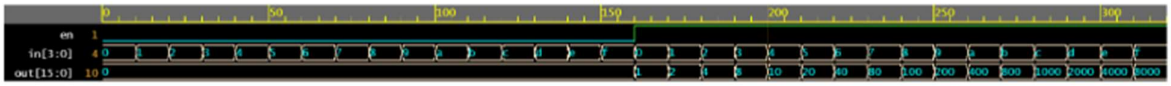
Verilog Code–

```
module dec_3x8 (    input           en,
                    input   [3:0]   in,
                    output  reg [15:0]  out);

  always @ (en or in) begin
    out = en ? 1 << in: 0;
  end

endmodule
```

Waveform –


0
50
100
150
200
250
300
en
in[3:0]
out[15:0]
1
4
10
0
1
2
4
8
10
20
40
80
100
200
400
800
1000
2000
4000
8000