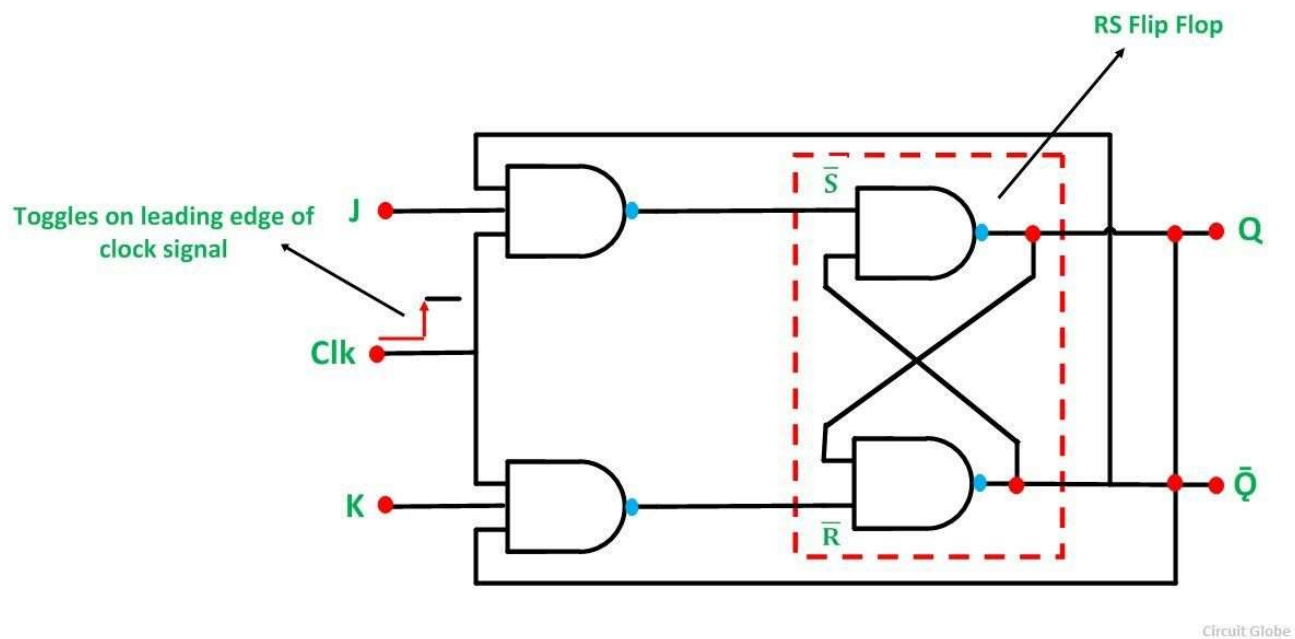


DAY #16

30 DAYS OF VERILOG

AIM – TO IMPLEMENT JK FLIP-FLOP

A **JK flip-flop** is a sequential logic circuit that can store one bit of binary information. It's named after its inventor, Jack Kilby, who was a Texas Instruments engineer and a co-inventor of the integrated circuit. The JK flip-flop has one clock input pin (CLK), two data input pins (J and K), and two output pins (Q and \bar{Q}).



CODE –

```
IMPLEMENTED DESIGN - xc7a200tbsbg484-1 (active)
Project Summary | Device | JK_FF.v | tb_JK.v |
C:/Users/sagni/Desktop/CAD_final_exam/1_K_FF.srscs/sources_1/new/JK_FF.v

23 module JK_FF(
24     input J,
25     input K,
26     input clk,
27     output Q,
28     output Q_bar
29 );
30
31 reg Q=0 ;
32 always@(posedge clk)
33     case({J,K})
34         2'b00: Q<=Q ;
35         2'b01: Q<=0 ;
36         2'b10: Q<=1 ;
37         2'b11: Q<=~Q ;
38     endcase
39     assign Q_bar=~Q ;
40 endmodule
41
```

WAVEFORM –

[illegible]