DAY #7

30 DAYS OF VERILOG

AIM – TO IMPLEMENT 4X1 MUX USING 2X1 MUX

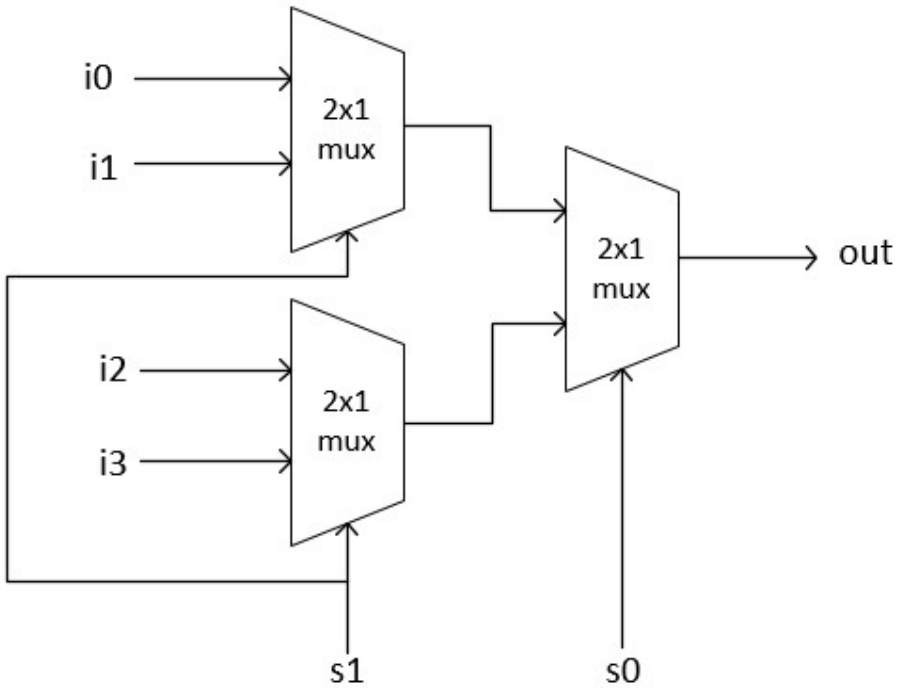
To design a **4:1 multiplexer (mux)** using a minimum number of **2:1 mux**, we can follow a partitioning approach.

Partition the 4:1 mux table into three sections based on the select lines (S1 and S0).

Truth Table –

INPUTS		Output
S_1	S_0	Y
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

Schematic –



Verilog Code–

design.sv

```
//-----------------------------------------
//          www.vlsiverify.com
//-----------------------------------------
module mux_2_1(
  input sel,
  input i0, i1,
  output y);

  assign y = sel ? i1 : i0;
endmodule

module mux_4_1(
  input sel0, sel1,
  input  i0,i1,i2,i3,
  output reg y);

  wire y0, y1;

  mux_2_1 m1(sel1, i2, i3, y1);
  mux_2_1 m2(sel1, i0, i1, y0);
  mux_2_1 m3(sel0, y0, y1, y);
endmodule
```

Waveform –