DAY #20

30 DAYS OF VERILOG

AIM – TO IMPLEMENT PIPO SHIFT REG.

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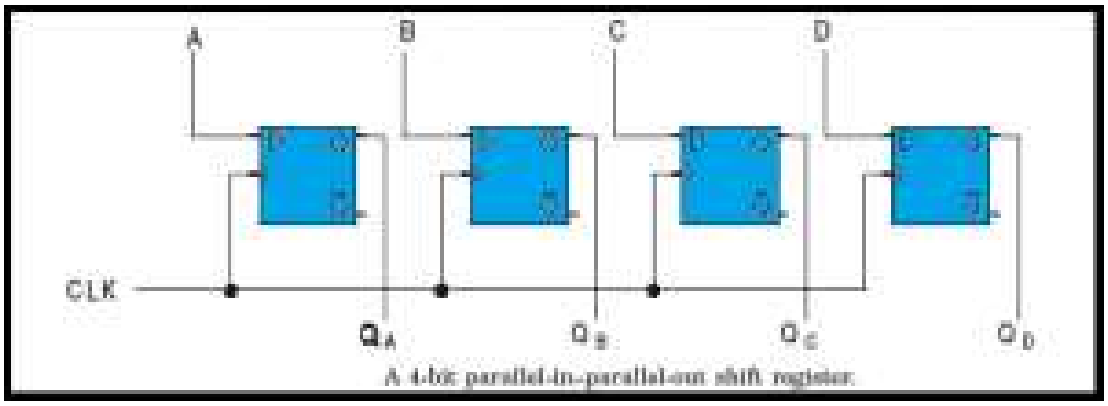
The PIPO module implements a Parallel In Parallel Out Register. It takes in these inputs (clk,reset,pipo_in,load) and an output (pipo_out).
If reset signal is HIGH, pipo_out = 0.

If load signal is HIGH, whatever new pipo_in is coming will be the output.

But, if the load signal is not high, then pipo_out should show the previously output value. Now what I'm doing is pipo_out = 0;

What changes can be done, so that when the load signal is not high, then pipo_out should show the previously output value.

SCHCEMATIC -



A 4-bit parallel-in–parallel-out shift register.

CODE –

```
// Design Name:
// Module Name:    pipo
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module pipo(q,clk,clr,d);
output reg [3:0]q;
input clk,clr;
input [3:0]d;
always @ (posedge clk)
if(clr==1)
q=4'b0000;
else
q=d;
endmodule
```

WAVEFORM –