DAY #13

30 DAYS OF VERILOG

AIM – TO IMPLEMENT 4 BIT COUNTER

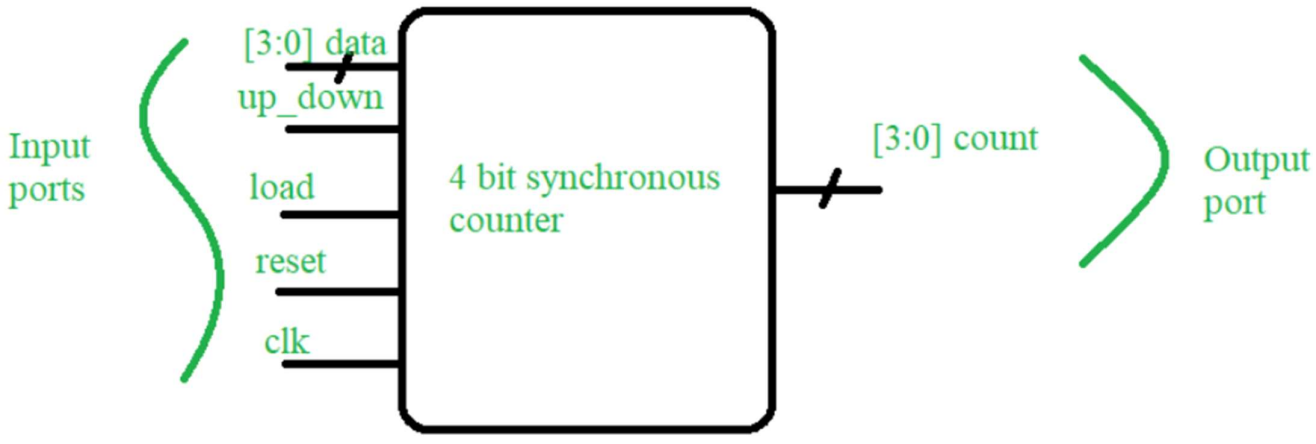
A 4-bit counter starts incrementing from 4'b0000 to 4'h1111 and then rolls back to 4'b0000. It will keep counting as long as it is provided with a running clock and the reset is held high.

The rollover happens when the most significant bit of the final addition gets discarded. When counter is at a maximum value of 4'b1111 and gets one more count request, the counter tries to reach 5'b10000 but since it can support only 4-bits, the MSB will be discarded resulting in 0.

0000
0001
0010
.....
1110
1111
Rolls over
0000
0001
.....

The design contains two inputs one for the clock and another for an active-low reset. An active-low reset is one where the design is reset when the value of the reset pin is 0. There is a 4-4bit output called out which essentially provides the counter values.

SCHEMATIC –



CODE –

```
// Create Date:    00:35:10 09/01/2016
// Design Name:
// Module Name:    counter
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module counter(
    input clk,
    input reset,
    output [3:0] y
    );
reg [3:0]y;
always @ (posedge(clk))
begin
if(reset==1'b1)
y=4'b0000;
else
y=y+1;
end
```

WAVEFORM –