
DAY #3

30 DAYS OF VERILOG

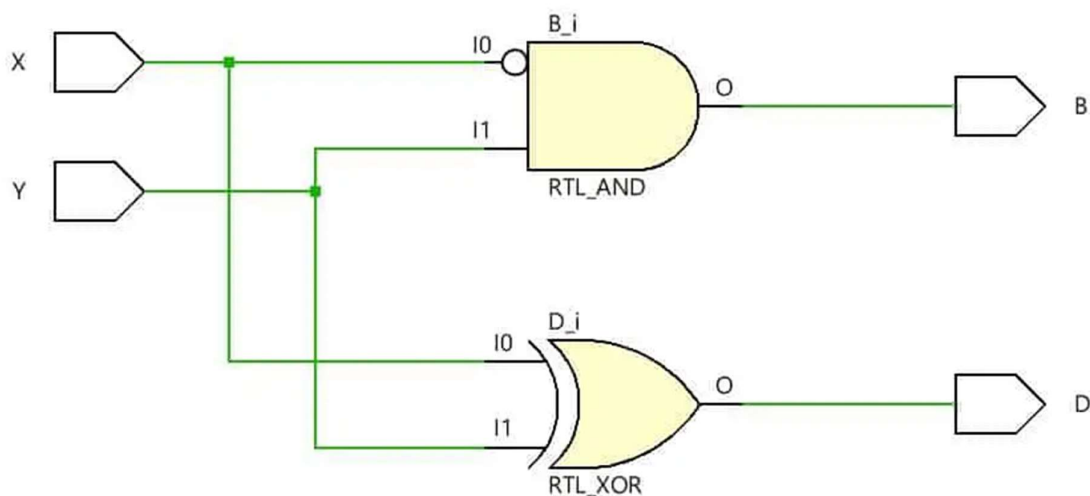
AIM – TO IMPLEMENT HALF SUBTRACTOR

The half subtractor works opposite to the half adder as it subtracts two single bits and results in a difference bit and borrow bit as an output.

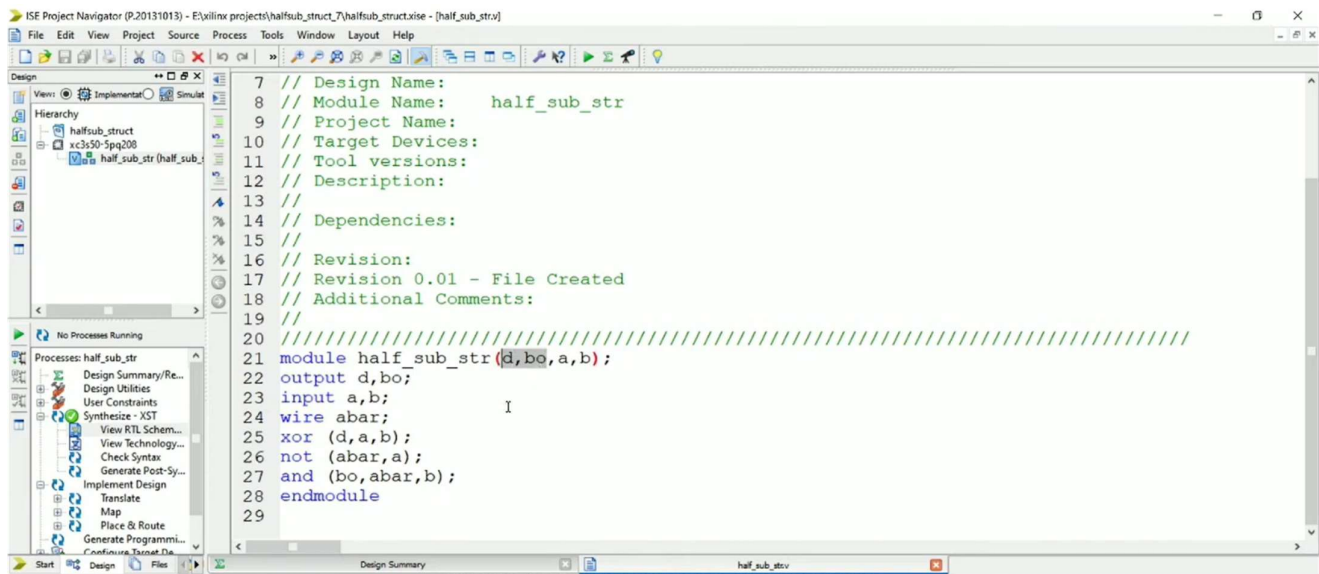
Truth Table –

Inputs		Outputs	
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Schematic –



Verilog Code–



The screenshot shows the ISE Project Navigator window with the Verilog code for a half-subtractor module. The code is as follows:

```
7 // Design Name:
8 // Module Name:    half_sub_str
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module half_sub_str(d,bo,a,b);
22 output d,bo;
23 input a,b;
24 wire abar;
25 xor (d,a,b);
26 not (abar,a);
27 and (bo,abar,b);
28 endmodule
29
```

Waveform –

