DAY #5

30 DAYS OF VERILOG

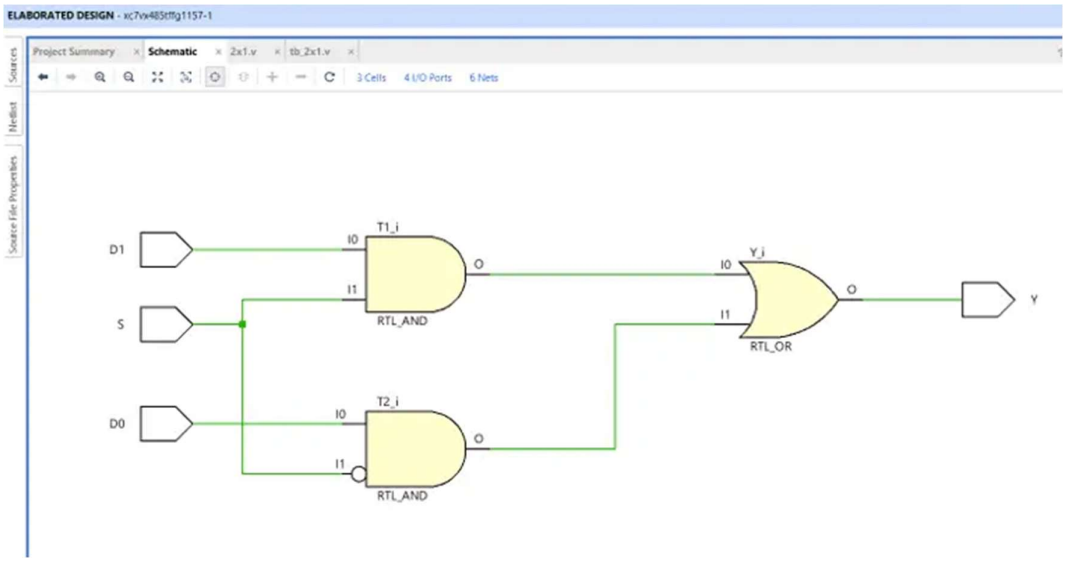
AIM – TO IMPLEMENT 2X1 MULTIPLEXER

A **Multiplexer** is a combinational circuit which has N **Selection Lines** and 2^N **Input Lines.**
Has only one output line.
The output depends upon the value of selection lines.
2x1 Multiplexer means it has 2 input lines and 1 output line.

Truth Table –

S	I_0	I_1	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Schematic –



Verilog Code–

```
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21 module demux_str(o,s,i);
22 output  [1:0]o;
23 input s,i;
24 assign o[0]=~s&i;
25 assign o[1]=s&i;
26 endmodule
27
```

Waveform –