DAY #9

30 DAYS OF VERILOG

AIM – TO IMPLEMENT 1x4 DEMUX

A **1x4 demultiplexer** (also known as a **1:4 demux**) is a combinational circuit that performs the reverse operation of a multiplexer.

Input: The 1x4 demux has a single input (usually denoted as "I").

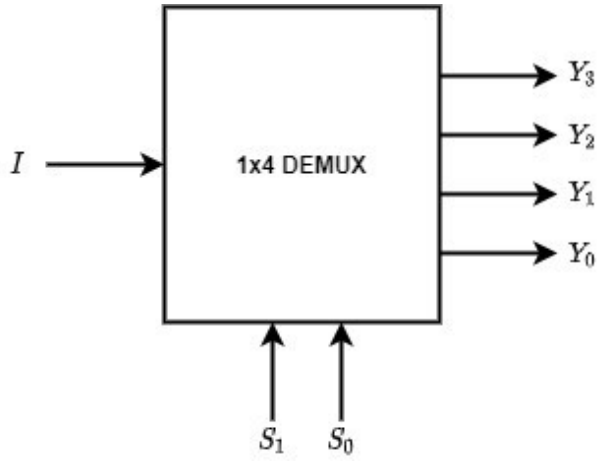
- **Selection Lines**: It has two selection lines (often labeled as "s1" and "s0").
- **Outputs**: There are four outputs (Y3, Y2, Y1, and Y0).

The input signal is routed to one of the four outputs based on the values of the selection lines. Each combination of the selection lines corresponds to a specific output. Here's the truth table for a 1x4 demux:

Truth Table –

sel[0]	sel[1]	y_0	y_1	y_2	y_3
0	0	i	0	0	0
0	1	0	i	0	0
1	0	0	0	i	0
1	1	0	0	0	i

Schematic –



Verilog Code–

design.sv

```
// Code your design here
//1x4 mux
module demux1x4 (a,o0,o1,o2,o3,sel);
  input [3:0]a;
  input [1:0] sel;
  output reg o0,o1,o2,o3;

  always@(*)begin
    case(sel)
      2'b00 : o0=a[0];
      2'b01 : o1=a[1];
      2'b10 : o2=a[2];
      2'b11 : o3=a[3];
    endcase
  end
endmodule
```

Waveform –