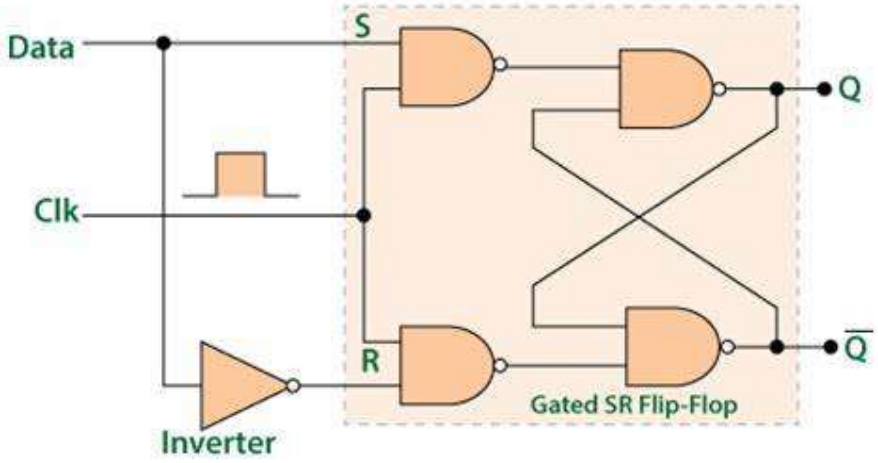
DAY #17

30 DAYS OF VERILOG

AIM – TO IMPLEMENT D FLIP-FLOP

A **D flip-flop**, also known as a **data flip-flop** or **delay flip-flop**, is a fundamental building block in digital electronics.

- **Function**: The D flip-flop stores a single bit of data (either 0 or 1) and has two stable states: the "set" state (Q = 1) and the "reset" state (Q = 0).
- **Inputs**:
  - **D (Data)**: Represents the input data. When the clock signal is high, the flip-flop samples and stores the D input.
  - **Clock (CLK)**: Controls the flip-flop. When the clock input transitions from low to high, the stored D input is reflected at the flip-flop's output (Q).
- **Outputs**:
  - **Q**: Represents the current state of the flip-flop. If D = 0, Q will be 0; if D = 1, Q will be 1.
  - **Q' (Q-bar)**: Complement of Q. If Q = 0, Q' will be 1; if Q = 1, Q' will be 0.



CODE –

```
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module dff(output reg q,qbar, input d,clk,clear);
always @ (posedge clk or negedge clear)
if(clear==1'b0)
begin  q<=1'b0; qbar<=1'b1; end
else
begin q<=d; qbar<=~d; end
endmodule

```

Design Summary (Synthesized) | dff.v | dff_tst.v | dff (RTL1)

WAVEFORM –