DAY #2

30 DAYS OF VERILOG

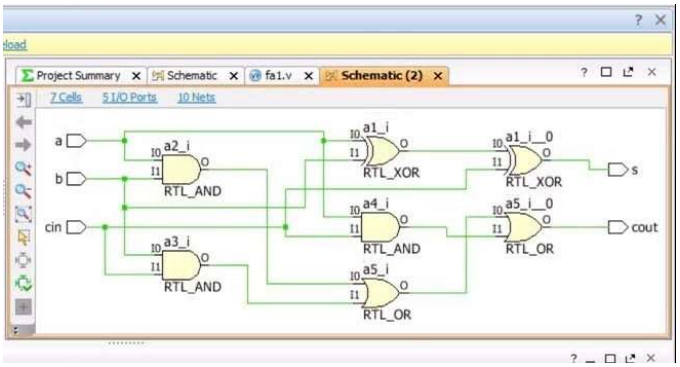
AIM – TO IMPLEMENT FULL ADDER

Full Adder is a digital combinational Circuit which is having three input a, b and cin and two output Sum and Carry. Below Truth Table is drawn to show the functionality of the Full Adder.

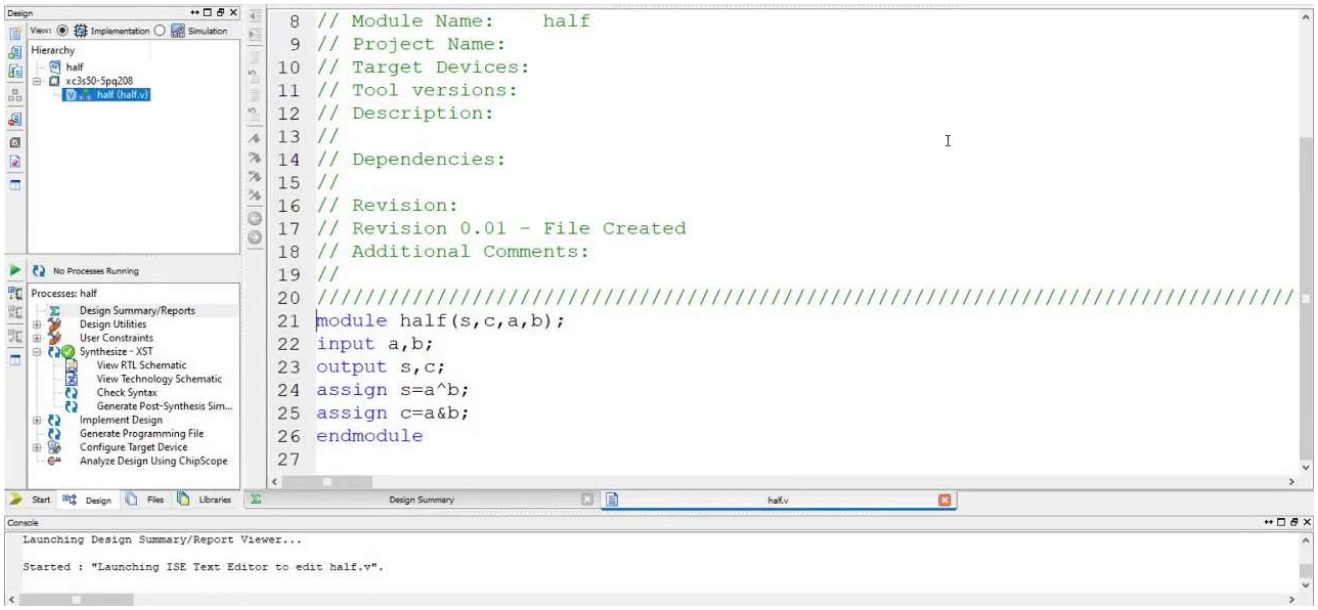
Truth Table –

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Schematic –



Verilog Code–



Waveform –