DAY #3

30 DAYS OF VERILOG

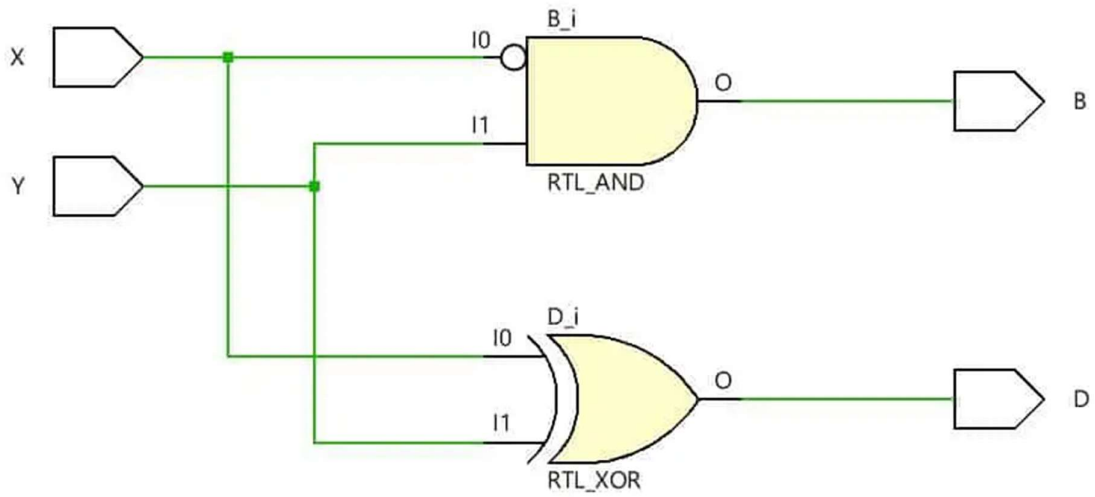
AIM – TO IMPLEMENT HALF SUBTRACTOR

The half subtractor works opposite to the half adder as it substracts two single bits and results in a difference bit and borrow bit as an output.

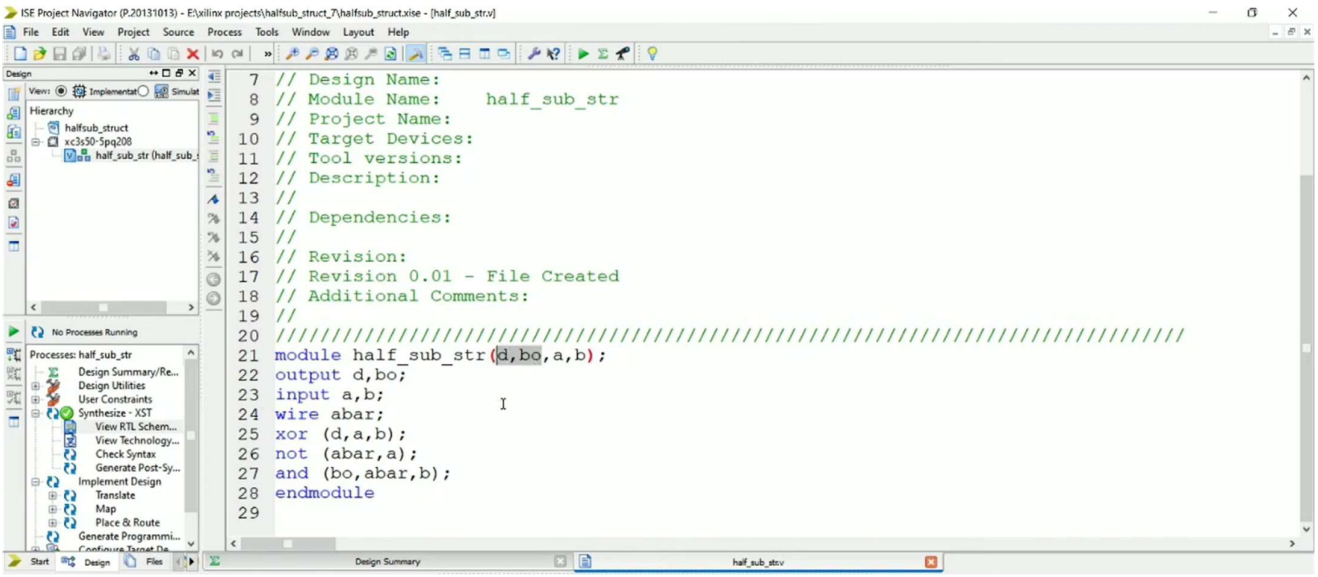
Truth Table –

Inputs		Outputs	
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Schematic –



Verilog Code–



Waveform –