DAY #18

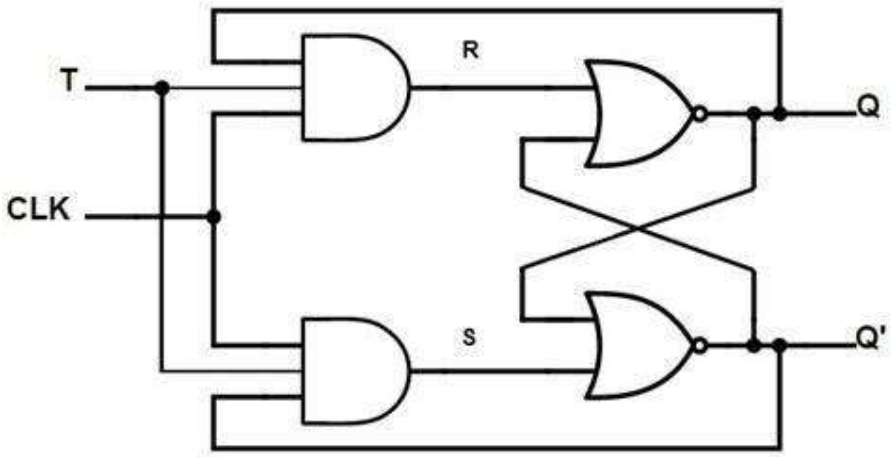
30 DAYS OF VERILOG

AIM – TO IMPLEMENT T FLIP-FLOP

A **T flip-flop**, also known as a **toggle flip-flop**, is a fundamental digital circuit element. Let's break it down:

1. **Purpose**: The T flip-flop can change its output state based on a triggering input. It toggles between two stable states.
2. **Construction**: It's a modified form of the JK flip-flop. Instead of separate J and K inputs, the T flip-flop has a single input called **T**. When the clock signal is high, the T input determines whether the output toggles or remains unchanged.

SCHCEMATIC -



CODE –

```
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21 module tff(output reg q,qbar, input t,clk,clr);
22 always @ (posedge clk)
23 if(clr==1'b1)
24 begin q<=1'b0; qbar<=1'b1; end
25 else if (t==1'b0)
26 begin q<=q; qbar<=qbar; end
27 else
28 begin q<=qbar; qbar<=q; end
29 endmodule
30
```

Design Summary (Synthesized) | tff.v | tff_tst.v

WAVEFORM –