DAY #21

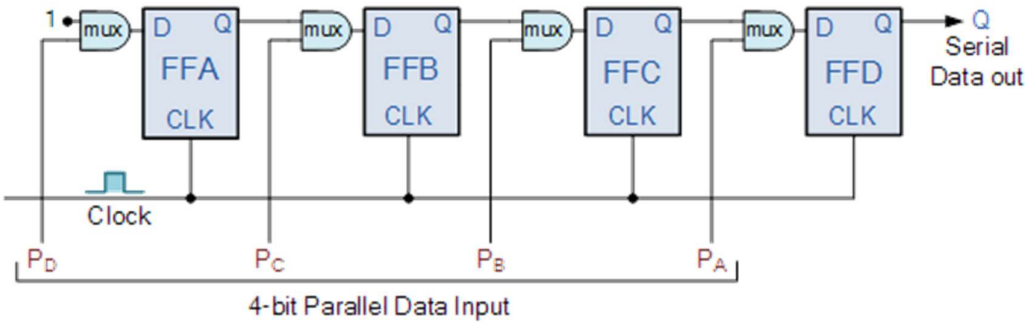
30 DAYS OF VERILOG

AIM – TO IMPLEMENT PISO SHIFT REG.

A **Parallel-In Serial-Out (PISO)** shift register is a digital circuit that accepts parallel input data and produces a sequential output.

1. **Functionality**:
   - A PISO shift register loads data in parallel (through multiple input lines) and outputs it sequentially (bit by bit) in a serial manner.
   - It consists of a chain of flip-flops, with each flip-flop storing one bit of data.
   - Unlike parallel-in/parallel-out (PIPO) shift registers, which offer both parallel input and output, PISO shift registers only accept parallel input and provide serial output.
2. **Terminology**:
   - **Shift Register**: A digital circuit allowing sequential shifting of data bits.
   - **Flip-Flops**: Storage elements within the shift register, each representing a stage through which data passes during shifting.
   - **Parallel Input**: Loading data simultaneously through multiple input lines.
   - **Serial Output**: Sequential output of data in a serial manner.
   - **Clock Signal**: Timing signal controlling the shifting operation.
   - **Most Significant Bit (MSB)**: Leftmost bit in binary representation.
   - **Least Significant Bit (LSB)**: Rightmost bit in binary representation.
3. **Applications**:
   - **Data Transmission**: PISO shift registers convert parallel data into a serial format for efficient transmission over serial communication channels.
   - **Serial-to-Parallel Conversion**: Used to load serial data and output it in parallel, enabling interfacing between serial and parallel systems.

SCHCEMATIC -



CODE –

```
1  `timescale 1ns / 1ps
2
3  module piso(v,clk,sel,clr,d);
4  reg [3:0]q;
5  input [3:0]d;input sel,clk,clr;
6  output reg v;
7  always @ (posedge clk)
8  if(clr==1)
9  q<=4'b0000;
10 else if (sel==0)
11 q<=d;
12 else
13 begin
14 v<=q[0];
15 q<=q>>1;
16 end
17 endmodule
18
```

Design Summary | piso.v | piso_tst.v

WAVEFORM –