DAY #1

30 DAYS OF VERILOG

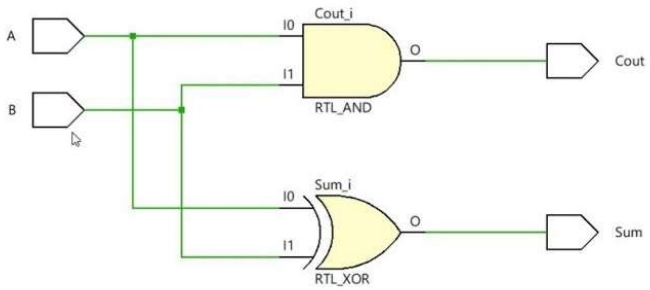
AIM – TO IMPLEMENT HALF ADDER

A half adder is a digital logic circuit that performs binary addition of two single-bit binary numbers. It has two inputs, A and B, and two outputs, SUM and CARRY. In this article we will discuss how to implement a Half adder Using Verilog HDL.

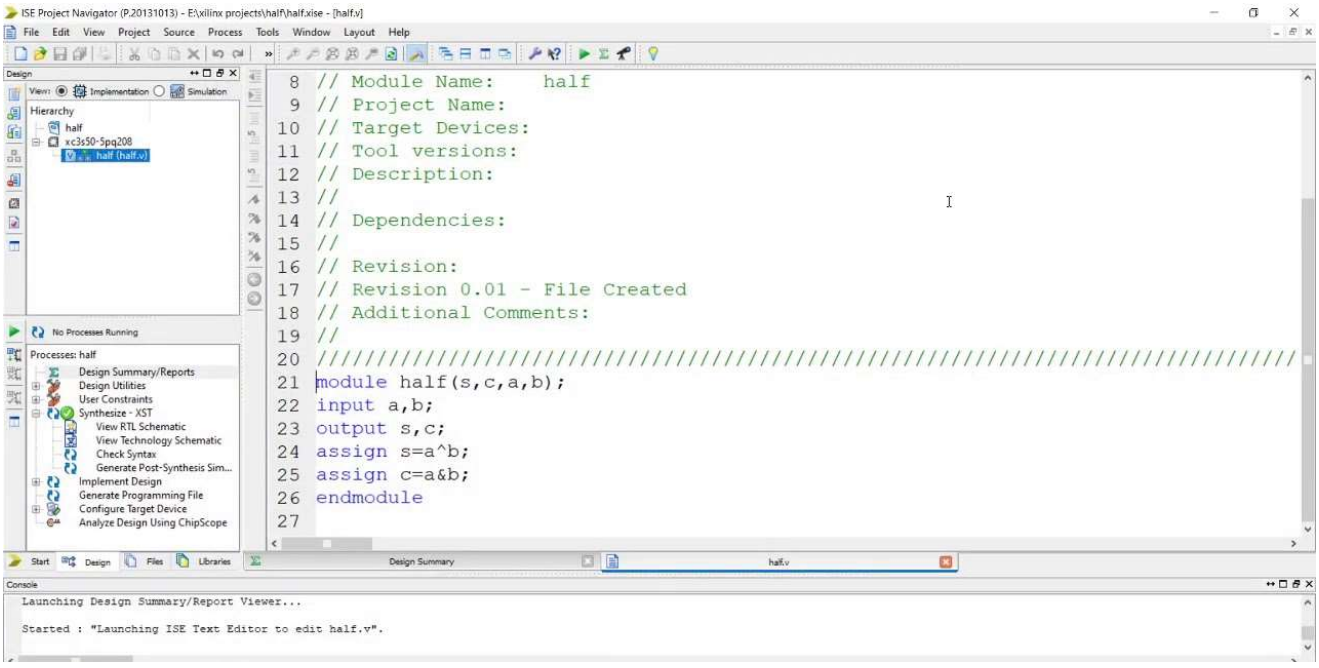
Truth Table –

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Schematic –



Verilog Code–



Waveform –