
DAY #2

30 DAYS OF VERILOG

AIM – TO IMPLEMENT FULL ADDER

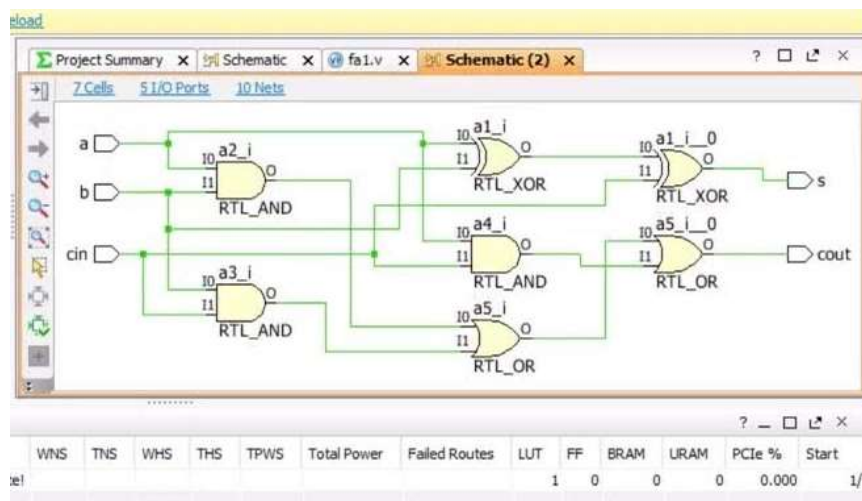
A **full adder** is a combinational logic circuit that adds three binary digits: two input bits (A and B) and a carry bit (Cin). It produces two outputs: a sum bit (S) and a carry-out bit (Cout). Let's break down its components:

1. **Inputs:**
 - **A and B:** The two binary digits to be added.
 - **C-IN:** The carry-in bit from a less significant digit.
2. **Outputs:**
 - **S:** The sum of the two input bits.
 - **C-OUT:** The carry-out bit to a more significant digit.

Truth Table –

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Schematic –



Verilog Code–

```

3 // Company:
4 // Engineer:
5 // Create Date: 06:51:17 10/18/2018
6 // Design Name:
7 // Module Name: Full_Adder
8 // Project Name:
9 // Target Devices:
10 // Tool versions:
11 // Description:
12 // Dependencies:
13 //
14 // Revision:
15 // Revision 0.01 - File Created
16 // Additional Comments:
17 //
18 //
19 //
20 ////////////////////////////////////////////////////////////////////
21 module Full_Adder(
22     input A,
23     input B,
24     input C_in,
25     output C_out,
26     output Sum
27 );
28
29 assign Sum = (C_in ^ (B^A));
30 assign C_out = ((C_in)*(B+A)) + A*B;
31 endmodule
32

```

Waveform –

