DAY #6

30 DAYS OF VERILOG

AIM – TO IMPLEMENT 4X1 MULTIPLEXER

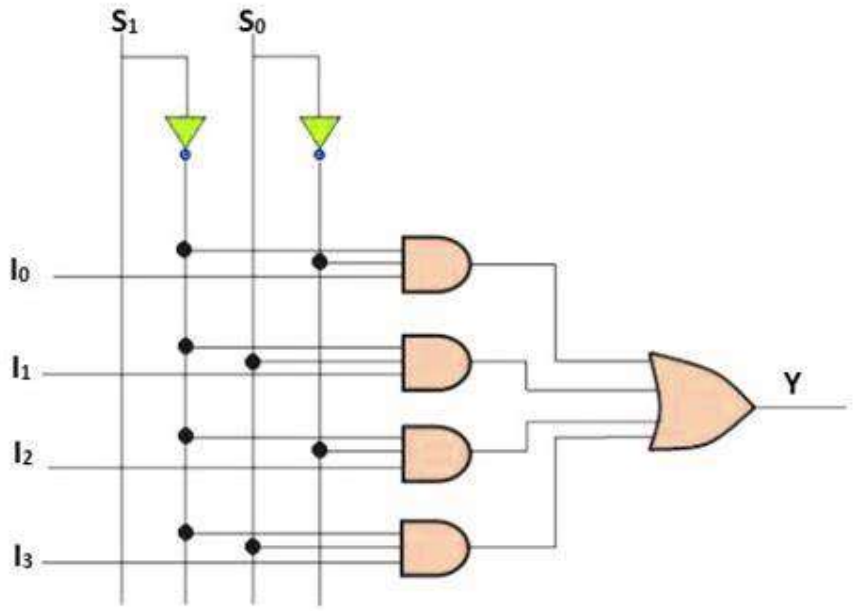
A **4x1 multiplexer** is a digital circuit that selects one of four data inputs and routes it to a single output based on the values of two select lines.

- **Inputs**: The 4x1 multiplexer has four data inputs, labeled as **I0**, **I1**, **I2**, and **I3**.
- **Selection Lines**: It also has two select lines, **S0** and **S1**, which determine which input is connected to the output.
- **Output**: The output is denoted as **Y**.

Truth Table –

INPUTS		Output
S_1	S_0	Y
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

Schematic –



Verilog Code–

```
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module mux4_1(
    input [3:0] i,
    output y,
    input [1:0] s
    );
reg y;
always @ (i,s)
begin
if(s==2'b00)
y<=i[0];
else if(s==2'b01)
y<=i[1];
else if(s==2'b10)
y<=i[2];
else if(s==2'b11)
y<=i[3];
else
y<=1'bZ;
end
```

Waveform –