DAY #11

30 DAYS OF VERILOG

AIM – TO IMPLEMENT 2 Bit COMPARATOR

A **2-bit comparator** is a circuit that compares two 2-bit natural numbers, denoted as A (with bits $A1$ and $A0$) and B (with bits $B1$ and $B0$). The output of the comparator, denoted as S, indicates the relationship between the two numbers:

- If A is greater than B, then $S = 1$.
- Otherwise, if A is less than or equal to B, then $S = 0$.

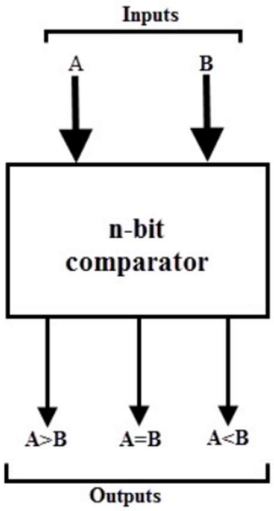
Comparison Process:

- The circuit compares the bits of the two numbers starting from the most significant bit (MSB) and moving toward the least significant bit (LSB).
- At each bit position, the corresponding bits of A and B are compared.
- If the bit in A is greater than the corresponding bit in B, the output $A > B$ is set to 1, indicating that A is greater than B.
- Similarly, if the bit in B is greater than the corresponding bit in A, the output $A < B$ is set to 1, indicating that A is less than B.
- If the two corresponding bits are equal, the circuit moves to the next bit position and compares the next pair of bits.
- This process continues until all the bits have been compared.

Truth table –

A	B	A>B	A<B	A=B
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

BLOCK DIAGRAM –



VERILOG CODE –

```
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module comparator(
    input [1:0] a,b,
    output alb,aeb,agb
    );
   always @(a,b)
   begin
      alb=0; aeb=0; agb=0;
      if(a>b)
         agb=1;
      else if (a==b)
         aeb=1;
      else alb =1;
   end
endmodule
```

halfadder.v | Design Summary (Synthesized) | HATB.v | fulladder.v | FATB.v | comparator.v*

WAVE FORM-