DAY #2

30 DAYS OF VERILOG

AIM – TO IMPLEMENT FULL ADDER

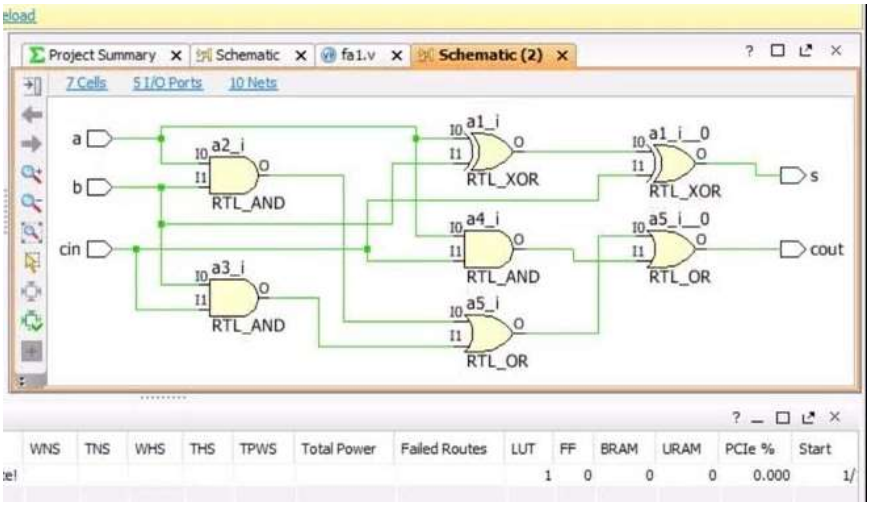
A **full adder** is a combinational logic circuit that adds three binary digits: two input bits (A and B) and a carry bit (Cin). It produces two outputs: a sum bit (S) and a carry-out bit (Cout). Let's break down its components:

1. **Inputs**:
   - **A** and **B**: The two binary digits to be added.
   - **C-IN**: The carry-in bit from a less significant digit.
2. **Outputs**:
   - **S**: The sum of the two input bits.
   - **C-OUT**: The carry-out bit to a more significant digit.

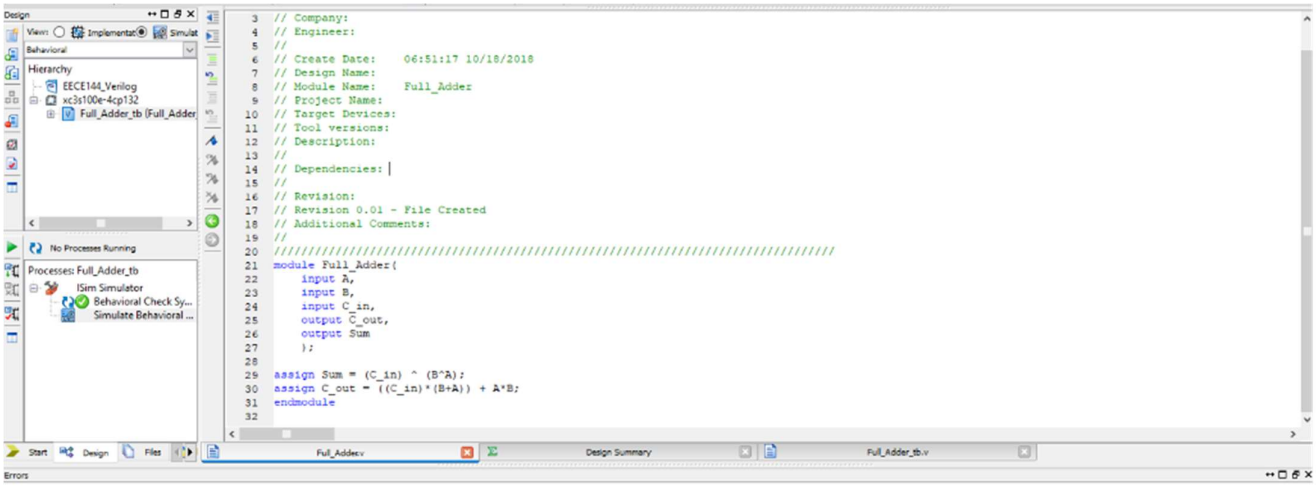
Truth Table –

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Schematic –



Verilog Code–



Waveform –