DAY #4

30 DAYS OF VERILOG

AIM - TO IMPLEMENT FULL SUBTRACTOR

A **full subtractor** is a digital logic circuit that performs the subtraction of two binary numbers. It has three inputs: **A, B,** and **Borrow In (Bin)**, and two outputs: **Difference (D)** and **Borrow Out (Bout)**. Let's break down how it works:

1. Inputs:

o **A**: Minuend bit

B: Subtrahend bit

o **Bin**: Borrow-in bit from the previous stage

2. Outputs:

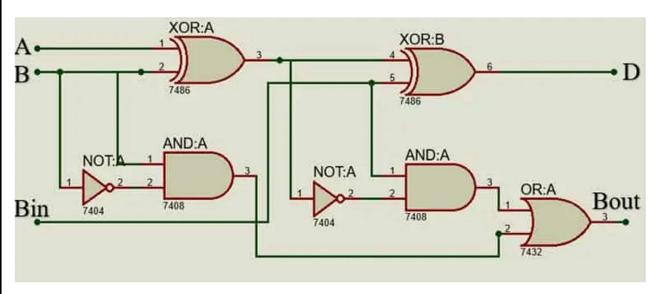
o **Diff**: Difference bit

o **Bout**: Borrow-out bit for the next stage

Truth Table -

	Input		Output	
Α	В	С	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Schematic -



Verilog Code-

```
ISE Project Navigator (P.20131013) - E:\xillinx projects\full_sub_df_11\full_sub_df_11.xise - [full_sub_df.v]
Bifle Edit View Project Source Process Tools Window Layout Help

| Project Name:
| Project Na
Hearth with the full sub_df (full sub_df)

| 10 // Talget be.
| 10 // Talget be.
| 11 // Tool versions:
| 12 // Description:
| 13 //
                                                                                     13 //
   % 14 // Dependencies:
                                                                                     * 15 //
                                                                                               16 // Revision:
           17 // Revision 0.01 - File Created
                                                                                               18 // Additional Comments:
   No Processes Running
                                                                                               19 //
  Processes: full_sub_df
 Processes full sub, df

Design Summary/Reports
Design Utilities
User Constraints
View RTL Schematic
View REchnology Sc...
Check Syntax
Generate Porgramming ...
Generate Programming ...
Configure Target Device
Analyze Design Using C...
                                                                                               21 module full sub df(output d,bo,input a,b,bi);
                                                                                                22 assign d=a^b^bi;
                                                                                                23 assign bo=((~a)&b)|(~(a^b)&bi);
                                                                                                24 endmodule
                                                                                               25
 Design Summary
                                                                                                                                                                                                                                     full_sub_df.v
```

Waveform -

