



NPTEL Online Certification

(Funded by the MoE, Govt. of India)



This certificate is awarded to

RAJ KAUSHAL YADAV

for successfully completing the course

Digital Design with Verilog

with a consolidated score of **55** %

Online Assignments	19.16/25	Proctored Exam	36/75
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Total number of candidates certified in this course: **1068**

Jan-Apr 2024

(12 week course)

Prof. T. V. Bharat

Head, Centre for Educational Technology
NPTEL Coordinator, IIT Guwahati



Indian Institute of Technology Guwahati

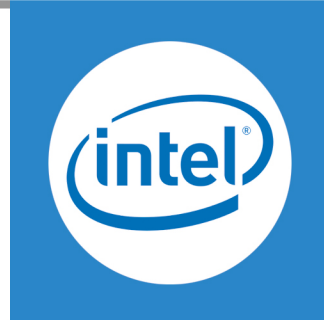


Roll No: NPTEL24CS61S652100048

To verify the certificate



No. of credits recommended: 3 or 4



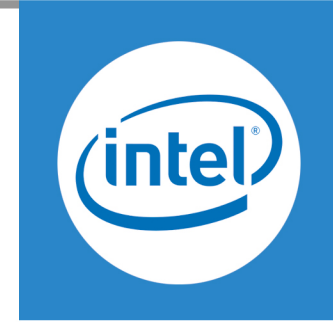
Verilog HDL Basics Course Completion

ISSUED TO

Raj Kaushal Yadav



Issued on: 10 APR 2024 | Issued by Intel
Verify: <https://www.credly.com/go/G2P2CJXc>



Beginner Workshop for Intel® FPGAs Course Completion

ISSUED TO

Raj Kaushal Yadav



Issued on: 25 APR 2024 | Issued by Intel
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