RAJ KAUSHAL YADAV

Vill. Kaserua khurd, Prayagraj, Uttar Pradesh 221507

(+91) 6393075461 | raj875.yadav@gmail.com | http://www.linkedin.com/in/raaj875a

CAREER OBJECTIVE

My goal is to become associated with a company where I can utilize my skills and gain further experience while enhancing the company's productivity and reputation.

EDUCATION

M.J.P. Rohilkhand University, Bareilly (U.P) — December 2021 – Present

Bachelor of Technology — Overall CGPA: 7.25

Department of Electronics and Communication Engineering

Bishop George School & College, Prayagraj (U.P) — July 2016 – April 2020

Intermediate — Overall Percentage: 68%

Physics, Chemistry, Mathematics

TECHNICAL STRENGTH

CAD Tools: Xilinx ISE, ModelSim
Languages: Verilog, C++
Operating System: Linux, Windows

PROJECT WORKED

Design and Verification of a Pipelined FIFO Buffer Using Verilog — September 2024 - Present

B.Tech - Final Project

M.J.P. Rohilkhand University, Bareilly (U.P)

This project aims to design a pipelined FIFO (First-In-First-Out) buffer using Verilog and verify its functionality and performance.

RELEVANT COURSES

NPTEL - Digital System Design using Verilog — https://bit.ly/47FgaGm

NPTEL - VLSI Design Flow: RTL to GDS — ongoing

AREA OF INTEREST

- Digital Electronics - VLSI Design