ICC2 : CTS Automated Script

Tool : Synopsys IC Compiler II (ICC2)

Stage : CTS

Date : 27-01-2025

```
##########################################################################
# CTS SPEC FILE
##########################################################################
puts "INFO: Sourcing CTS specification..."
# ------------------------------------------------------------
# Pre-CTS sanity checks
# ------------------------------------------------------------
check_clock_trees
check_design -checks pre_clock_tree_stage
# ------------------------------------------------------------
# Derive existing clock cell references
# ------------------------------------------------------------
derive_clock_cell_references -output ./scripts/ref_cell.tcl
# ------------------------------------------------------------
# Clock cell control
# ------------------------------------------------------------
# Exclude all cells from CTS
set_lib_cell_purpose -exclude cts [get_lib_cells]
# Source derived reference cells
source ./scripts/ref_cell.tcl
# Allow only selected CTS cells (LVT/RVT buffers & inverters)
set_lib_cell_purpose -include cts \
  [get_lib_cells -filter \
    "ref_name =~ *BUF*LVT* || ref_name =~ *BUF*RVT* || \
     ref_name =~ *INV*LVT* || ref_name =~ *INV*RVT*"]
```

```
# ------------------------------------------------------------
# Clock routing rules (NDR – double width & spacing)
# ------------------------------------------------------------
remove_routing_rules -all
create_routing_rule icc_clock_double_spacing \
   -default_reference_rule \
   -multiplier_spacing 2 \
   -taper_distance 0.4 \
   -driver_taper_distance 0.4
set_clock_routing_rules \
   -net_type sink \
   -rules icc_clock_double_spacing \
   -min_routing_layer M4 \
   -max_routing_layer M5
# ------------------------------------------------------------
# CTS constraints
# ------------------------------------------------------------
current_mode func
set_max_transition 0.15 \
   -clock_path [get_clocks] \
   -corners [all_corners]
# ------------------------------------------------------------
# Target skew (corner-based)
# ------------------------------------------------------------
set_clock_tree_options -clock_tree [get_clocks] \
   -target_skew 0.05 \
   -corners [get_corners ss_125c]
set_clock_tree_options -clock_tree [get_clocks] \
   -target_skew 0.02 \
   -corners [get_corners ff_m40c]
```

```
# ----------------------------------------------------------
# Clock uncertainty (scenario-aware)
# ----------------------------------------------------------
foreach_in_collection scen [all_scenarios] {
   current_scenario $scen
   set_clock_uncertainty 0.10 -setup [all_clocks]
   set_clock_uncertainty 0.05 -hold  [all_clocks]
}
# ----------------------------------------------------------
# Enable CRPR
# ----------------------------------------------------------
set_app_options \
   -name time.remove_clock_reconvergence_pessimism \
   -value true
# ----------------------------------------------------------
# CTS balance points (example – design Exceptions)
# ----------------------------------------------------------
foreach_in_collection mode [all_modes] {
   current_mode $mode
   set_clock_balance_points \
      -consider_for_balancing true \
      -balance_points [get_pins "I_SDRAM_TOP/I_SDRAM_IF/sd_mux_*/SO"]
}
# ----------------------------------------------------------
# Hold fixing cell control
# ----------------------------------------------------------
set_lib_cell_purpose -exclude hold [get_lib_cells]
set_lib_cell_purpose -include hold \
   [get_lib_cells -filter \
      "ref_name =~ *DEL*HVT* || ref_name =~ *BUF*HVT*"]


puts "INFO: CTS specification completed."
```

```
##########################################################################
# CTS RUN SCRIPT
# This script is executed AFTER sourcing cts_spec.tcl
##########################################################################
puts "================ CTS FLOW STARTED ================"
#-----------------------------------------------
# Set prefixes for CTS and data path cells
#-----------------------------------------------
puts "INFO: Setting instance name prefixes..."
# Prefix for CTS-added cells
set_app_options -name opt.common.user_instance_name_prefix -value clock_opt_clock_
# Prefix for data-path optimization cells
set_app_options -name opt.common.user_instance_name_prefix \
-value clock_opt_data_
#-----------------------------------------------
# 3. Remove existing global routes
#-----------------------------------------------
puts "INFO: Removing existing global routes..."
remove_routes -global_route
#-----------------------------------------------
# 4. Build Clock Tree (CTS build phase)
#-----------------------------------------------
puts "INFO: Building clock tree..."
clock_opt -to build_clock
save_block -as build_clock_done
#-----------------------------------------------
# 5. Route Clock Tree
#-----------------------------------------------
puts "INFO: Routing clock tree..."
clock_opt -from build_clock -to route_clock
save_block -as route_clock_done
```

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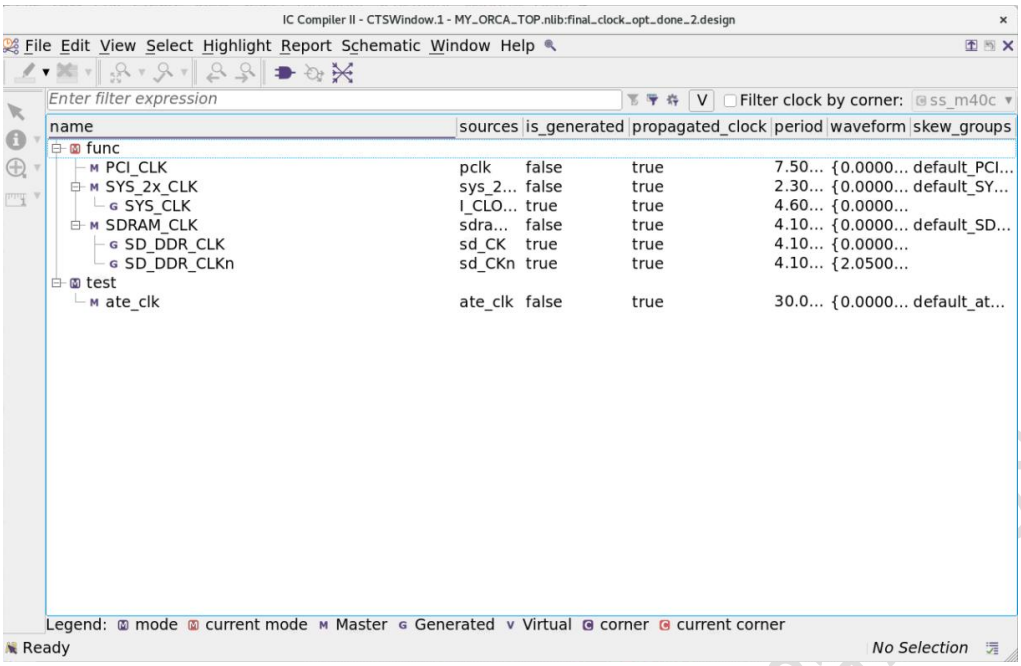
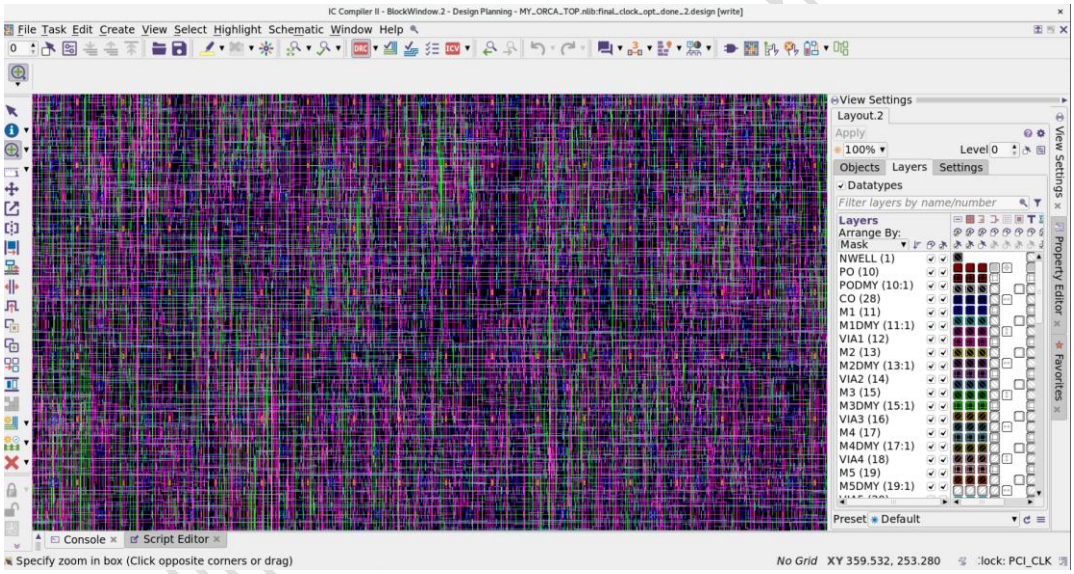
#-----------------------------------------------
# 6. Post-CTS timing check
#-----------------------------------------------
puts "INFO: Reporting post-CTS timing..."
file mkdir ./reports/cts
report_global_timing > ./reports/cts/cts_global_timing.rpt
#-----------------------------------------------
# 7. Enable aggressive hold fixing options
#-----------------------------------------------
puts "INFO: Enabling hold-fix optimization options..."
set_app_options -name clock_opt.hold.effort -value high
set_app_options -name ccd.hold_control_effort -value high
set_app_options -name opt.dft.clock_aware_scan_reorder -value true
#-----------------------------------------------
# 8. Final CTS optimization (skew + hold cleanup)
#-----------------------------------------------
puts "INFO: Running final CTS optimization..."
clock_opt
save_block -as final_clock_opt_done
puts "================ CTS FLOW COMPLETED ================"
##########################################################################
# CTS REPORT DUMP
##########################################################################
set rpt_dir ./reports/cts_qor
# Create directory if it does not exist
if {![file exists $rpt_dir]} {
   file mkdir $rpt_dir
}
puts "INFO: Dumping CTS reports into $rpt_dir"
#-----------------------------------------------
# Global Timing
#-----------------------------------------------
```

```
report_global_timing > $rpt_dir/global_timing.rpt
#--------------------------------------------
# Clock Latency Reports
#--------------------------------------------
report_clock_qor -type latency \
  -scenarios func_ff_125c \
  -nosplit > $rpt_dir/clock_latency_func_ff_125c.rpt
report_clock_qor -type latency \
  -scenarios func_ss_m40c \
  -nosplit > $rpt_dir/clock_latency_func_ss_m40c.rpt
#--------------------------------------------
# Clock DRC Violations
#--------------------------------------------
report_clock_qor -type drc_violators \
  > $rpt_dir/clock_drc_violators.rpt
#--------------------------------------------
# Minimum Pulse Width Violations
#--------------------------------------------
report_min_pulse_width -all_violators \
  > $rpt_dir/min_pulse_width_violations.rpt
#--------------------------------------------
# Max Transition Violations
#--------------------------------------------
report_constraints -all_violators -max_transition \
  > $rpt_dir/max_transition_violations.rpt
#--------------------------------------------
# Max Capacitance Violations
#--------------------------------------------
report_constraints -all_violators -max_capacitance \
  > $rpt_dir/max_capacitance_violations.rpt
puts "INFO: CTS report dumping completed"
```

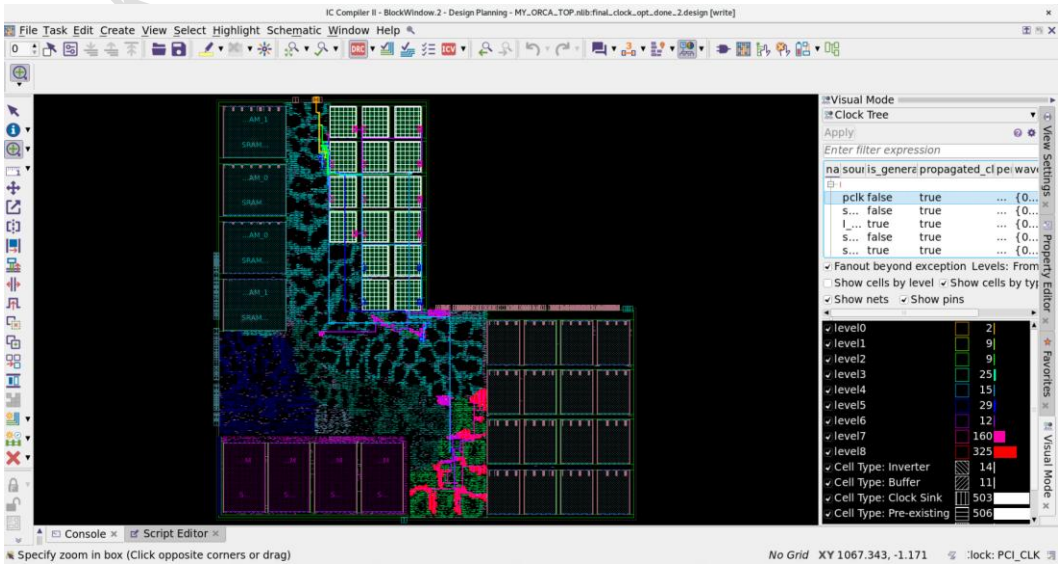
CTS Clock Window Overview

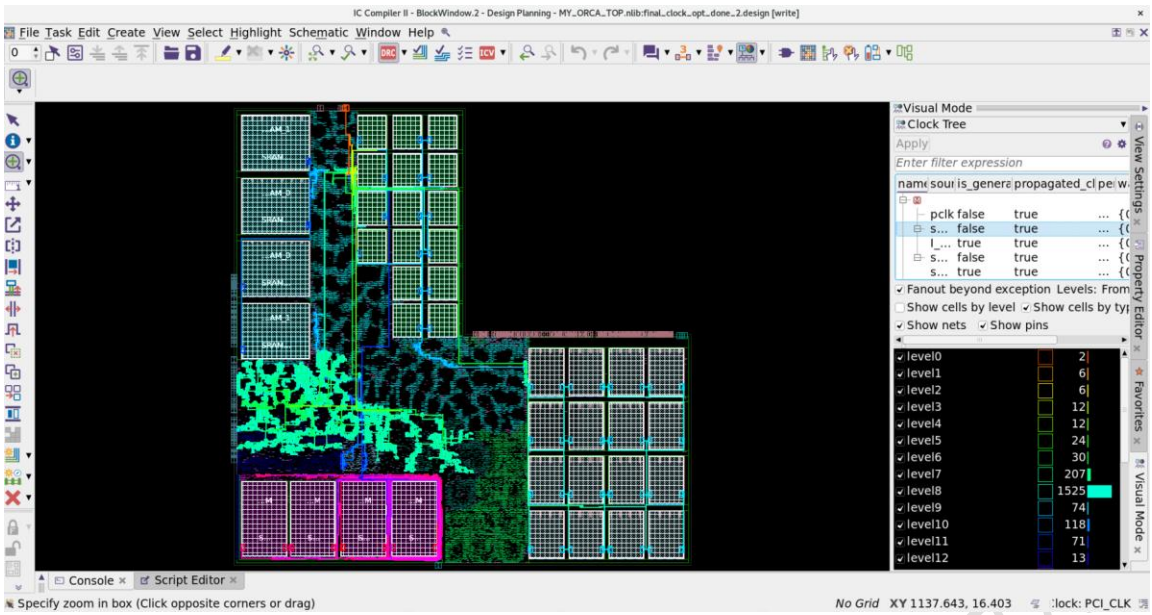


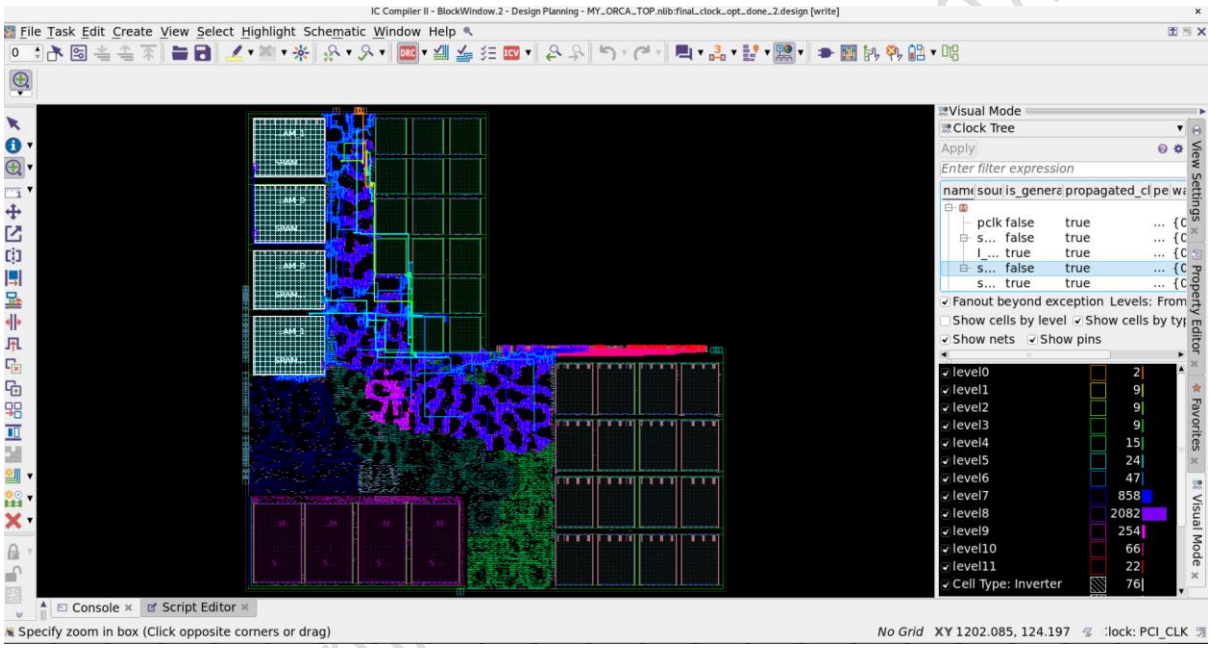
Clock path routed

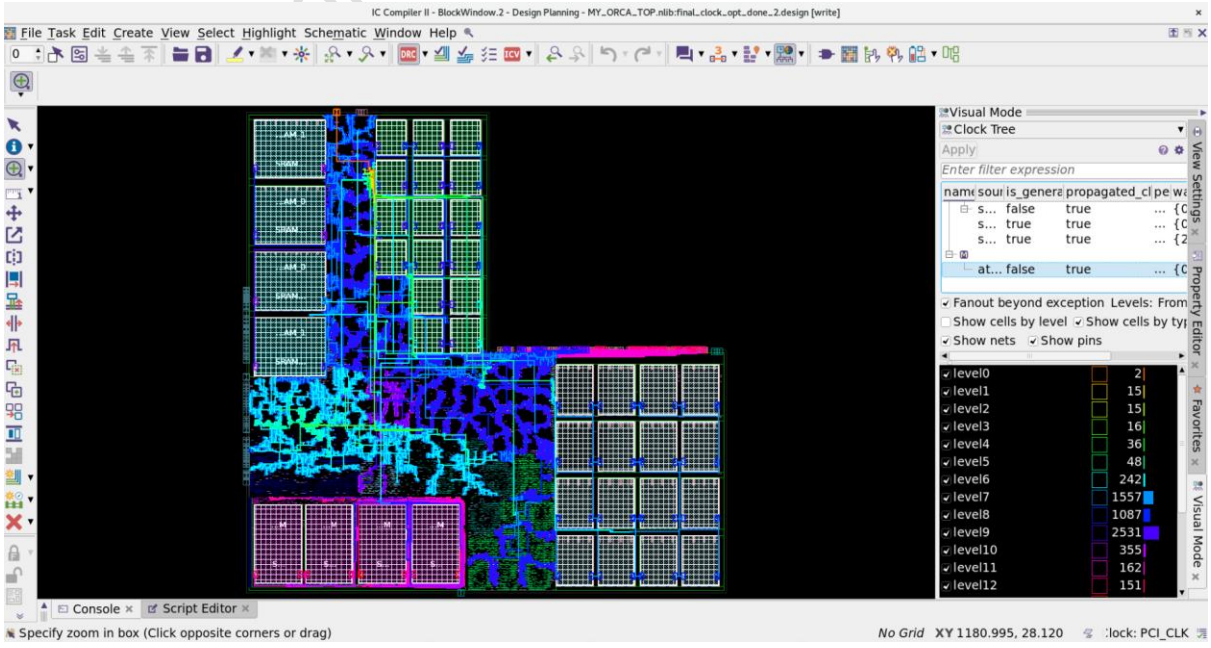


CLOCK_TREE

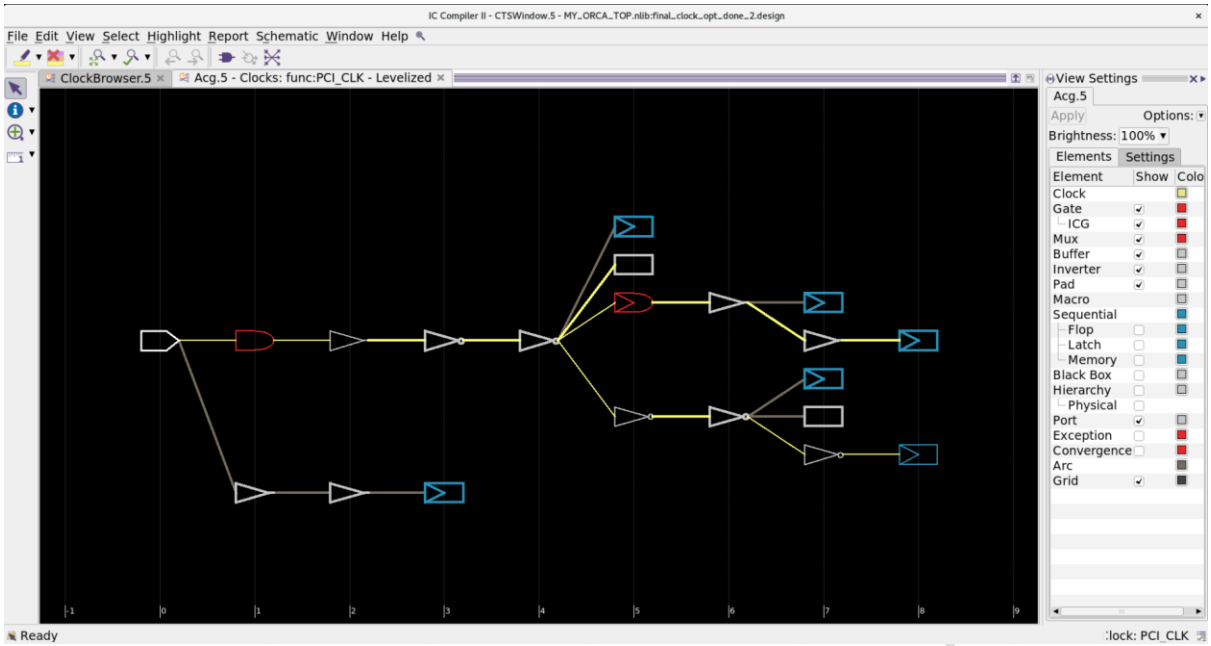


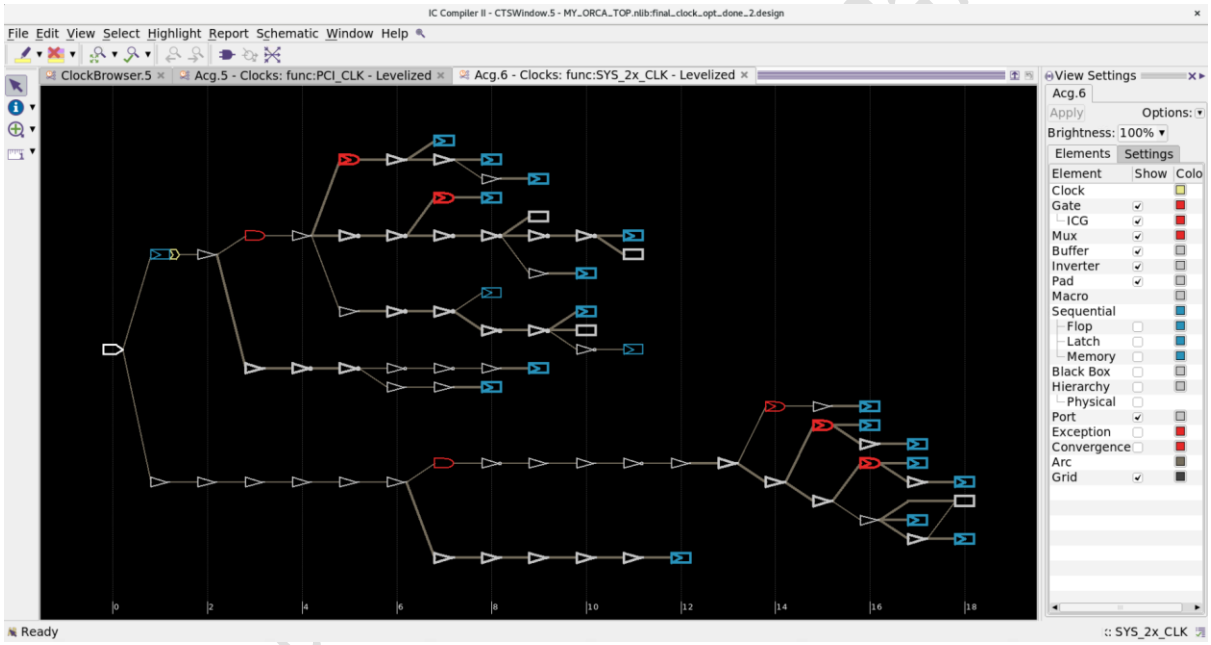

IC Compiler II - BlockWindow.2 - Design Planning - MY_ORCA_TOP.nlib:final_clock_opt_done_2.design [write]
File Task Edit Create View Select Highlight Schematic Window Help
Visual Mode
Clock Tree
Apply
Enter filter expression
Fanout beyond exception Levels: From
Show cells by level Show cells by ty
Show nets Show pins
level0 2
level1 6
level2 6
level3 12
level4 12
level5 24
level6 30
level7 207
level8 1525
level9 74
level10 118
level11 71
level12 13
Console
Script Editor
Specify zoom in box (Click opposite corners or drag)
No Grid XY 1137.643, 16.403
:lock: PCI_CLK

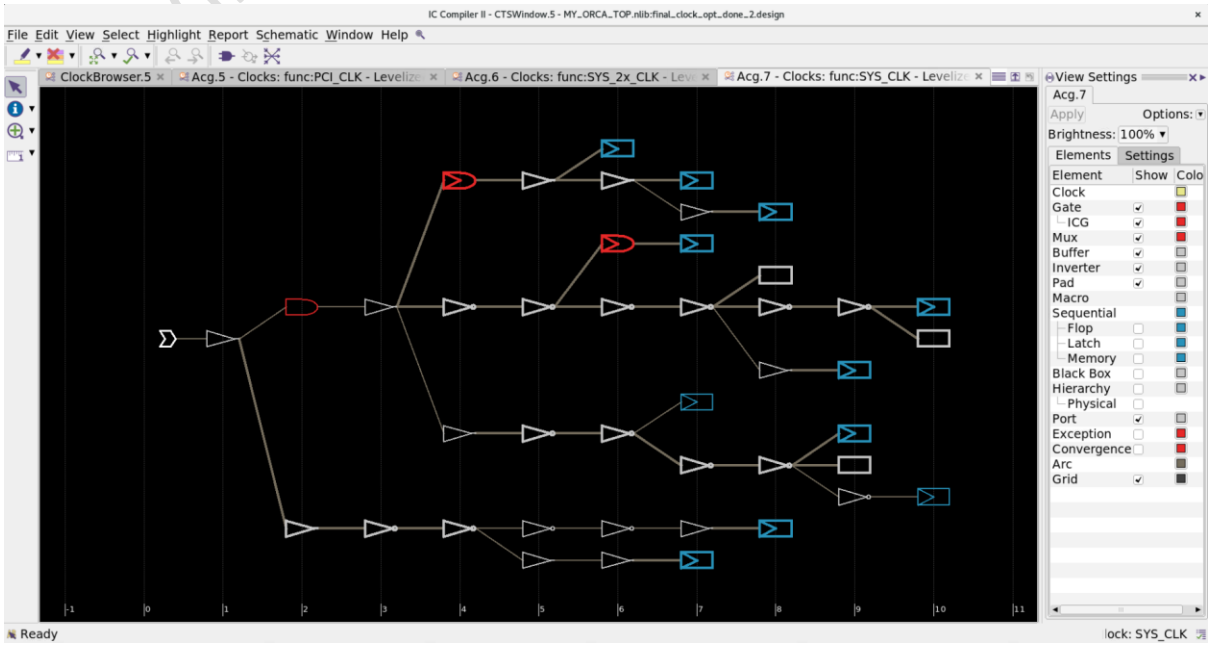

IC Compiler II - BlockWindow.2 - Design Planning - MY_ORCA_TOP.nlib:final_clock_opt_done_2.design [write]
File Task Edit Create View Select Highlight Schematic Window Help
Visual Mode
Clock Tree
Apply
Enter filter expression
Fanout beyond exception Levels: From
Show cells by level Show cells by ty
Show nets Show pins
level0 2
level1 9
level2 9
level3 9
level4 15
level5 24
level6 47
level7 858
level8 2082
level9 254
level10 66
level11 22
Cell Type: Inverter 76
Console
Script Editor
Specify zoom in box (Click opposite corners or drag)
No Grid XY 1202.085, 124.197
:lock: PCI_CLK

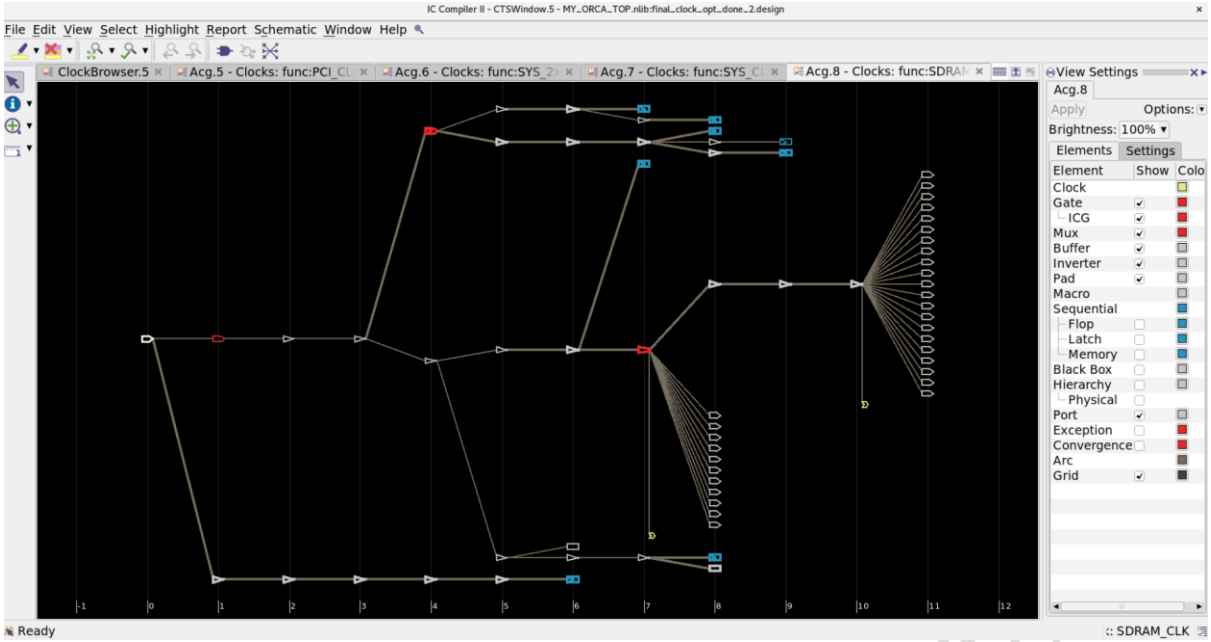

IC Compiler II - BlockWindow.2 - Design Planning - MY_ORCA_TOP.nlib:final_clock_opt_done_2.design [write]
File Task Edit Create View Select Highlight Schematic Window Help
Visual Mode
Clock Tree
Apply
Enter filter expression
Fanout beyond exception Levels: From
Show cells by level Show cells by ty
Show nets Show pins
level0 2
level1 15
level2 15
level3 16
level4 36
level5 48
level6 242
level7 1557
level8 1087
level9 2531
level10 355
level11 162
level12 151
Console
Script Editor
Specify zoom in box (Click opposite corners or drag)
No Grid XY 1180.995, 28.120
:lock: PCI_CLK

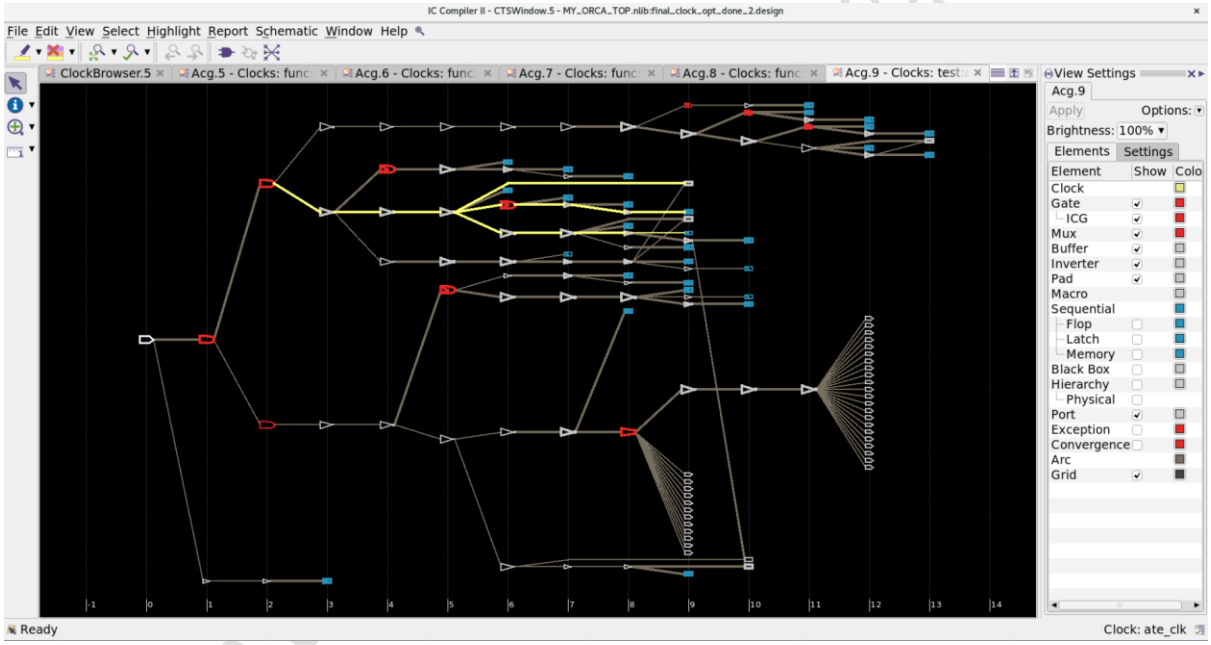
WE CAN VIEW THE LATENCY








IC Compiler II - CTSWindow.5 - MY_ORCA_TOP.nlib:final_clock_opt_done_2.design
File Edit View Select Highlight Report Schematic Window Help
ClockBrowser.5
Acg.5 - Clocks: func:PCI_CL
Acg.6 - Clocks: func:SYS_2
Acg.7 - Clocks: func:SYS_CL
Acg.8 - Clocks: func:SDRAM
View Settings
Acg.8
Apply
Options:
Brightness: 100%
Elements
Settings
Element
Show
Colo
Clock
Gate
ICG
Mux
Buffer
Inverter
Pad
Macro
Sequential
Flop
Latch
Memory
Black Box
Hierarchy
Physical
Port
Exception
Convergence
Arc
Grid
-1
0
1
2
3
4
5
6
7
8
9
10
11
12
Ready
:: SDRAM_CLK


IC Compiler II - CTSWindow.5 - MY_ORCA_TOP.nlib:final_clock_opt_done_2.design
File Edit View Select Highlight Report Schematic Window Help
ClockBrowser.5
Acg.5 - Clocks: func
Acg.6 - Clocks: func
Acg.7 - Clocks: func
Acg.8 - Clocks: func
Acg.9 - Clocks: test
View Settings
Acg.9
Apply
Options:
Brightness: 100%
Elements
Settings
Element
Show
Colo
Clock
Gate
ICG
Mux
Buffer
Inverter
Pad
Macro
Sequential
Flop
Latch
Memory
Black Box
Hierarchy
Physical
Port
Exception
Convergence
Arc
Grid
-1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
Ready
Clock: ate_clk