```
# ICC2  : ROUTING Automated Script
# Tool    : Synopsys IC Compiler II (ICC2)
# Stage  : ROUTING
# Date    : 28-01-2026
##############################################################################
# ROUTING STAGE
##############################################################################
puts "INFO: Routing stage started..."
#--------------------------------------------------
# Pre-routing checks
#--------------------------------------------------
set rpt_dir "./reports/pre_route_checks"
#--------------------------------------------------
# Create report directory automatically
#--------------------------------------------------
if {![file exists $rpt_dir]} {
   file mkdir $rpt_dir
   puts "INFO: Created report directory $rpt_dir"
} else {
   puts "INFO: Using existing report directory $rpt_dir"
}
#--------------------------------------------------
# Routability check
#--------------------------------------------------
puts "INFO: Running check_routability..."
check_routability > $rpt_dir/routability.rpt
#--------------------------------------------------
# Pre-route design checks
#--------------------------------------------------
puts "INFO: Running pre-route design checks..."
check_design -check pre_route_stage > $rpt_dir/pre_route_design_check.rpt
```

```
puts "INFO: Pre-route checks completed successfully"

#--------------------------------------------------

# Enable timing-driven routing

#--------------------------------------------------

set_app_options -name route.global.timing_driven  -value true

set_app_options -name route.track.timing_driven   -value true

set_app_options -name route.detail.timing_driven  -value true

#--------------------------------------------------

# Enable crosstalk-aware routing

#--------------------------------------------------

set_app_options -name route.global.crosstalk_driven -value true

set_app_options -name route.track.crosstalk_driven  -value true

#--------------------------------------------------

# Timing analysis options

#--------------------------------------------------

set_app_options -name time.si_enable_analysis       -value true

set_app_options -name time.si_xtalk_composite_aggr_mode -value statistical

set_app_options -name time.all_clocks_propagated      -value true


#--------------------------------------------------

# Improve DRC convergence

#--------------------------------------------------

set_app_options -name route.detail.eco_max_number_of_iterations -value 20

set_app_options -name route.detail.drc_convergence_effort_level -value high

set_app_options -name route.detail.force_max_number_iterations  -value true

#--------------------------------------------------

# Prefix for routing-added cells

#--------------------------------------------------

set_app_options -name opt.common.user_instance_name_prefix -value route_opt_

#--------------------------------------------------

# Read antenna rules

#--------------------------------------------------
```

```
Source /home/vlsiguru/PHYSICAL_DESIGN/TRAINER1/ICC2/ORCA_TOP/ref/tech/saed32nm_ant_1p9m.tcl
#-------------------------------------------------
# Perform routing
#   1) Global routing
#   2) Track assignment
#   3) Detail routing
#-------------------------------------------------
route_auto \
   -save_after_global_route true \
   -save_after_track_assignment true \
   -save_after_detail_route true
#-------------------------------------------------
# Routing optimization
#-------------------------------------------------
route_opt
#-------------------------------------------------
# Save block
#-------------------------------------------------
save_block -as route_opt_done
puts "INFO: Routing stage completed successfully"
################################################################################
# POST ROUTING CHECKS
################################################################################
set rpt_dir "./reports/post_route_checks"
#-------------------------------------------------
# Create directory automatically
#-------------------------------------------------
if {![file exists $rpt_dir]} {
   file mkdir $rpt_dir
   puts "INFO: Created report directory $rpt_dir"
} else {
  puts "INFO: Report directory already exists: $rpt_dir"
}
#--------------------------------------------------
# Power / Ground checks
#--------------------------------------------------
puts "INFO: Running PG connectivity check..."
check_pg_connectivity  > $rpt_dir/pg_connectivity.rpt
puts "INFO: Running PG missing vias check..."
check_pg_missing_vias  > $rpt_dir/pg_missing_vias.rpt
puts "INFO: Running PG DRC check..."
check_pg_drc > $rpt_dir/pg_drc.rpt
#--------------------------------------------------
# Routing checks
#--------------------------------------------------
puts "INFO: Running routing check..."
check_routes > $rpt_dir/route_check.rpt
#--------------------------------------------------
# LVS check
#--------------------------------------------------
puts "INFO: Running LVS check..."
check_lvs -max_error 0 > $rpt_dir/lvs.rpt
puts "INFO: All post-routing checks completed successfully"
```

DRC and LVS Checks

Objective

Design Rule Check (DRC) and Layout Versus Schematic (LVS) checks are performed to ensure physical correctness, power integrity, and logical consistency of the layout before signoff.

DRC Violations

Common Metal DRC Types

- Shorts between metal shapes
- Same-net spacing violations
- Different-net spacing violations
- Minimum metal width violations
- Minimum metal area violations
- Fat contact (via enclosure) violations
- Routing on restricted layers over macros

LVS Violations

- Shorted nets where two different nets are unintentionally connected.
- Open nets where connectivity is broken in layout.

- **Manual Debug and Fix – GUI Shortcuts**

These shortcuts are used to manually fix DRC and routing issues in the layout editor.

- **Select Shape**

Used to select metal shapes or vias for editing.

- **Stretching Metal Shape**

Extends or reduces the length of a metal shape.

Shortcut:

s

Used to fix spacing violations or improve connectivity.

- **Delete Shape or Via**

Removes unwanted metal shapes or vias.

Shortcut: first select the object and press

d

Used to fix shorts or remove incorrect routing.

- **Create Via on Specific Metal Layer**

Creates a via between metal layers.

Shortcut:

Shift + c

Used to fix missing via violations and improve connectivity.

- **Cut Metal Layer**

Cuts or breaks a metal shape at a desired location.

Shortcut:

Shift + l

Used to resolve shorts or reroute metal segments.

- **Manual Routing Mode**

Enables manual routing for selected nets.

Shortcut:

Shift + r

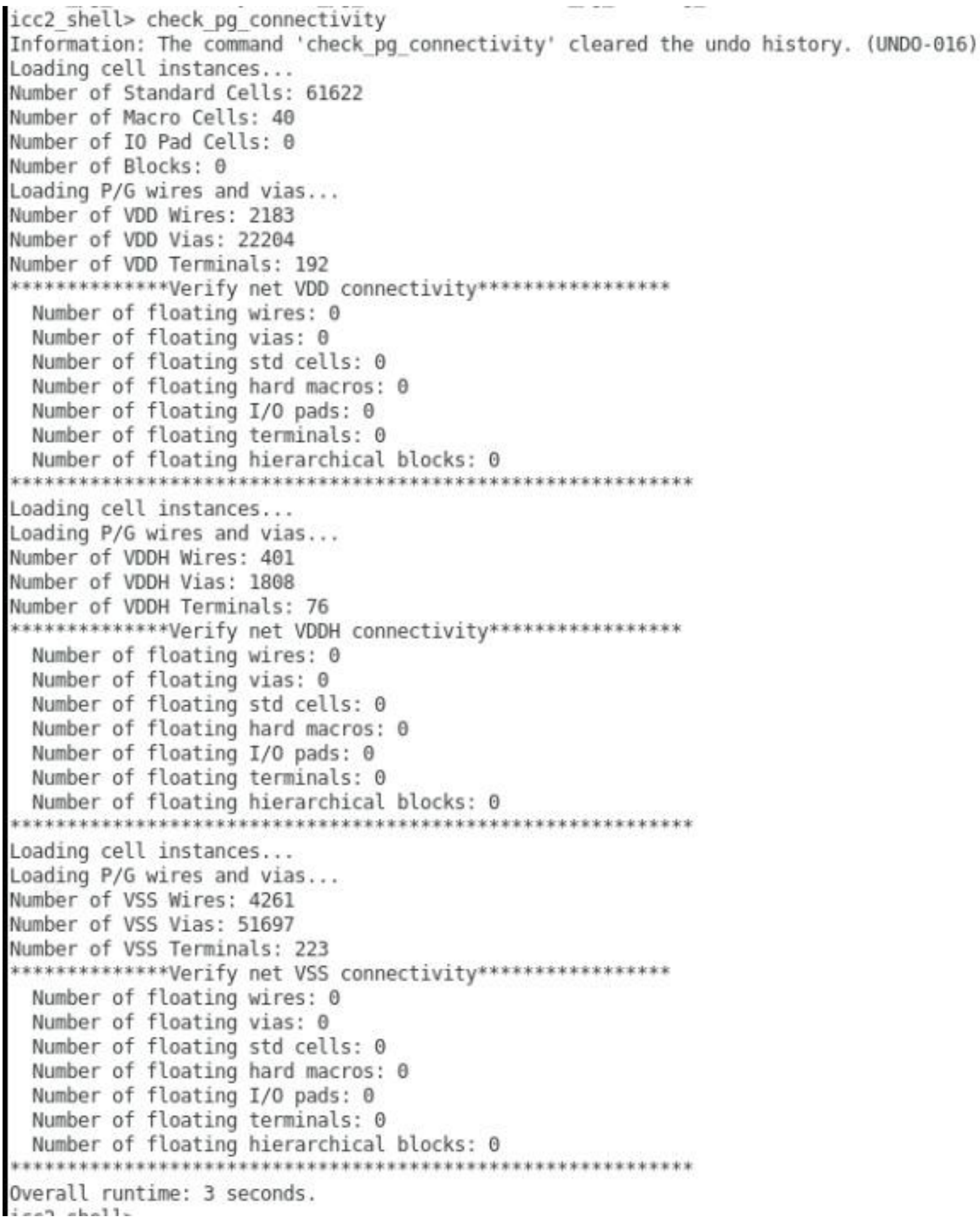
Used when automatic routing cannot fix specific violations.

DRC Checks

- DRC checks verify that the layout meets routing, connectivity, and manufacturing rules.

Power and Ground Connectivity Check

check_pg_connectivity

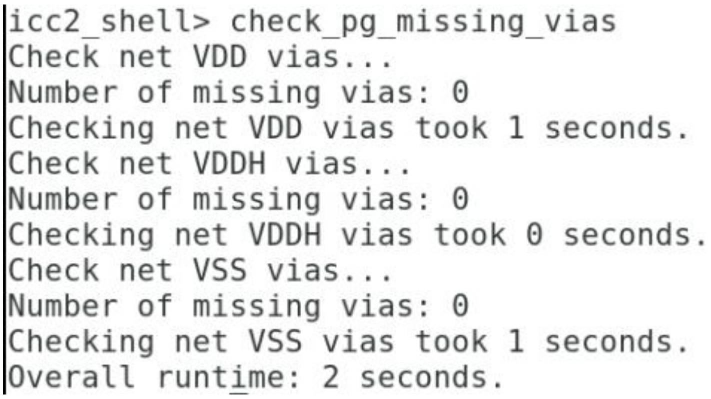


```
icc2_shell> check_pg_connectivity
Information: The command 'check_pg_connectivity' cleared the undo history. (UNDO-016)
Loading cell instances...
Number of Standard Cells: 61622
Number of Macro Cells: 40
Number of IO Pad Cells: 0
Number of Blocks: 0
Loading P/G wires and vias...
Number of VDD Wires: 2183
Number of VDD Vias: 22204
Number of VDD Terminals: 192
**************Verify net VDD connectivity****************
  Number of floating wires: 0
  Number of floating vias: 0
  Number of floating std cells: 0
  Number of floating hard macros: 0
  Number of floating I/O pads: 0
  Number of floating terminals: 0
  Number of floating hierarchical blocks: 0
************************************************************
Loading cell instances...
Loading P/G wires and vias...
Number of VDDH Wires: 401
Number of VDDH Vias: 1808
Number of VDDH Terminals: 76
**************Verify net VDDH connectivity****************
  Number of floating wires: 0
  Number of floating vias: 0
  Number of floating std cells: 0
  Number of floating hard macros: 0
  Number of floating I/O pads: 0
  Number of floating terminals: 0
  Number of floating hierarchical blocks: 0
************************************************************
Loading cell instances...
Loading P/G wires and vias...
Number of VSS Wires: 4261
Number of VSS Vias: 51697
Number of VSS Terminals: 223
**************Verify net VSS connectivity****************
  Number of floating wires: 0
  Number of floating vias: 0
  Number of floating std cells: 0
  Number of floating hard macros: 0
  Number of floating I/O pads: 0
  Number of floating terminals: 0
  Number of floating hierarchical blocks: 0
************************************************************
Overall runtime: 3 seconds.
icc2_shell>
```

Verifies that all VDD and VSS nets are properly connected across the design.

- **Missing Via Check**

check_pg_missing_vias



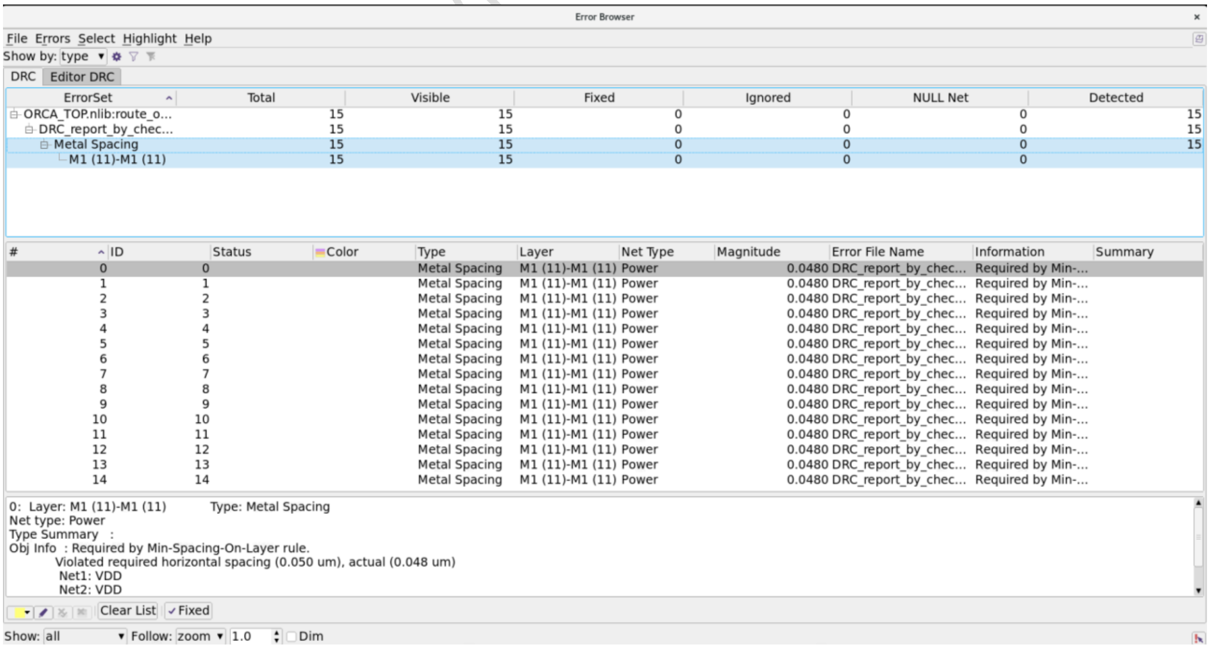
```
icc2_shell> check_pg_missing_vias
Check net VDD vias...
Number of missing vias: 0
Checking net VDD vias took 1 seconds.
Check net VDDH vias...
Number of missing vias: 0
Checking net VDDH vias took 0 seconds.
Check net VSS vias...
Number of missing vias: 0
Checking net VSS vias took 1 seconds.
Overall runtime: 2 seconds.
```

Identifies missing vias in power and ground paths that can cause floating metal segments or IR drop issues.

- **Power DRC Check**

check_pg_drc

```
icc2_shell> check_pg_drc
Command check_pg_drc started  at Tue Dec 30 11:37:37 2025
Command check_pg_drc finished at Tue Dec 30 11:38:37 2025
CPU usage for check_pg_drc: 60.68 seconds ( 0.02 hours)
Elapsed time for check_pg_drc: 60.35 seconds ( 0.02 hours)
Total number of errors found: 15
   15 insufficient spacings on M1
------------
Description of the errors can be seen in gui error set "DRC_report_by_check_pg_drc"
------------
```



ErrorSet	Total	Visible	Fixed	Ignored	NULL Net	Detected
ORCA_TOP.nlib:route_o...	15	15	0	0	0	15
DRC_report_by_chec...	15	15	0	0	0	15
Metal Spacing	15	15	0	0	0	15
M1 (11)-M1 (11)	15	15	0	0	0	

#	ID	Status	Color	Type	Layer	Net Type	Magnitude	Error File Name	Information	Summary
0	0			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	
1	1			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	
2	2			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	
3	3			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	
4	4			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	
5	5			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	
6	6			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	
7	7			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	
8	8			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	
9	9			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	
10	10			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	
11	11			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	
12	12			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	
13	13			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	
14	14			Metal Spacing	M1 (11)-M1 (11)	Power	0.0480	DRC_report_by_chec...	Required by Min-...	

```
0:  Layer: M1 (11)-M1 (11)          Type: Metal Spacing
Net type: Power
Type Summary   :
Obj Info  : Required by Min-Spacing-On-Layer rule.
       Violated required horizontal spacing (0.050 um), actual (0.048 um)
        Net1: VDD
        Net2: VDD
```

Checks power routing DRC while ignoring shapes inside hierarchical blocks to reduce false violations.

0: Layer: M1 (11)-M1 (11)   Type: Metal Spacing

Net type: Power

Type Summary :

Obj Info : Required by Min-Spacing-On-Layer rule.

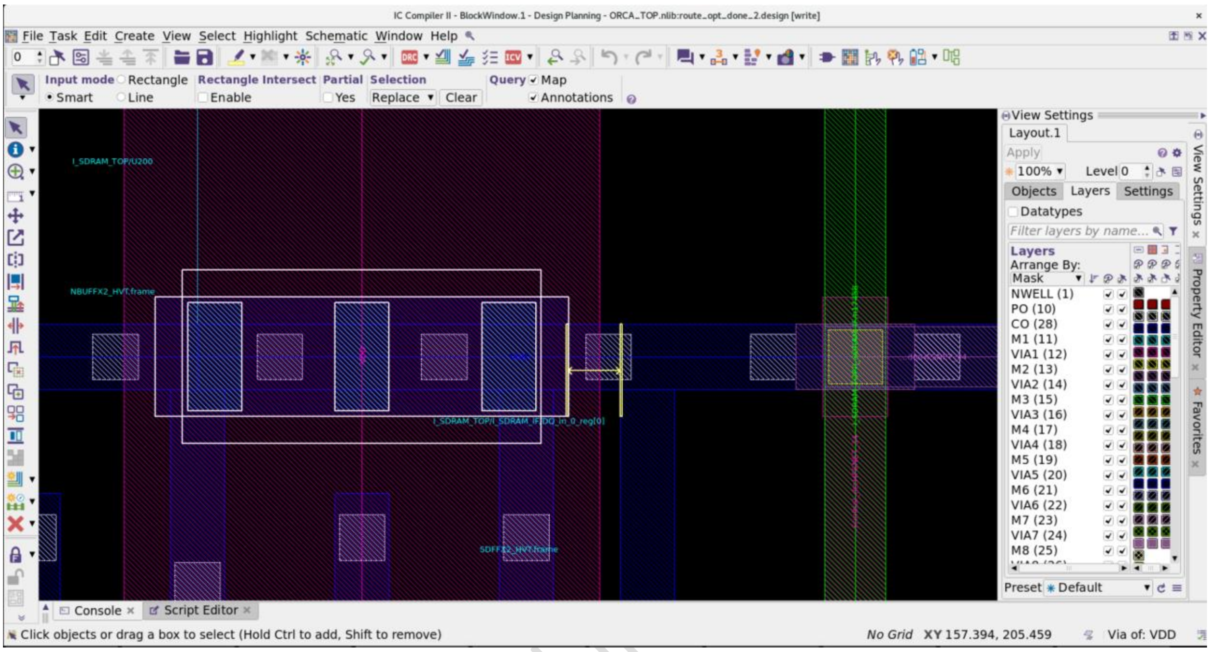
Violated required horizontal spacing (0.050 um), actual (0.048 um)

Net1: VDD

Net2: VDD

Error ID: 0 Status: Error

Bbox : (225.133 11.658) (225.185 11.743)

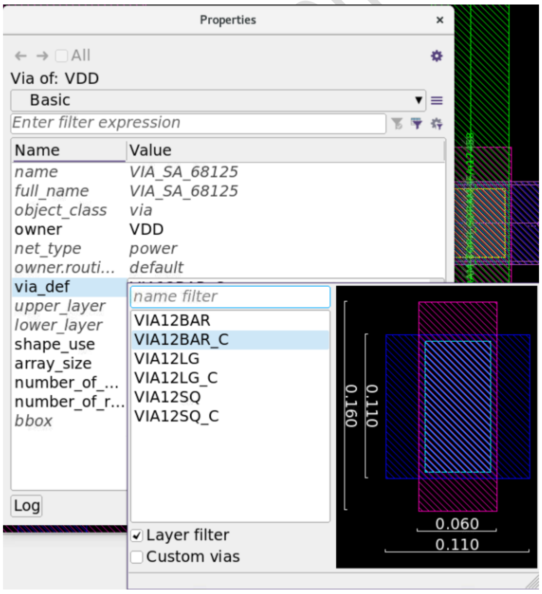


Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)   No Grid XY 157.394, 205.459   Via of: VDD

Fixes

Using gui method we can fix if there minimum number of violations

Select the via and do ctrl+r go to properties and reduce the via_def **VIA12BAR_C** to **VIA12SQ_C**



Via of: VDD

Name	Value
name	VIA_SA_68125
full_name	VIA_SA_68125
object_class	via
owner	VDD
net_type	power
owner.routi...	default
via_def	
upper_layer	
lower_layer	
shape_use	
array_size	
number_of_...	
number_of_r...	
bbox	

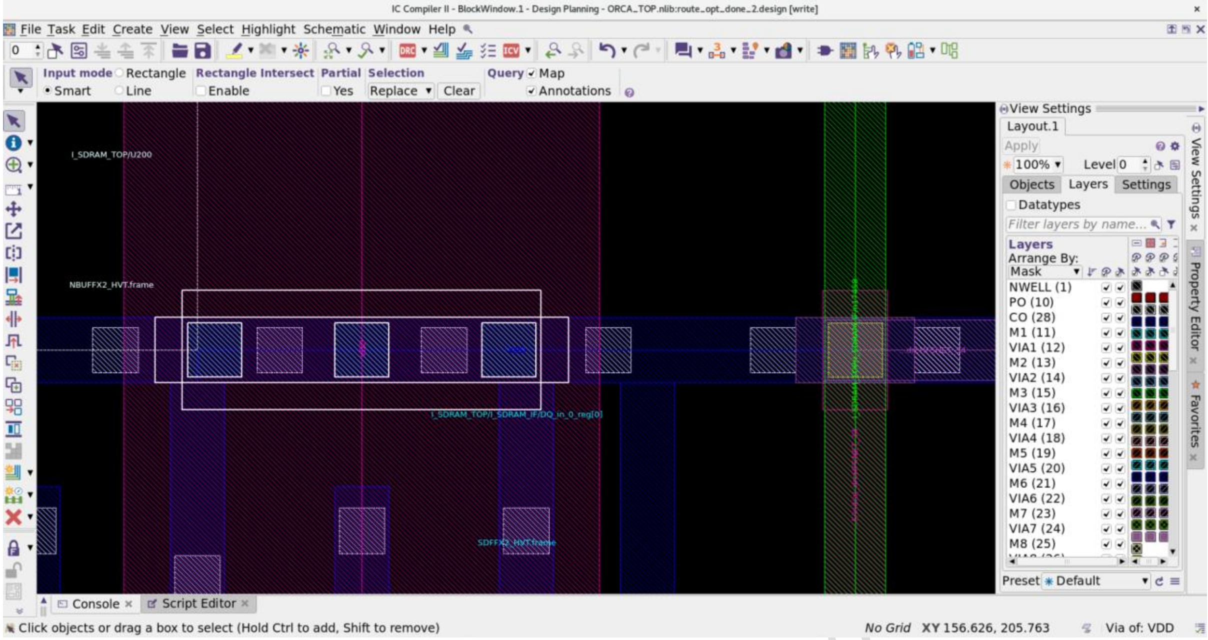
VIA12BAR
VIA12BAR_C
VIA12LG
VIA12LG_C
VIA12SQ
VIA12SQ_C

If there are 100’s of violation like this we can use command to slove in one go…..

```
set via [get_vias VIA_SA* -filter {via_def_name == "VIA12BAR_C"}]
```

set_attribute -objects [get_vias $via] -name via_def -value [get_via_defs -library [get_libs ORCA_TOP.nlib] VIA12SQ_C]

After fixes it look like this…….

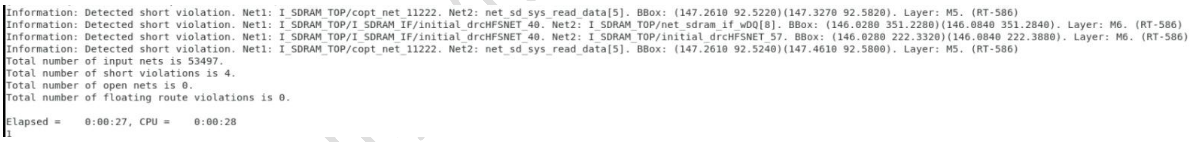


- **LVS Check**

LVS ensures logical equivalence between the layout and the schematic/netlist.

check_lvs -max_error 0

Confirms that the layout exactly matches the schematic with zero tolerance for mismatches.



```
Information: Detected short violation. Net1: I_SDRAM_TOP/copt_net_11222. Net2: net_sd_sys_read_data[5]. BBox: (147.2610 92.5220)(147.3270 92.5820). Layer: M5. (RT-586)
Information: Detected short violation. Net1: I_SDRAM_TOP/I_SDRAM_IF/initial_drcHFSNET_40. Net2: I_SDRAM_TOP/net_sdram_if_wDQ[8]. BBox: (146.0280 351.2280)(146.0840 351.2840). Layer: M6. (RT-586)
Information: Detected short violation. Net1: I_SDRAM_TOP/I_SDRAM_IF/initial_drcHFSNET_40. Net2: I_SDRAM_TOP/initial_drcHFSNET_57. BBox: (146.0280 222.3320)(146.0840 222.3880). Layer: M6. (RT-586)
Information: Detected short violation. Net1: I_SDRAM_TOP/copt_net_11222. Net2: net_sd_sys_read_data[5]. BBox: (147.2610 92.5240)(147.4610 92.5800). Layer: M5. (RT-586)
Total number of input nets is 53497.
Total number of short violations is 4.
Total number of open nets is 0.
Total number of floating route violations is 0.

Elapsed =     0:00:27, CPU =     0:00:28
1
```

In my design I don’t have open nets if it exists we can use the command route_eco and with the net name

ECO Routing for LVS Fix

When LVS violations are found on specific nets, ECO routing is used to fix only the affected nets without disturbing the entire routing.

route_eco -nets I_SDRAM_TOP/I_SDRAM_IF/n17458 -reuse_existing_global_route true -utilize_dangling_wires true -reroute modified_nets_first_then_others

-nets
Targets the specific net that has LVS or connectivity issues

• -reuse_existing_global_route true
Reuses existing global routing to minimize disturbance to clean routes

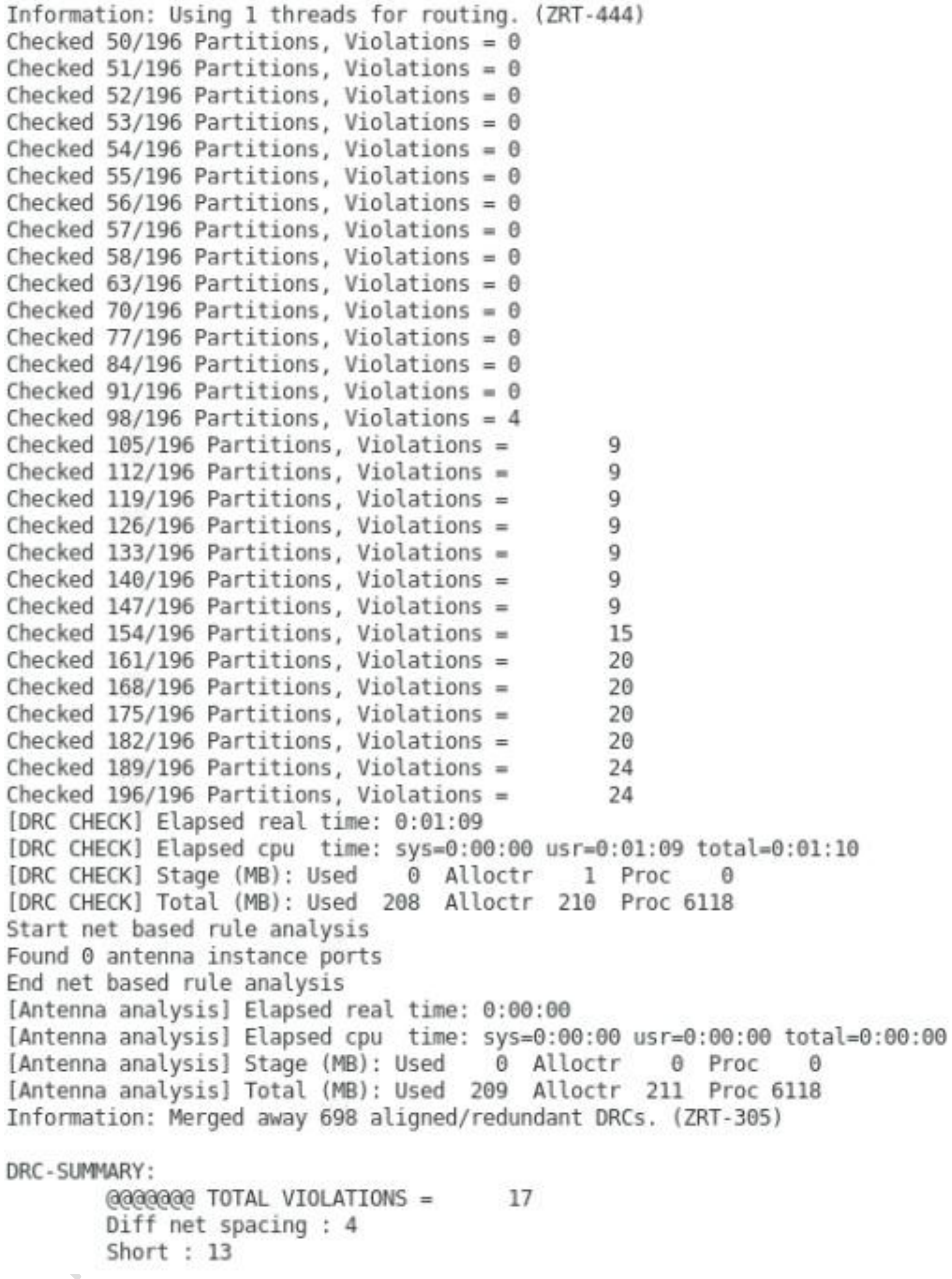
• -utilize_dangling_wires true
Reconnects floating or dangling wire segments instead of deleting them

- -reroute modified_nets_first_then_others

Prioritizes rerouting of modified nets before touching other nets

- **Routing DRC Check**

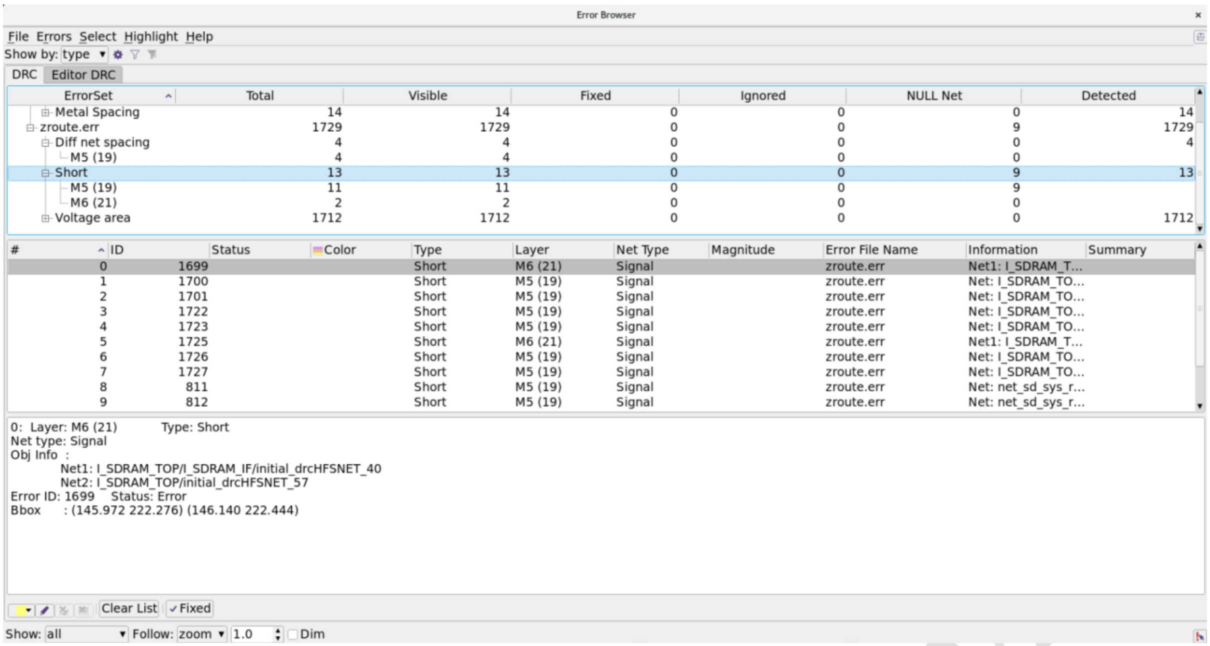
check_routes



```
Information: Using 1 threads for routing. (ZRT-444)
Checked 50/196 Partitions, Violations = 0
Checked 51/196 Partitions, Violations = 0
Checked 52/196 Partitions, Violations = 0
Checked 53/196 Partitions, Violations = 0
Checked 54/196 Partitions, Violations = 0
Checked 55/196 Partitions, Violations = 0
Checked 56/196 Partitions, Violations = 0
Checked 57/196 Partitions, Violations = 0
Checked 58/196 Partitions, Violations = 0
Checked 63/196 Partitions, Violations = 0
Checked 70/196 Partitions, Violations = 0
Checked 77/196 Partitions, Violations = 0
Checked 84/196 Partitions, Violations = 0
Checked 91/196 Partitions, Violations = 0
Checked 98/196 Partitions, Violations = 4
Checked 105/196 Partitions, Violations =        9
Checked 112/196 Partitions, Violations =        9
Checked 119/196 Partitions, Violations =        9
Checked 126/196 Partitions, Violations =        9
Checked 133/196 Partitions, Violations =        9
Checked 140/196 Partitions, Violations =        9
Checked 147/196 Partitions, Violations =        9
Checked 154/196 Partitions, Violations =        15
Checked 161/196 Partitions, Violations =        20
Checked 168/196 Partitions, Violations =        20
Checked 175/196 Partitions, Violations =        20
Checked 182/196 Partitions, Violations =        20
Checked 189/196 Partitions, Violations =        24
Checked 196/196 Partitions, Violations =        24
[DRC CHECK] Elapsed real time: 0:01:09
[DRC CHECK] Elapsed cpu  time: sys=0:00:00 usr=0:01:09 total=0:01:10
[DRC CHECK] Stage (MB): Used    0  Alloctr    1  Proc    0
[DRC CHECK] Total (MB): Used  208  Alloctr  210  Proc 6118
Start net based rule analysis
Found 0 antenna instance ports
End net based rule analysis
[Antenna analysis] Elapsed real time: 0:00:00
[Antenna analysis] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[Antenna analysis] Stage (MB): Used    0  Alloctr    0  Proc    0
[Antenna analysis] Total (MB): Used  209  Alloctr  211  Proc 6118
Information: Merged away 698 aligned/redundant DRCs. (ZRT-305)

DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      17
        Diff net spacing : 4
        Short : 13
```

Detects routing violations such as spacing, width, shorts, and opens in signal and power nets.

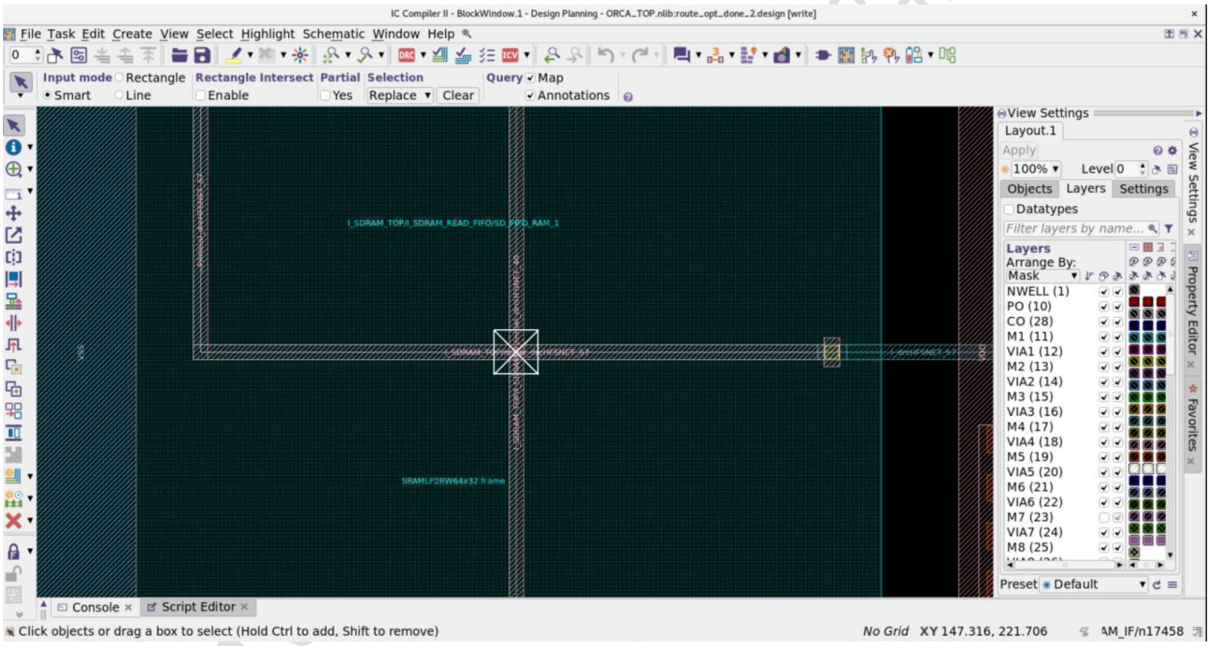


ErrorSet	Total	Visible	Fixed	Ignored	NULL Net	Detected
Metal Spacing	14	14	0	0	0	14
zroute.err	1729	1729	0	0	9	1729
Diff net spacing	4	4	0	0	0	4
M5 (19)	4	4	0	0	0	
Short	13	13	0	0	9	13
M5 (19)	11	11	0	0	9	
M6 (21)	2	2	0	0	0	
Voltage area	1712	1712	0	0	0	1712

#	ID	Status	Color	Type	Layer	Net Type	Magnitude	Error File Name	Information	Summary
0	1699			Short	M6 (21)	Signal		zroute.err	Net1: I_SDRAM_T...	
1	1700			Short	M5 (19)	Signal		zroute.err	Net: I_SDRAM_TO...	
2	1701			Short	M5 (19)	Signal		zroute.err	Net: I_SDRAM_TO...	
3	1722			Short	M5 (19)	Signal		zroute.err	Net: I_SDRAM_TO...	
4	1723			Short	M5 (19)	Signal		zroute.err	Net: I_SDRAM_TO...	
5	1725			Short	M6 (21)	Signal		zroute.err	Net1: I_SDRAM_T...	
6	1726			Short	M5 (19)	Signal		zroute.err	Net: I_SDRAM_TO...	
7	1727			Short	M5 (19)	Signal		zroute.err	Net: I_SDRAM_TO...	
8	811			Short	M5 (19)	Signal		zroute.err	Net: net_sd_sys_r...	
9	812			Short	M5 (19)	Signal		zroute.err	Net: net_sd_sys_r...	

```
0:  Layer: M6 (21)        Type: Short
Net type: Signal
Obj Info  :
          Net1: I_SDRAM_TOP/I_SDRAM_IF/initial_drcHFSNET_40
          Net2: I_SDRAM_TOP/initial_drcHFSNET_57
Error ID: 1699    Status: Error
Bbox      : (145.972 222.276) (146.140 222.444)
```

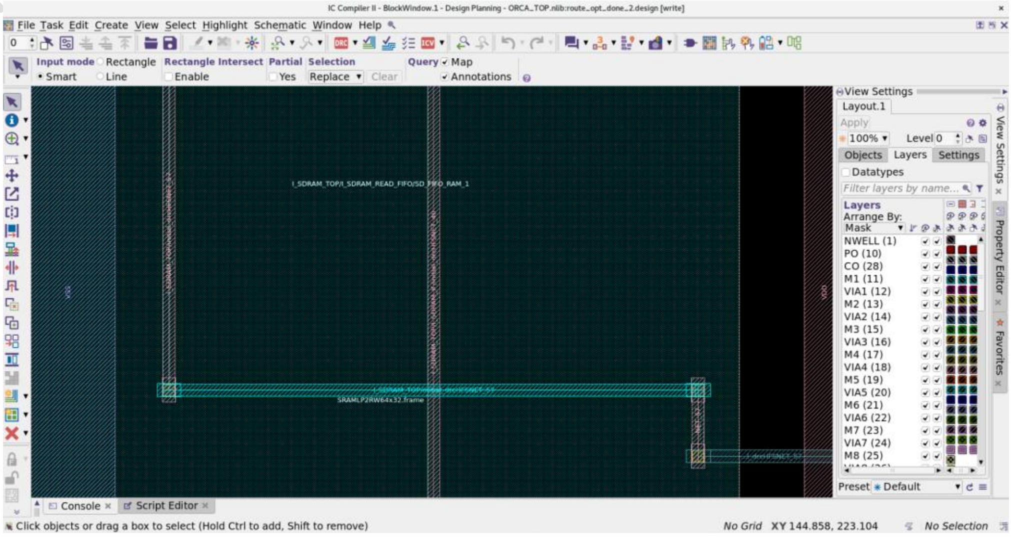
Shorts



Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)   No Grid XY 147.316, 221.706   AM_IF/n17458

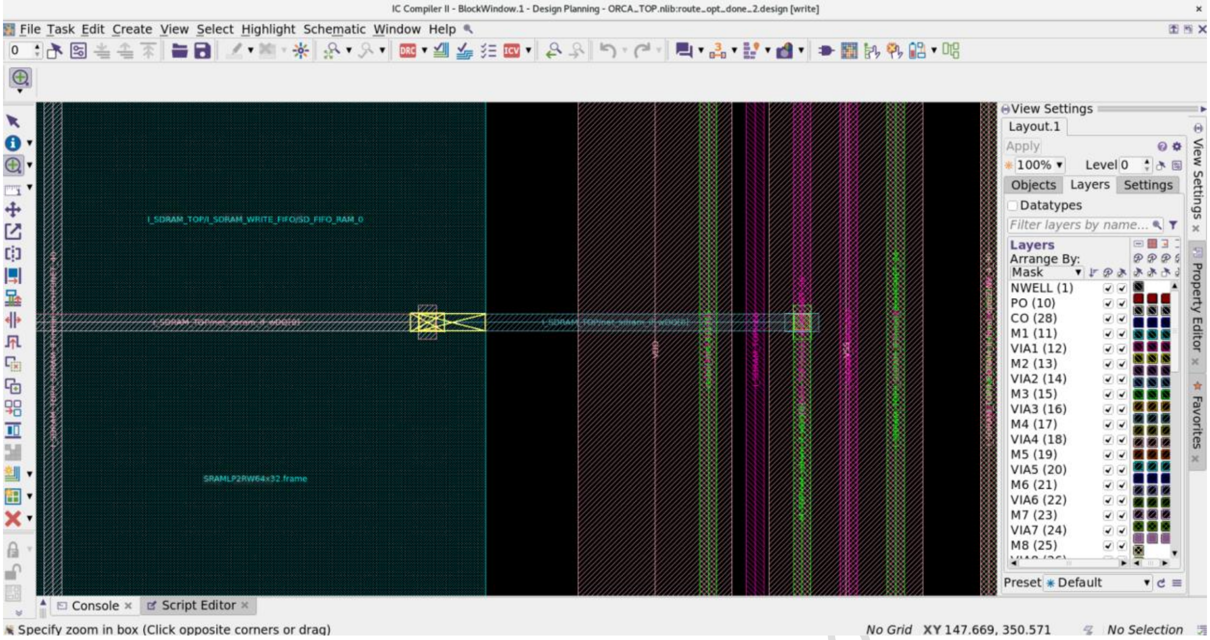
Metal layers {M6,M6} are same but different nets

Fixes



Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)   No Grid XY 144.858, 223.104   No Selection

I have used M7 metal layer to fix violation why because on top of macro M1 to M5 are already routes if I use any one of lower metal layers it will shorted.



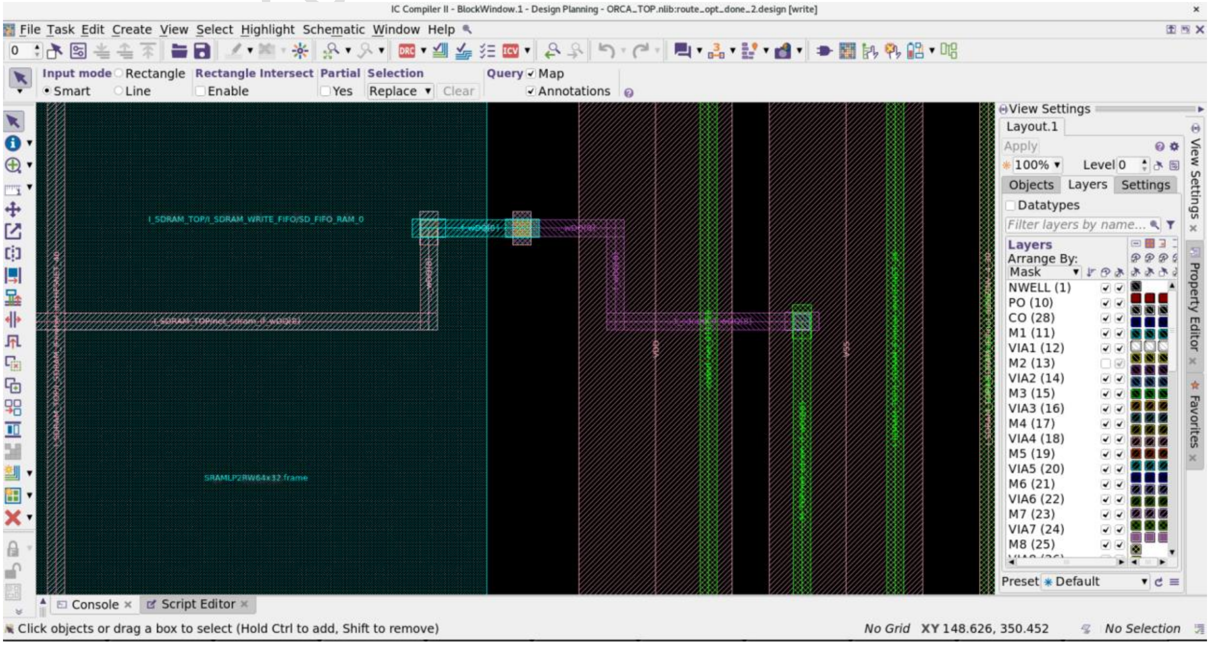
IC Compiler II - BlockWindow.1 - Design Planning - ORCA_TOP.nlib:route_opt_done_2.design [write]

Specify zoom in box (Click opposite corners or drag)

No Grid XY 147.669, 350.571 No Selection

M5 is shorted because it has entered the macro so we have to select the m5 layer which is connected up the m4 metal layer delete the m5 layer and via which is created between the m5 and m4 layer and re-route manually m3 layer up to the macro and continue with m7 layer and connect to m6 metal layer

This is the fixes

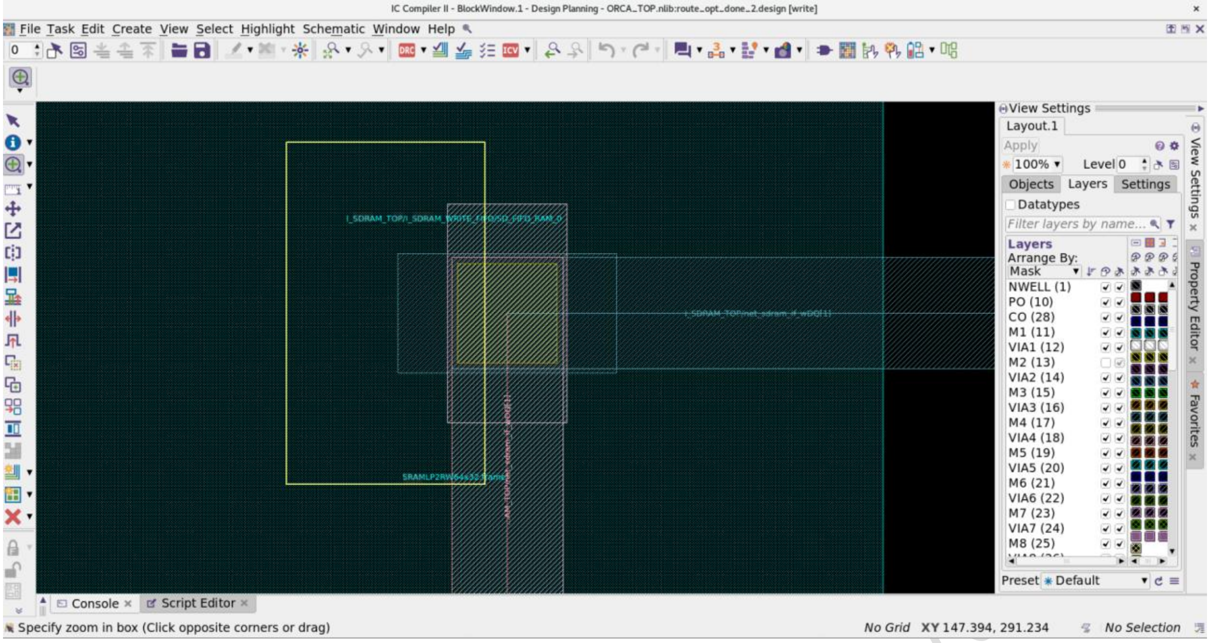


IC Compiler II - BlockWindow.1 - Design Planning - ORCA_TOP.nlib:route_opt_done_2.design [write]

Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)

No Grid XY 148.626, 350.452 No Selection

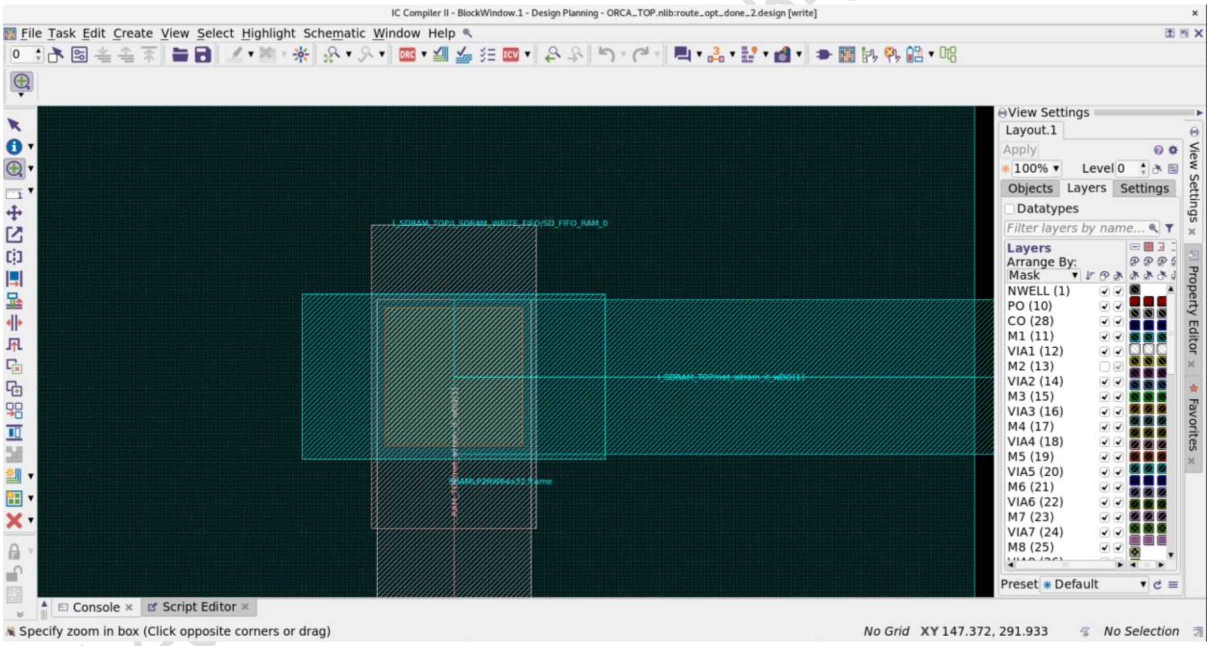
Different net spacing


IC Compiler II - BlockWindow.1 - Design Planning - ORCA_TOP.nlib:route_opt_done_2.design [write]

Specify zoom in box (Click opposite corners or drag)

No Grid XY 147.394, 291.234 No Selection

This violation comes because if there is same nets are routed but having net spacing and it is not followed the tech DRC rules so we can change the metal layers to M7


IC Compiler II - BlockWindow.1 - Design Planning - ORCA_TOP.nlib:route_opt_done_2.design [write]

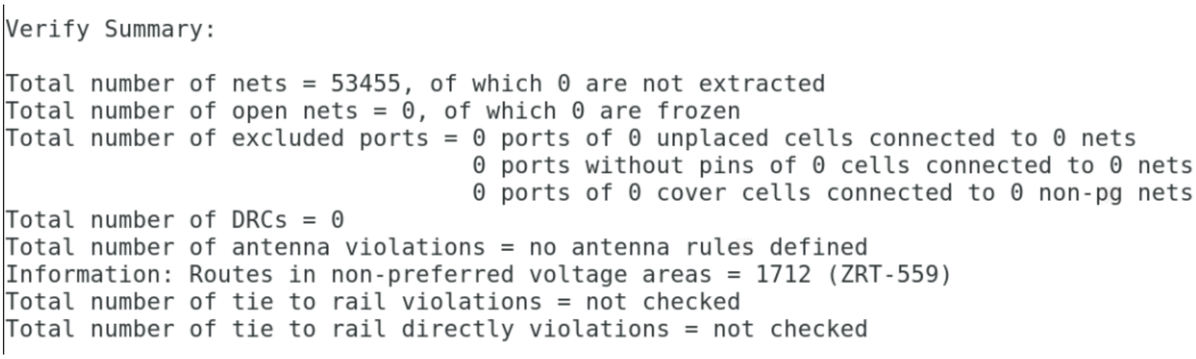
Specify zoom in box (Click opposite corners or drag)

No Grid XY 147.372, 291.933 No Selection

Now it is solved

Final checks after fixing all violations

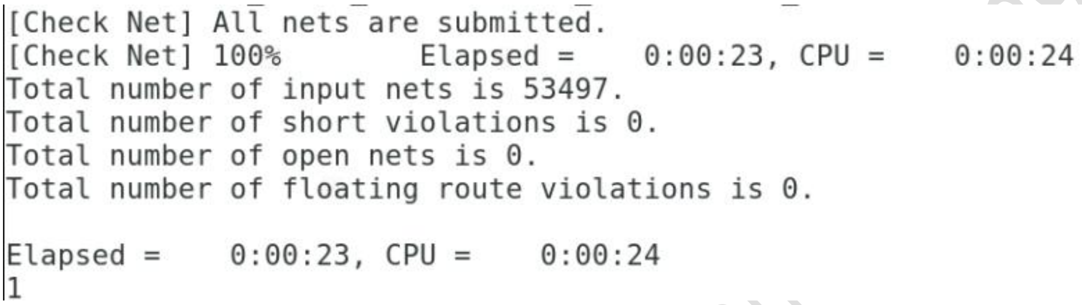
Check_routes



```
Verify Summary:

Total number of nets = 53455, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                 0 ports without pins of 0 cells connected to 0 nets
                                 0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 0
Total number of antenna violations = no antenna rules defined
Information: Routes in non-preferred voltage areas = 1712 (ZRT-559)
Total number of tie to rail violations = not checked
Total number of tie to rail directly violations = not checked
```

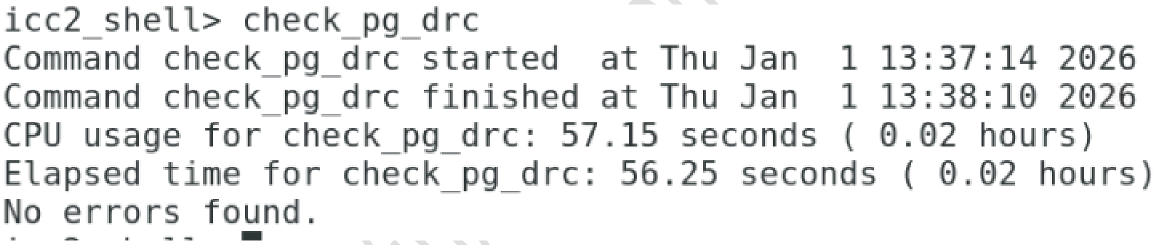
Check_lvs -max_error 0



```
[Check Net] All nets are submitted.
[Check Net] 100%        Elapsed =    0:00:23, CPU =    0:00:24
Total number of input nets is 53497.
Total number of short violations is 0.
Total number of open nets is 0.
Total number of floating route violations is 0.

Elapsed =    0:00:23, CPU =    0:00:24
1
```

Check_pg_drc



```
icc2_shell> check_pg_drc
Command check_pg_drc started  at Thu Jan  1 13:37:14 2026
Command check_pg_drc finished at Thu Jan  1 13:38:10 2026
CPU usage for check_pg_drc: 57.15 seconds ( 0.02 hours)
Elapsed time for check_pg_drc: 56.25 seconds ( 0.02 hours)
No errors found.
```