FPGAspeaks
Level - 1

Raj Kohale

10 September 2023

1 Introduction

In this Level I have learned Functionalities of basic logic gates using verilog programming.

Gates:

- AND gate :
  The AND gate is a basic digital logic gate that implements logical conjunction from mathematical logic. A HIGH output (1) results only if all the inputs to the AND gate are HIGH. Otherwise, LOW output results.Logical expression is Y=A.B
- OR gate
  The output is HIGH if either or both of the inputs are HIGH. If both inputs are LOW then the output is LOW. Logical expression for OR gate is Y= A +B.
- NOT gate
  A NOT gate performs logical negation on its input. If the input is HIGH then the output will be LOW. Similarly,a LOW input results in a HIGH output. Logical expression for NOT gate is Y= ˜A
- NAND gate
  A logic gate which produces an output which is LOW only if all its inputs are HIGH. thus its output is complement to that of an AND gate. Logical expression for NAND gate is Y= ˜(A.B)
- NOR gate
  A HIGH output (1) results if both the inputs to the gate are LOW (0); if one or both input is HIGH (1), a LOW output (0) results. NOR is the result of the negation of the OR operator. Logical expression for NOR gate is Y= ˜(A+B).
- XOR gate
  The output is HIGH if either, but not both of the inputs are HIGH.The output is LOW if both inputs are LOW or if both inputs are HIGH.
- XNOR gate
  The output of an XNOR gate is HIGH when all of its inputs are HIGH or when all of its inputs are LOW.

2 Pre - Requisite

- Truth table and expression of logic gates
- Verilog HDL Language

3 Tools/Requirements

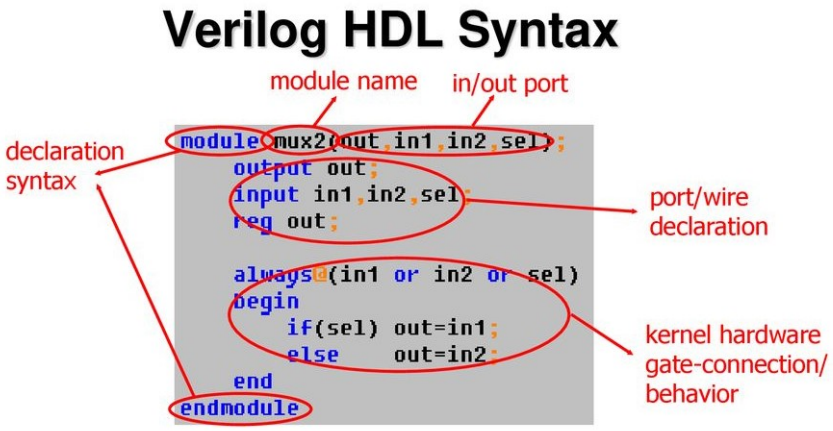
Xiling Vivado To simulate and for observing behaviour of different logic gate we need Xiling Vivado tool.Vivado is a software for synthesis and analysis of hardware description language designs, superseding Xilinx ISE with additional features for system on a chip development and high-level synthesis.

4 What have I done?

I have written Verilog code for all logic gates in verilog hdl language by using modules.

basic syntax of module:

example,



I have written all codes according to given module syntax in Xiling Vivado and perform Simulation to observed functionalities of logic gate according to given input signals. Also obtain RTL Schematics for each logic gate and for further use I am making a collection of each logic gate code on Github under project **"FPGAspeaks"** .

5 Observation

Simulation of AND gate

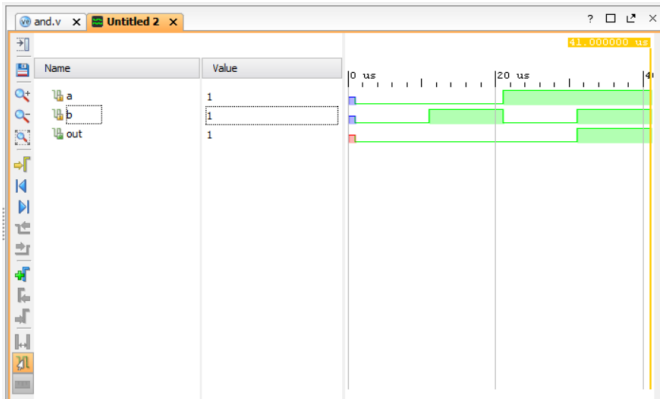


Figure 1: Simulation

RTL SChematic for AND gate

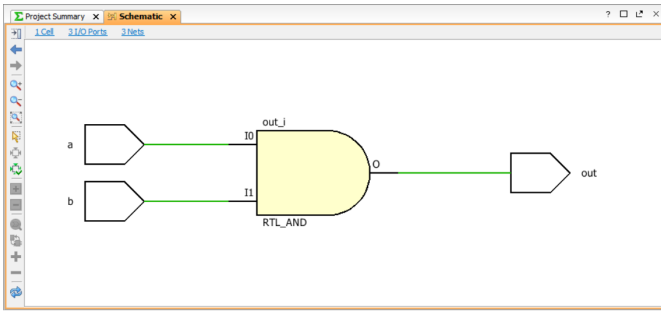


Figure 2: RTL Schematic

Similarly, I have observed simulation and RTL schematic for all basic logic gates.

6 For more information

6.1 Github