Report on D2DAdapter

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1. Introduction

Universal Chiplet Interconnect Express (UCIe) represents a significant advancement in semiconductor technology, offering a sophisticated, open, on-package interconnect solution that integrates multiple dies within a single package. By supporting a range of protocols, including Peripheral Component Interconnect Express (PCIe), Compute Express Link (CXL), and various streaming formats, UCIe delivers a versatile framework capable of accommodating diverse data transfer requirements. Additionally, its provision for a raw format enables the seamless incorporation of emerging protocols, ensuring adaptability and forward compatibility. The architecture is pivotal in promoting a flexible and scalable ecosystem for disaggregated die architectures, driving enhancements in both power efficiency and overall system performance. The implementation of UCIe is poised to redefine the landscape of chiplet-based design, facilitating unprecedented levels of integration and interoperability in advanced computing environment.

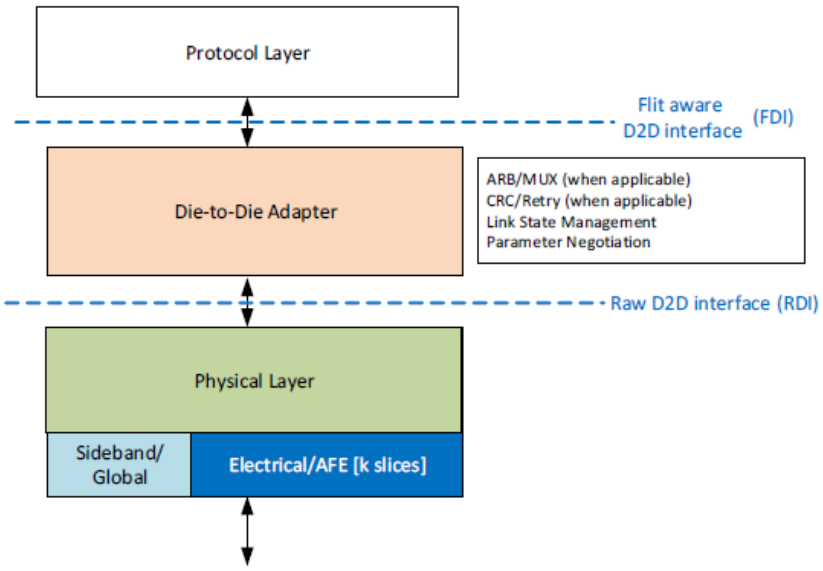

Figure 1: UCIe Layers and Functionalities [1]

Employing an Off-Package Interconnect, a UCIe Retimer can effectively extend UCIe connectivity beyond the confines of the package, leveraging electrical, optical and other advanced technologies to facilitate communication at the rack or pod level. UCIe operates as a layered protocol, meticulously structured with each layer executing specific tasks to ensure seamless functionality. The UCIe stack is divided into three primary components, each responsible for delivering the requisite bandwidth and capabilities. Critical handshakes and state transitions within the stack are governed by predefined timeouts and fault mechanisms, with all timeout values adhering to a strict tolerance range of -0 percent to + 50 percent. Following a domain test, it is imperative that all timeout and counter values are recalibrated to their designated settings to maintain operational integrity. This rigorous framework ensures that every element within the UCIe stack can reliably meet performance expectations, supporting the sophisticated demands of modern interconnected systems.

2. Protocol Layer

The protocol layer within the Universal Chiplet Interconnect Express (UCIe) specification epitomizes a pivotal element in the seamless data transfer between disparate dies within a pacakage. Engineered to support a plethora of protocols, notably Peripheral Component Interconnect Express (PCIe) and Compute Express Link (CXL), alongside various streaming protocols, this layer ensures robust interoperability and optimized data transmission. It meticulous orchestrates the intricate processes of data exchange, error correction, and protocol negotiations, thereby enhancing the efficiency and reliability of inter-die communication. Integral to the UCIe architecture, the protocol layer synergizes with the Die-to-Die-Adapter, underpinning the sophisticated mechanisms required for maintaining protocol coherence and managing complex data flows. This orchestration not only underscores the architectural sophistication of Ucie but also fortifies its role in advancing high-performance computing and scalable chiplet-based designs.

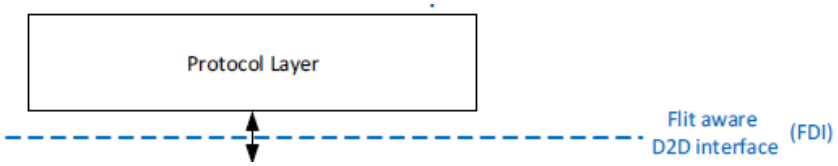

Figure 2: Protocol Layer [1]

3. Physical Layer

The Physical Layer in the Universal Chiplet Interconnect Express (UCIe) specification stands as a cornerstone in the architecture, meticulously orchestrating the electrical and logical dimensions of data transmission between dies within a semiconductor package. This layer is meticulously crafted to ensure data is conveyed with utmost accuracy and efficiency across the physical medium, safeguarding the integrity and performance of the interconnect. It is subdivided into a series of specialized subcomponents and functions, each integral to the overall operation. These subcomponents collectively manage signal integrity, error detection, and correction mechanisms, as well as synchronization and timing control, thereby fortifying the robustness of the communication channel. By meticulously addressing the nuanced challenges of high-speed data transfer, the Physical Layer upholds the reliability and efficacy of UCIe, fostering advancements in semiconductor technology and enhancing the capabilities of integrated systems.

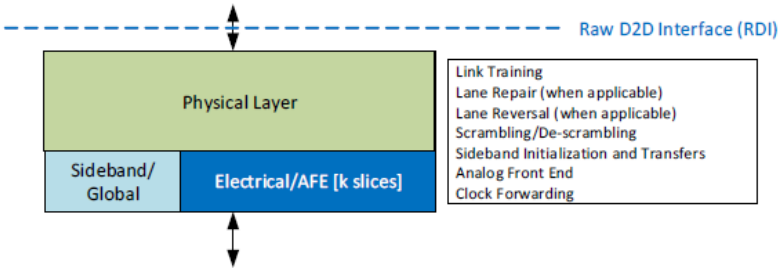

Figure 3: Physical Layer [1]

4. Die-to-Die (D2D Adapter)

The Die-to-Die (D2D) Adapter is an indispensable element within the Universal Chiplet Interconnect Express (UCIe) framework, acting as the vital conduit between the Protocol Layer and the Physical Layer. This sophisticated component is engineered to ensure seamless communication and data transfer across the UCIe link, thereby enhancing both performance and interoperability. By meticulously coordinating a multitude of functions, the D2DAdapter not only facilitates efficient data flow but also upholds the integrity and reliability of the transmission process. Its role extends to optimizing signal integrity and managing the complex interactions between different layers, making it a cornerstone in the architecture of modern chiplet-based systems. The precision and robustness of the D2DAdapter underscore its critical importance in advancing the capabilities of the UCIe specification, driving forward the evolution of high-performance computing and integrated circuit design.

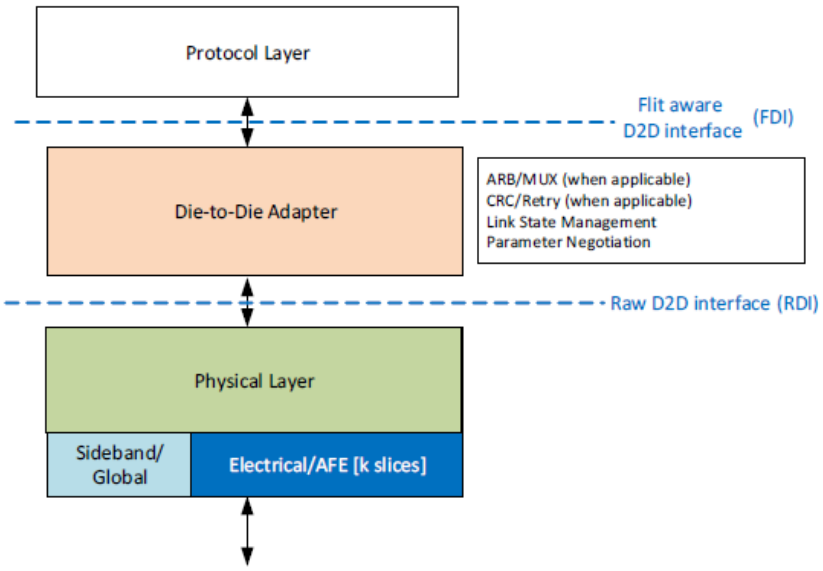

Figure 4: D2DAdapter and it's work flow [1]

5. Key functions and features of the D2DAdapter

- **Coordination with Protocol and Physical Layers:**The D2DAdapter operates with dual interfacing capabilities, engaging with the Protocol Layer through the Flit-aware Die-to-Die Interface (FDI) and with the Physical Layer via the Raw Die-to-Die Interface (RDI). This bifurcated approach facilitates a seamless integration of data transfer and protocol management. By minimizing the logic required on the primary data path, the D2DAdapter optimizes latency, ensuring an efficient and high-performance data flow tailored for protocol Flits.

- **Protocol Support and Multiplexing:**The D2DAdapter is engineered to support a diverse array of protocols, encompassing PCIe, CXL, and Streaming protocols. It adeptly accommodates various Flit formats and operational modes, which are negotiated with the remote Link partner to ensure seamless integration. In scenarios

where multiple protocols are concurrently active, the D2DAdapter employs sophisticated arbitration and multiplexing (ARB/MUX) techniques to optimize data flow management and maintain operational efficiency.

- **Error Handling and Retry Mechanisms:**In scenarios where the raw Bit Error Rate (BER) exceeds 1e-27, the D2DAdapter implements a CRC and Retry scheme to ensure data integrity. This is particularly important for protocols like PCIe, CXL, and Streaming. The D2DAdapter is responsible for performing necessary handshakes and parameter exchanges to bring the RDI to an active state while keeping the FDI in reset to prevent main band traffic during certain compliance modes.

- **Link State Management and Parameter Negotiation:** The D2D Adapter manages the higher-level Link State Machine (LSM) and coordinates the bring-up process, including protocol options and parameter exchanges with the remote Link partner. It also handles power management coordination, ensuring efficient power usage across the UCIe link.

- **Compliance and Testing:** The D2DAdapter includes a Test/Compliance Register Block, which allows for testing and compliance verification. This block includes registers for controlling compliance modes and performing necessary handshakes and parameter exchanges. The Adapter must support various capabilities and Flit formats to ensure interoperability and compliance with the UCIe specification.

- **Mailbox and Sideband Communication:** The D2DAdapter uses a mailbox mechanism for indirect access to remote die registers. Theis involves sending request over the FDI and receiving responses over the RDI and sideband channels. It manages sideband message transmission and reception, which are used for control and management purposes.

- **Power Management:**The Adapter coordinates power management states and transitions, including entry and exit form power management modes. It ensures that all conditions for power management entry are met and handles any pending sideband requests for power management exit.

6. Operational Flow of D2DAdapter

- **Protocol Layer:**
  Input: Receives protocol-specific data packets (Flits) from the system.
  Output: Sends Flits to the D2DAdapter via the Flit-aware Die-to-Die Interface (FDI).

- **D2DAdapter:**
  FDI: Receives Flits from the Protocol Layer.
  ARB/MUX: If multiple protocols are in use, this component arbitrates and multiplexes the data streams.
  CRC/Retry Mechanisms: Ensures data integrity by performing CRC checks and implementing retry mechanisms in errors are detected.
  Link State Management: Manages the state of the link, ensuring proper initialization, training, and maintenance.

Parameter Negotiation: Handles the exchange of protocol and parameter information with the remote link partner.
RDI: Sends processed Flits to the Physical Layer for raw data transmission.

- **Physical Layer:**
  Input: Receives processed Flits from the D2DAdapter via the Raw Die-to-Die Interface (RDI).
  Output: Transmits raw data between dies, ensuring accurate and efficient communication.

7. My Work

The UCIe Digital repository on GitHub, maintained under the account "ucb-ucie," [2] is a sophisticated collection of modules designed to facilitate the implementation of various digital protocols. Written entirely in Scala, these modules exemplify advanced programming techniques and architectural design principles, making the repository an invaluable resource for developers and researchers in digital systems design. The project's scope and depth reflect a concerted effort to bridge theoretical concepts with practical applications, demonstrating the power of Scala in handling complex digital design tasks. In my recent endeavor, I focused on generating Verilog files for several key modules within the repository: D2DAdapter, e2e, logphy, and protocol. This task required not only a thorough understanding of the underlying Scala code but also a meticulous approach to ensure accurate translation into Verilog. Each module presented unique challenges, necessitating a deep dive into the specifics of digital communication and logic design. The successful generation of these Verilog files signifies a pivotal step in advancing the repository's usability, enabling seamless integration with hardware design workflows.

Utilizing the sophisticated tools like CLion and GitHub Copilot, I adeptly generated Verilog files, demonstrating a robust command over modern development tools. My efforts culminated in the successful completion of the Zero to ASIC course, an intensive program designed to impart comprehensive knowledge and practical skills in ASIC design. Through this course, I developed and refined my ability to produce GDS II files for the D2DAdapter.

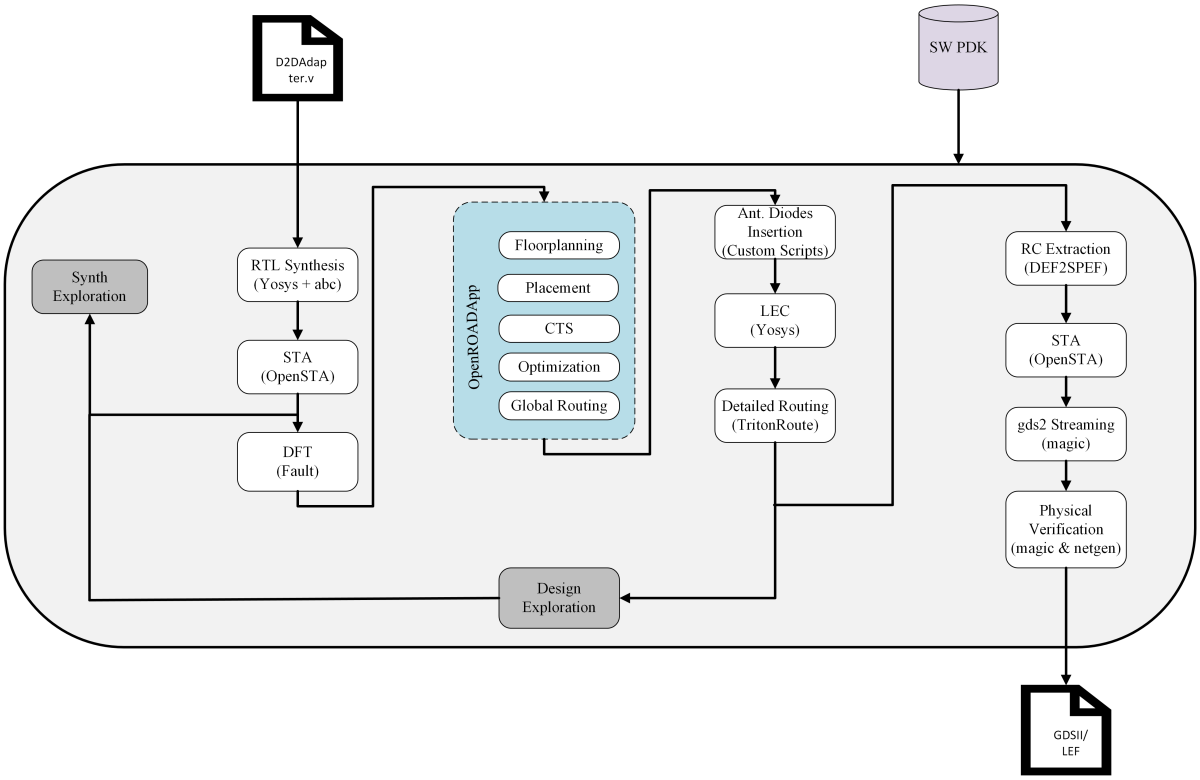

Figure 5: The OpenLane Flow for generating GDSII file. "It involves Floorplanning, RTL Synthesis, Placement and Optimization, Clock Tree Synthesis, Routing, Design Verification and GDSII Streaming."

OpenLane is a cutting-edge silicon implementation platform that supports both open-source tools, including Yosys, OpenROAD, Magic, and KLayout, as well as other open-source and proprietary utilities. Figure 5 explains the work flow of openlane for generating GDSII layout of D2DAdapter. [4] At floorplannig stage, the initial step involves organizing the layout of the chip's major functional blocks. It sets the stage for efficient placement and routing. Uisng tools like Yosys and ABC, the Register Transfer Level(RTL) design is synthesized into a gate-level netlist, which is a more detailed representation of the circuit. Thir third stage is placement and optimization stage, where the synthesized netlist undergoes placement, where the physical locations of the cells are determined. Optimization processes are applied to improve performance metrics like timing, area, and power. The fourth stage is Clock Tree Synthesis (CTS). This step involves designing the clock distribution network to ensure that clock signals reach all parts of the chip with minimal skew. The fifth stage is routing. At this stage the design goes through global and detailed routing phases using tools like TritonRoute. This involves creating the physical connections between the placed cells. The sixth stage is Design Verification. Before generating the final layout, the design is verified for correctness using tools like Magic and Netgen, ensuring that it meets all design rules and specifications. The final stage is GDSII Streaming. Once the design is verified, it is converted into the GDSII format, which is the standard file format for IC layout data. This file contains all the geometric shapes and patterns needed for fabricating the chip. We used SkyWater SKY130nm technology PDK for building the gds file and which is a final layout of D2DAdapter. It is a open source PDK. [3]

8. Results

8.1. Floor planning

During the floorplanning stage, OpenLane determines the necessary area to accommodate all components. The required standard cells are strategically placed in the bottom-left corner, preparing the design for the place-and-route stage. The Core Area dimensions of the D2DAdapter are 5.52µm, 10.88µm, 1309.16µm, 1313.76µm. The Die Area dimensions of the D2DAdapter are 0.0µm, 0.0µm, 1314.84µm, and 1325.56µm. Chip area for module D2DAdapter: 849947.667200 μm^2

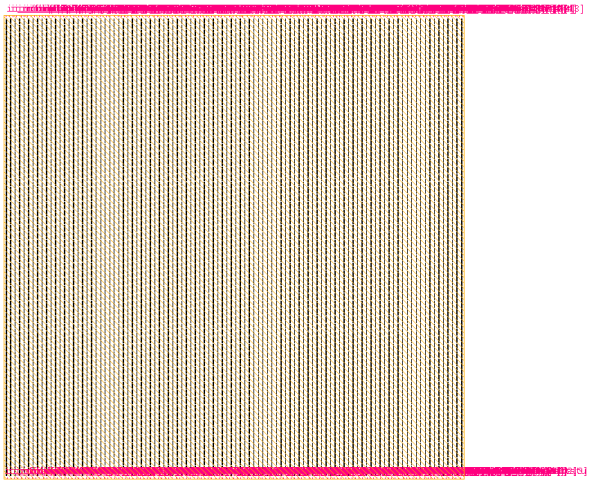

Figure 6: Floorplan of D2DAdapter. "At the floorplanning stage, OpenLane determines the necessary area to accommodate all components."

8.2. Power Delivery Network (PDN)

The Power Delivery Network is responsible for providing power for all the macros in the design. For instance, memories, processor core, serdes, PLL, Power grid cells etc. The purple lines and the blue lines are the power rails.

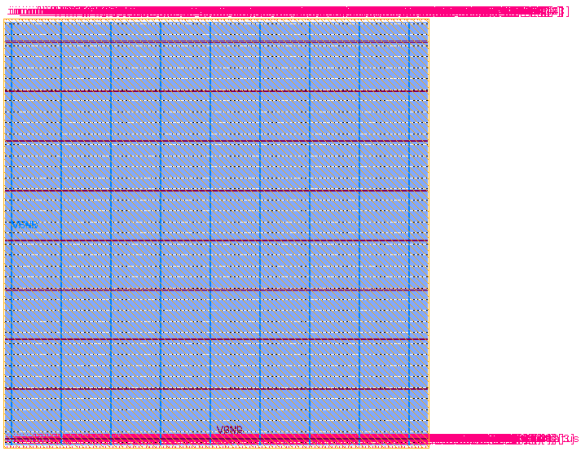

Figure 7: Power Delivery Network (PDN) of D2DAdapter. "Supplies power to all macros"

8.3. Gloabal Placement

Placements are of two types. Gloabal placement is one of them. In the figure, this placement introduced dramatic changes by distrubing all the instances to appropriate locations in the global scale with minor overlaps.

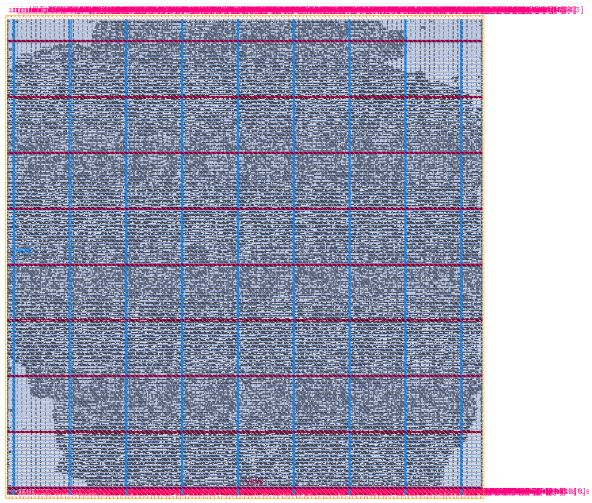

Figure 8: Global placement of D2DAdapter. " Allows cell overlap and non-row alignment, with overlaps resolved during legalization and specific values optimized."

The global placement has relaxed constraints: Cells and macros can overlap, the overlap will be removed during legalization. Also they need not be placed strictly in rows yet. However, certain values should be optimized.

8.4. Detailed Placement

Detailed placement adjusts each instance to a nearby legal location with minimal changes to the overall layout. It legalizes all the cell locations and produces a high-quality, non-overlapping placement. At this stage, cells are spread out to remove all overlaps.

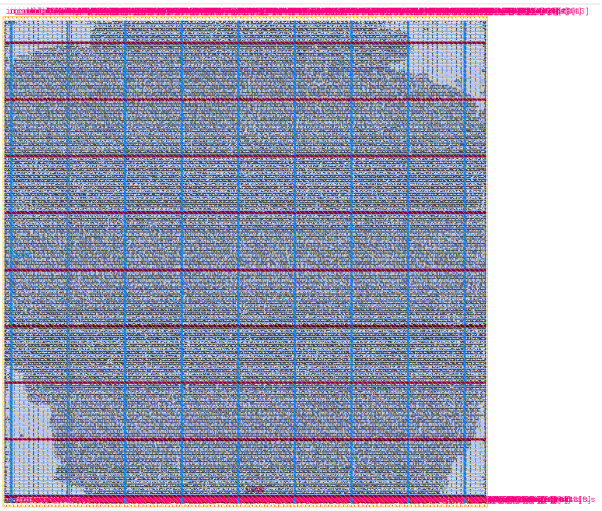

Figure 9: Detailed placement of D2DAdapter."Ensures all cells are legally positioned and non-overlapping."

8.5. GDSII

GDS files are used in the ASIC manufacturing process to describe the physical layout of the chip.

Figure 10: Final GDS Layout. "GDSII: Binary format depicting layers for ASIC production."

This includes the precise geometric shapes of different layers, such as metal layers, diffusion layers, and polysilicon layers, that are used to fabricate the integrated circuit.

9. Conclusion

Universal Chiplet Interconnect Express (UCIe) represents a key advancement in semiconductor technology, providing an open, on-package interconnect solution that enables efficient integration of multiple dies within a single package.The D2DAdapter is responsible for ensuring reliable data transfer, managing arbitration and multiplexing, overseeing link state management, and handling protocol and parameter negotiation with the remote link partner. The OpenLane and SKY water 130nm technology PDK helped in generating a GDSII file of D2DAdapter. Overall, this experience underscored the importance of a robust understanding of both software and hardware paradigms, illustrating the critical interplay between them in modern digital system design.

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