Report For VHDL Project

*HalfAdder: to sum 2bits.

*FullAdder: to sum 3bits.

*RCA: to sum n-bit+n-bit

First Stage:

-Idea:

We want to add 3numbers x,y,z in s,c
we declare x,y,z,s,c as bit_vector with size 4 bits

Then we add each column and the sum append to s and the carry append to c

Like this:

we add the first right bit x,y,z and add it in s and carry in c

Like this x(0)+y(0)+z(0)=s(0) and c(0)

x(1)+y(1)+z(1)=s(1) and c(1)

x(2)+y(2)+z(2)=s(2) and c(2)

x(3)+y(3)+z(3)=s(3) and c(3)

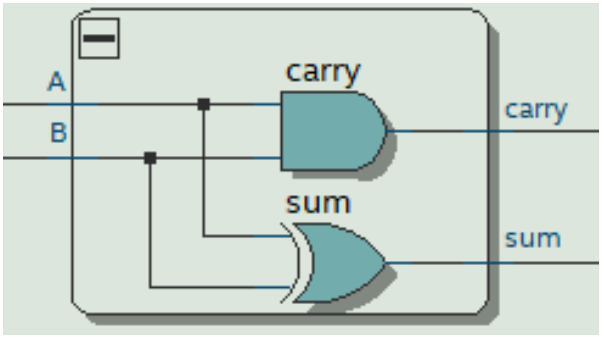
and because we added 3 bits we will use FullAdder

Conclusion we need 4FullAdders in this stage.

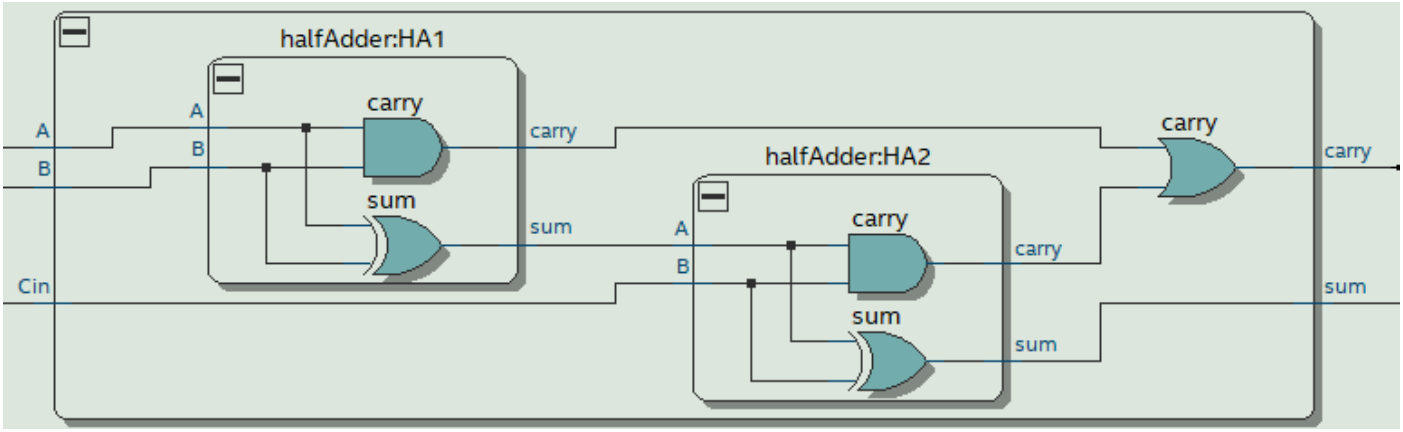
- InCoding:

1.Implement FullAdder Entity using two instances from HalfAdder Entity.

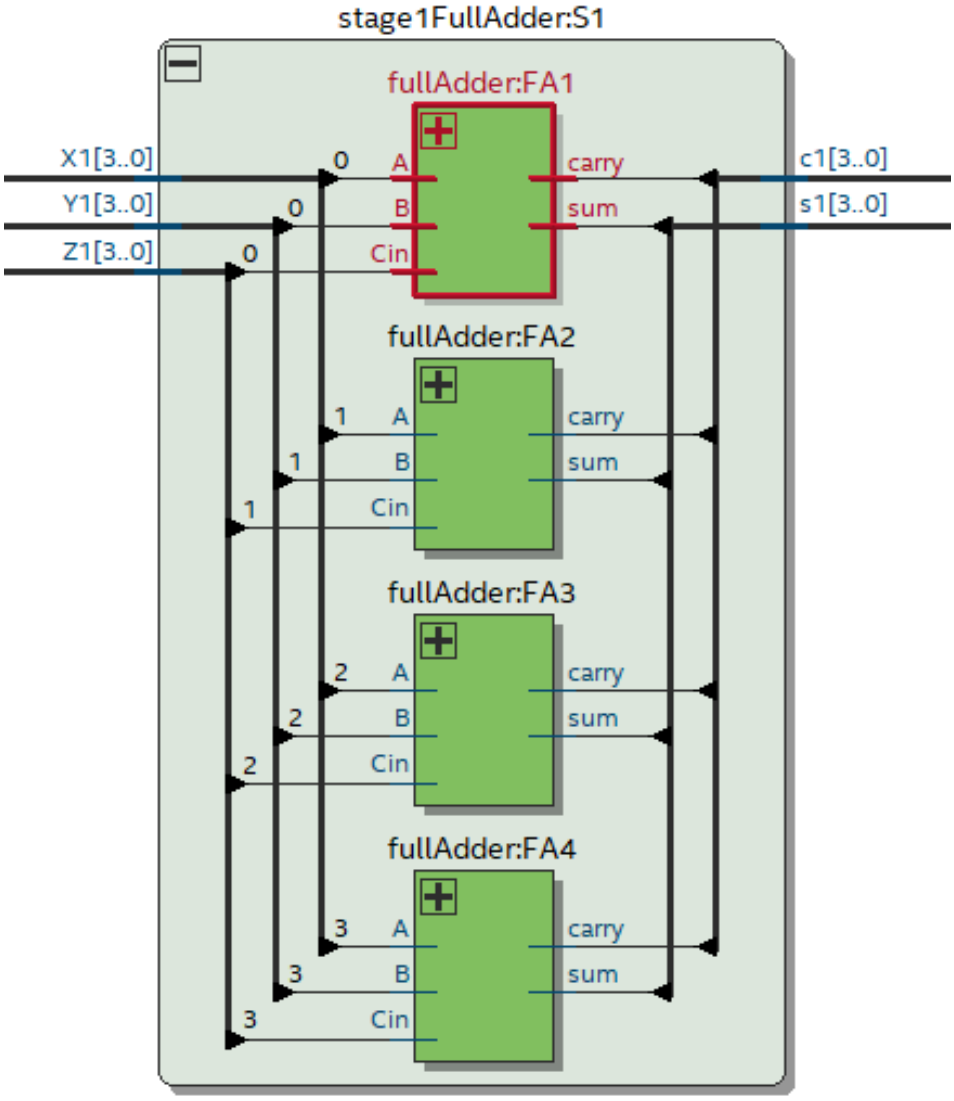
**HalfAdder:

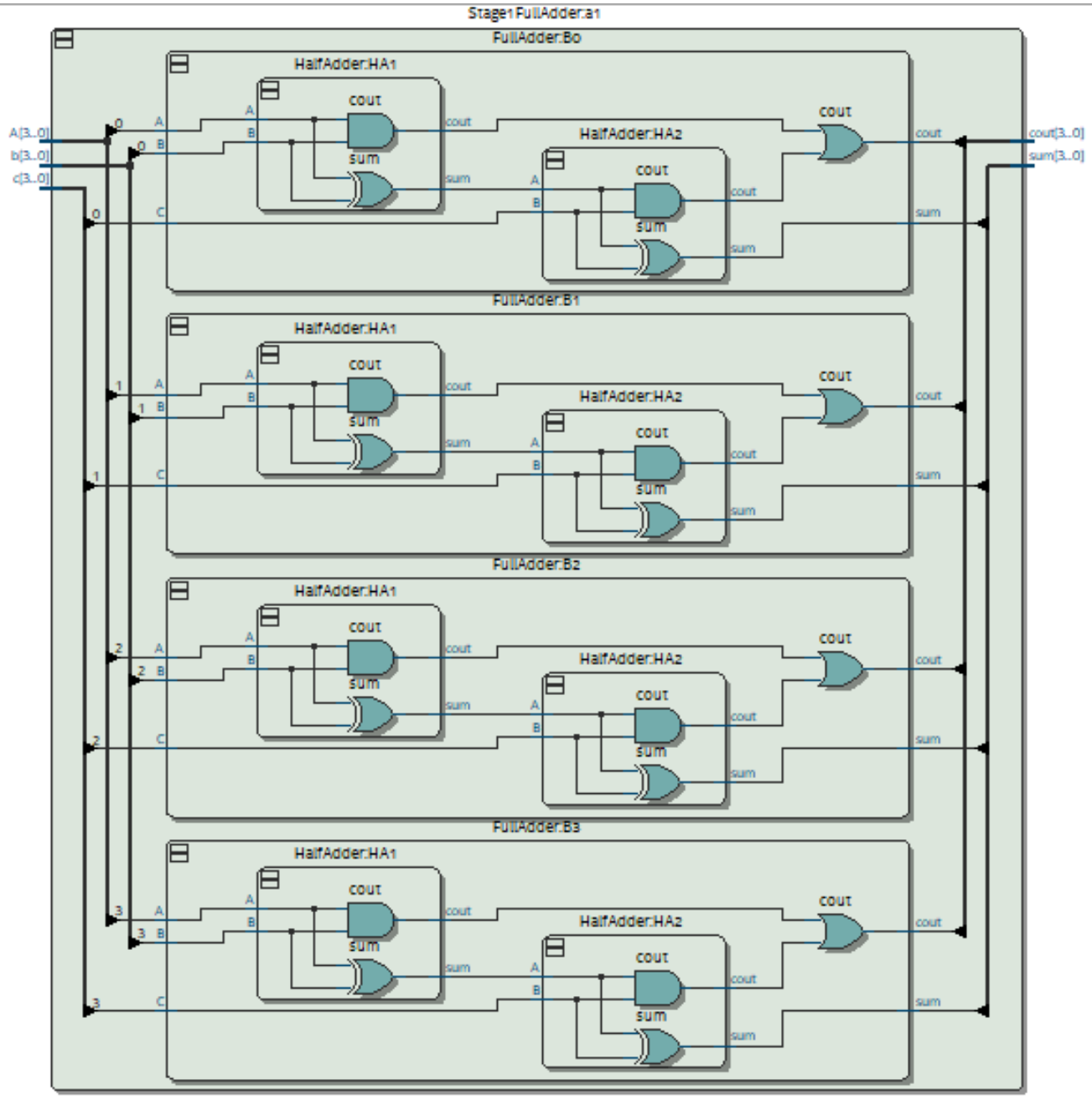


**FullAdder:



2.Implement stage1 by using 4instances from FullAdder:





Stage1 is done.

Second Stage:

We have 2bit_vector s,c with size 4bit

And declare bit_vector sum with size 5bit ,one bit carry.

-idea:

1.keep the first left bit in s the same because it isn't have carry to add

Sum(0)<=s(0)

2.add the next bit (second bit) in s with the first bit in carry, and put the carry in c1(it is a signal to connect the next step)

Sum(1)<=s(1)+c(0)+'0'(no additional carry)

3.add the third bit in s with the second bit in carry and the c1 from previous step, and put the carry in c2(it is a signal to connect the next step)

Sum(2)<=s(2)+c(1)+c1

4.add the fourth bit in s with the third bit in carry and the c2 from previous step, and put the carry in c3(it is a signal to connect the next step)

Sum(3)<=s(3)+c(2)+c2

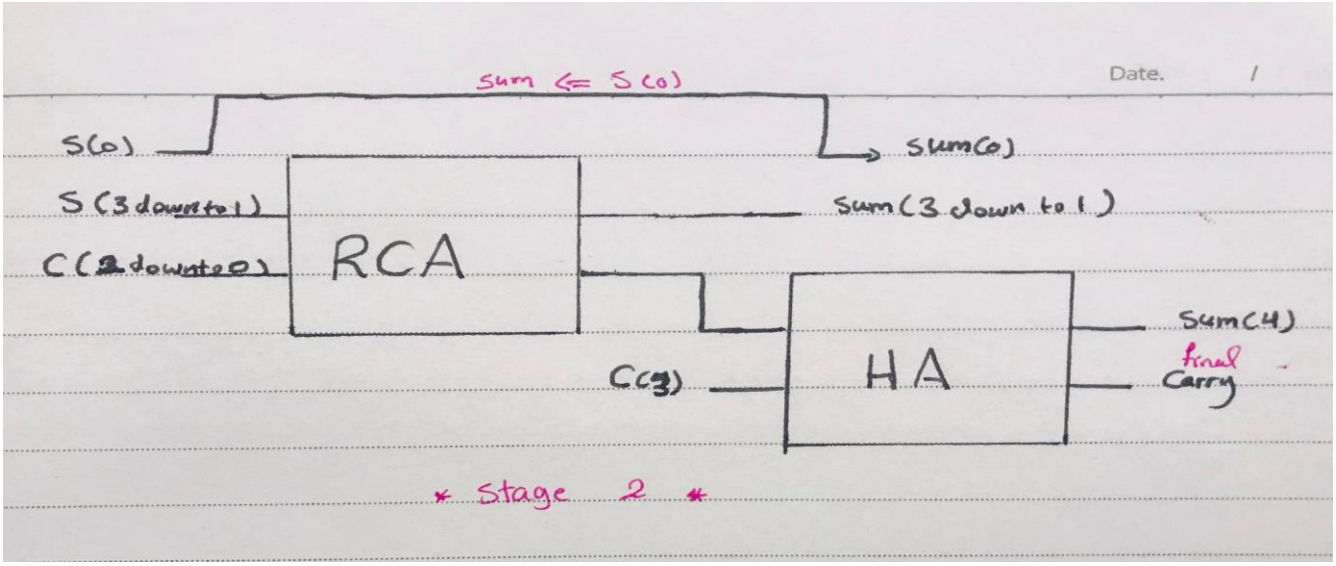
Step 2 and 3 and 4 can do it by using RCA_3bit

(RCA_3bit contains 3FullAdders)

5.Then we will use HalfAdder to sum the c3(from previous step) and the last bit in carry c(3)

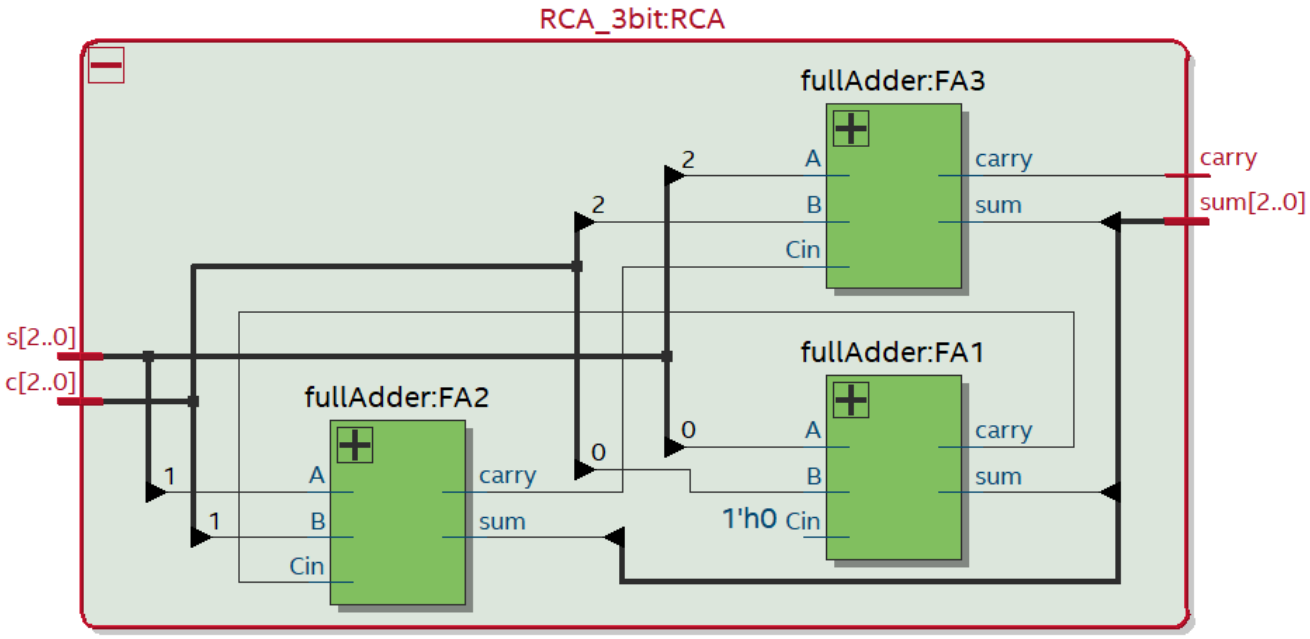
The output s from HA is sum(4)

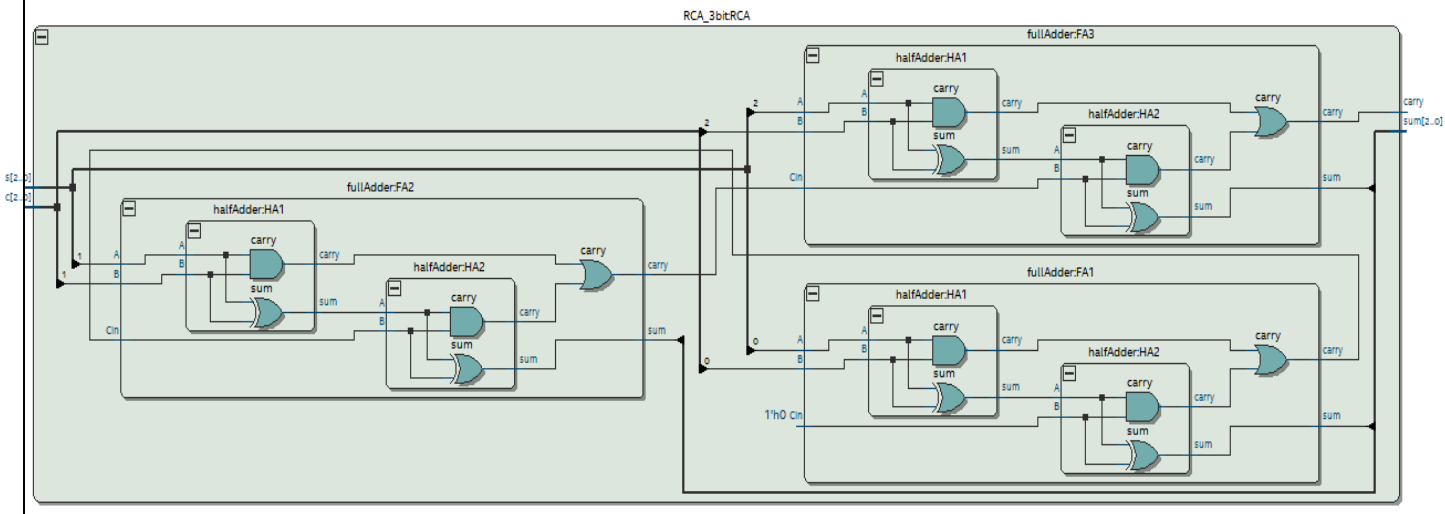
And the carry is the final carry



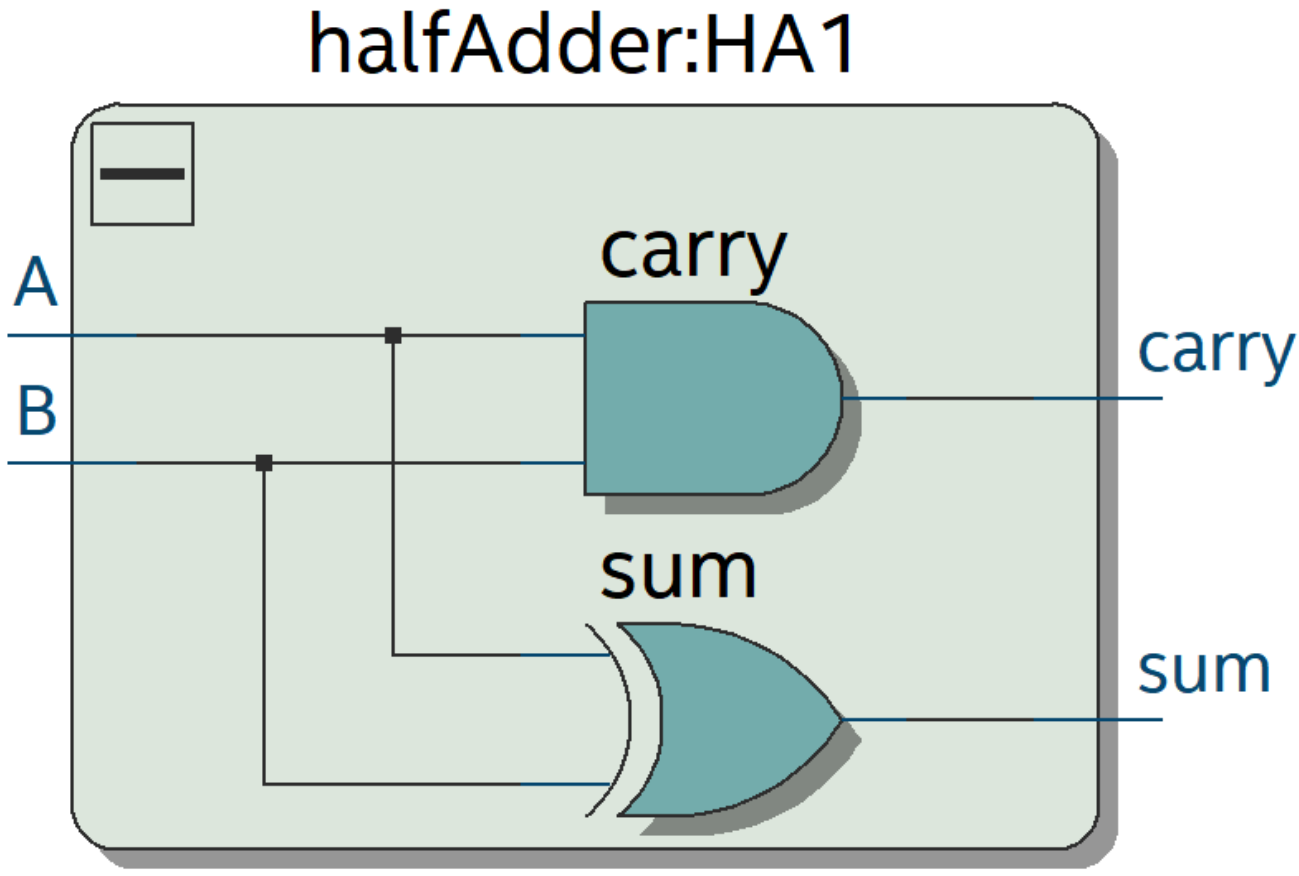
- InCoding:

1.implement RCA_3bit Entity by using 3FullAdder

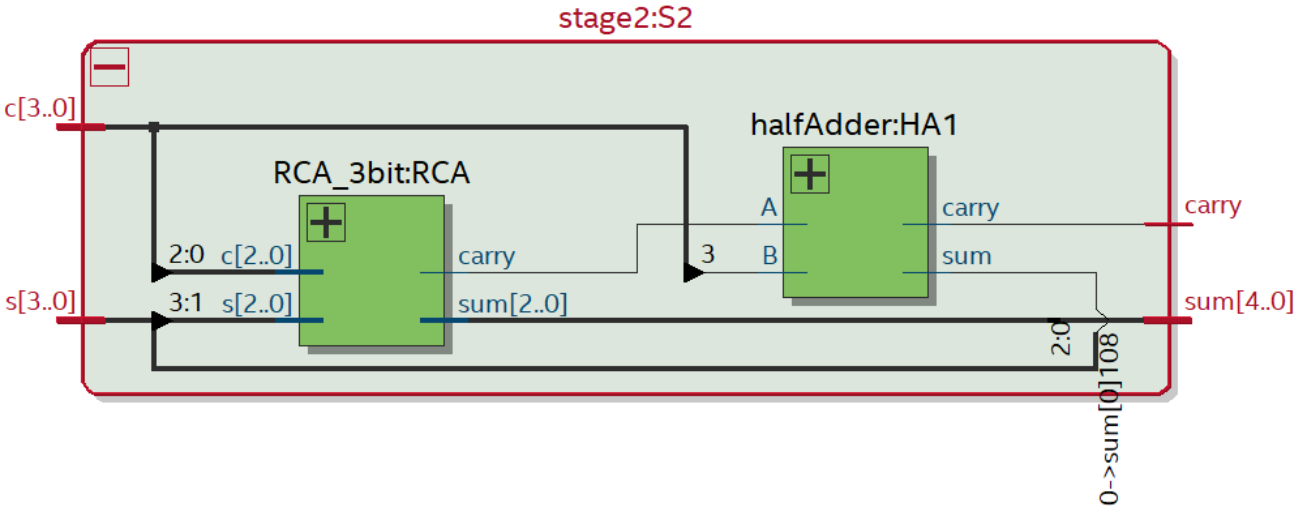


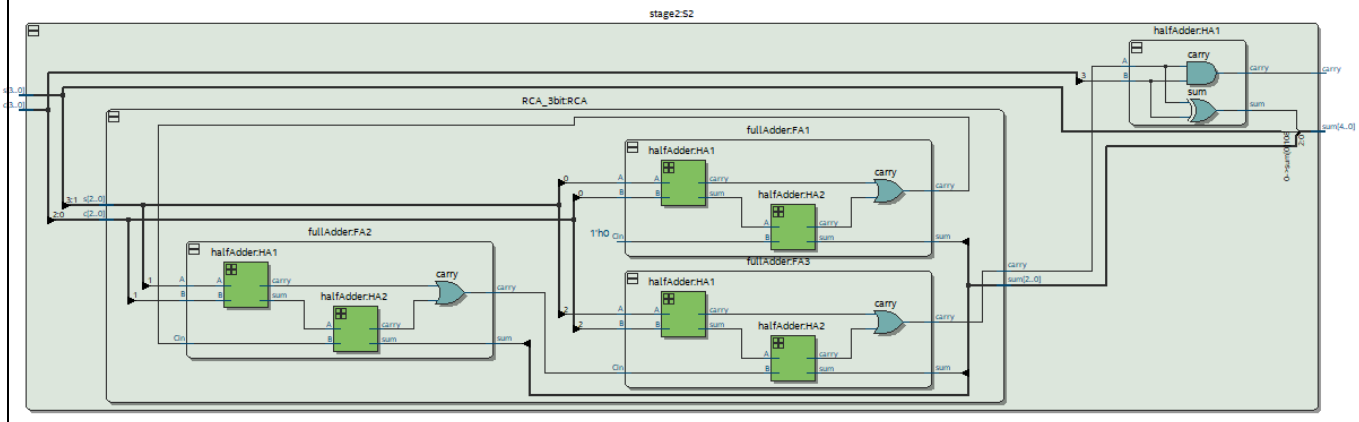


2.implement HalfAdder:



3.implement stage2 by using RCA and HA:





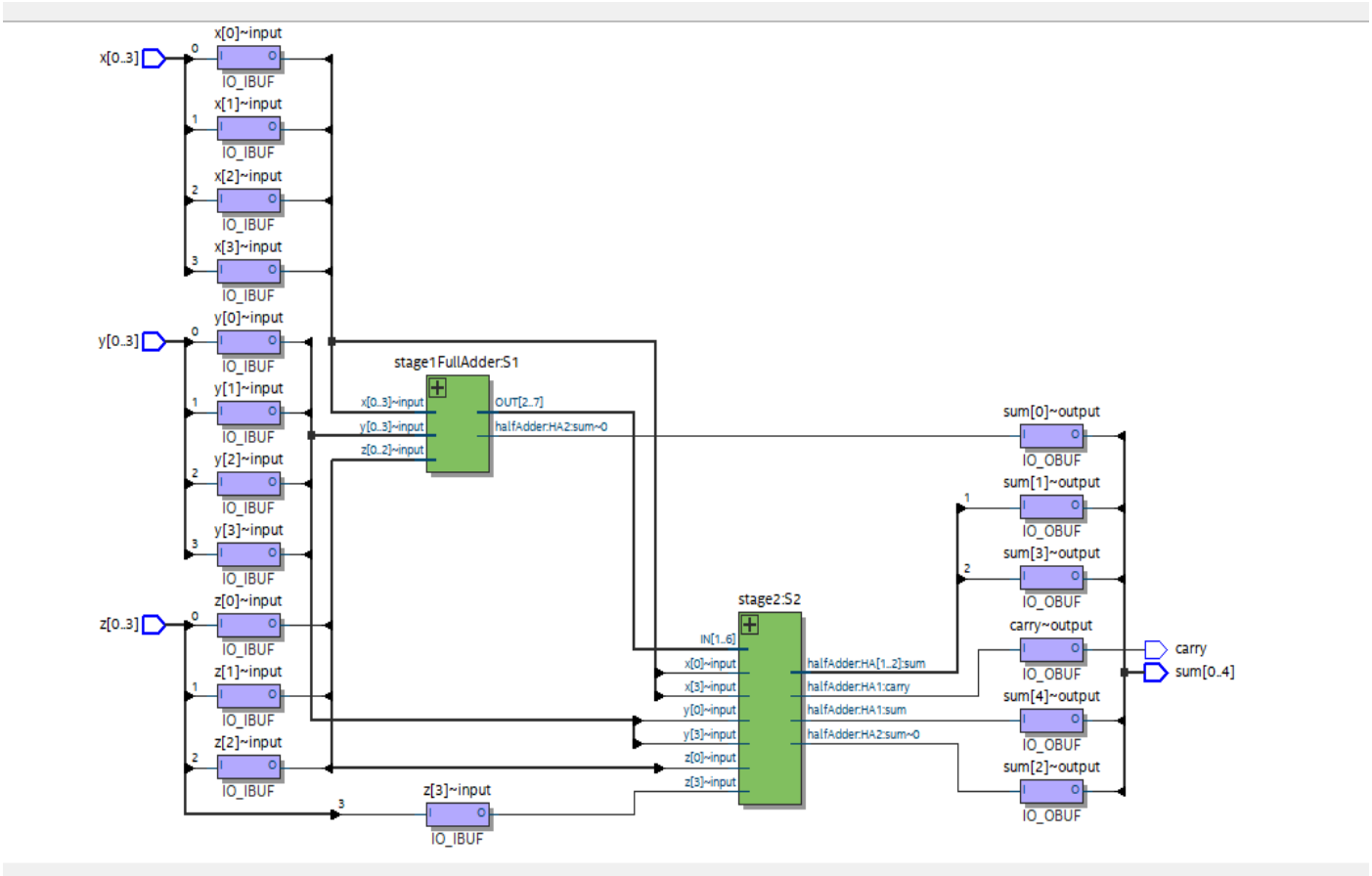
Stage2 is done

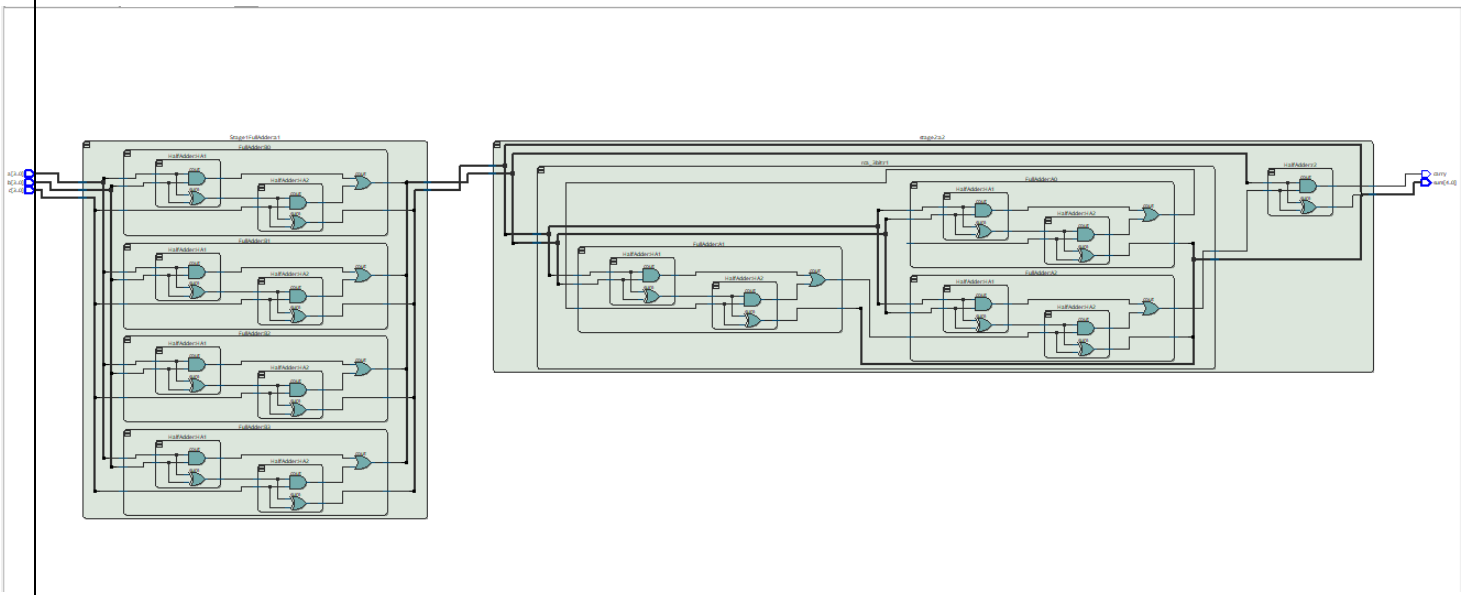
Now concatenate stage1 and stage2 in one project:

1.implement stage1 as component

2.implement stage2 as component

3.implemant 2signals to link first stage with second stage





In our Quartus file we have 6Entites:

1.HA

2.FA

3.RCA

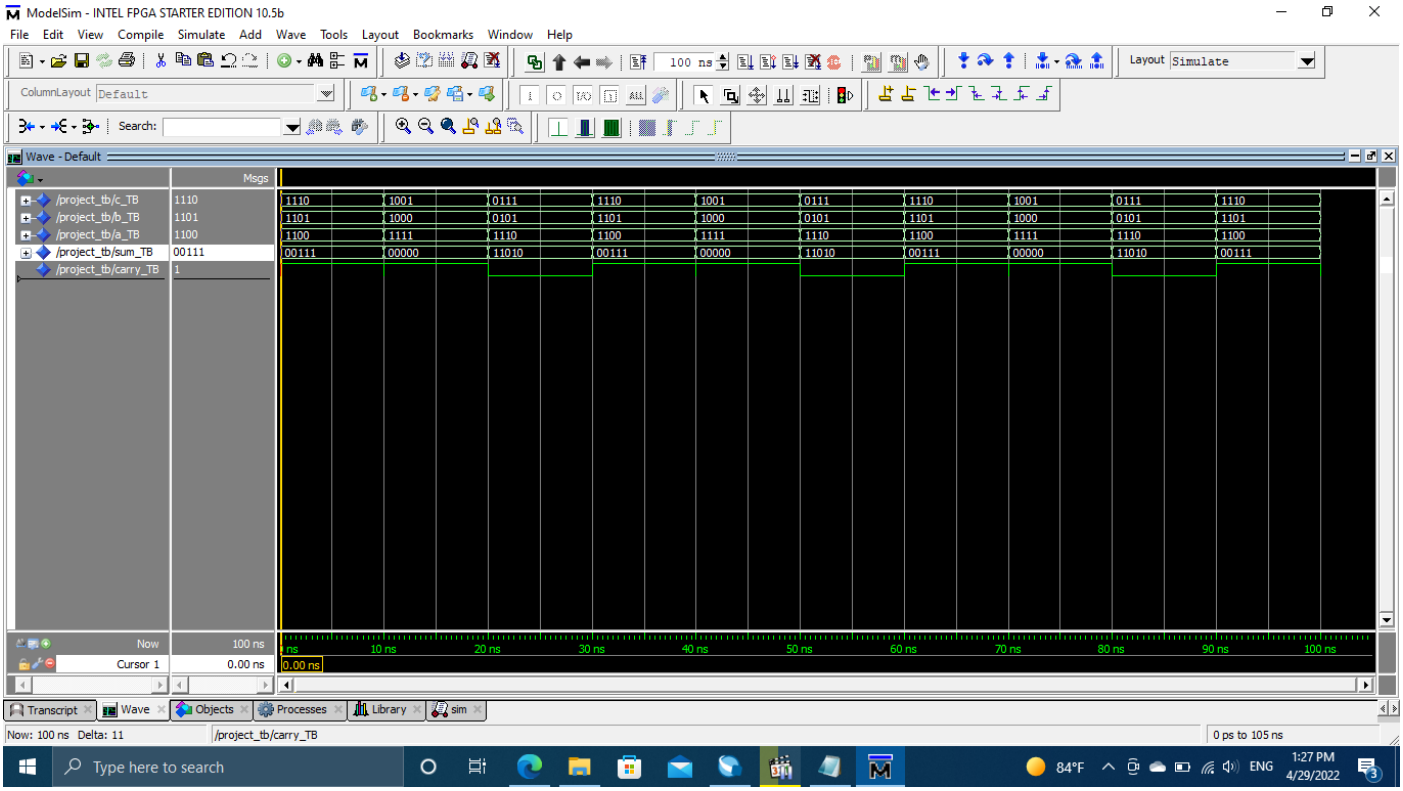
4.stage1(4fullAdder)

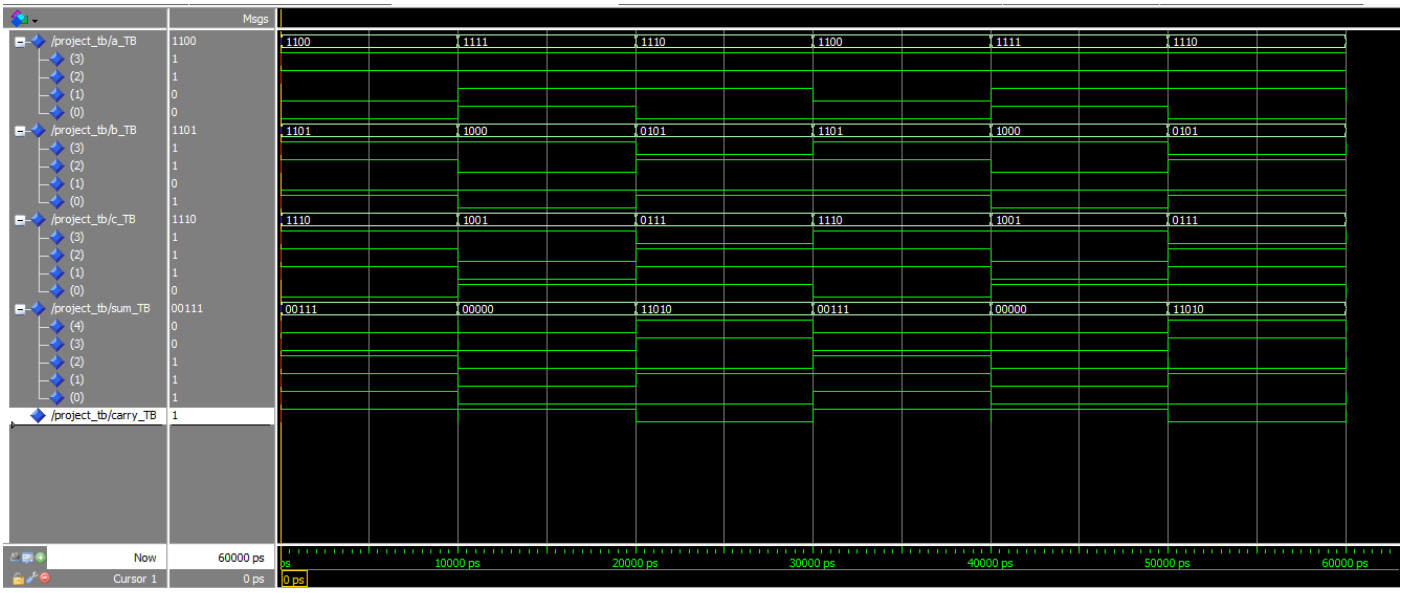
5.stage2(RCA and HA)

6.the Project(concatenate stage1 and stage2)final Results

And have Test bench file, and testing 3 tuples

*Wave:





DONE PROJECT

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