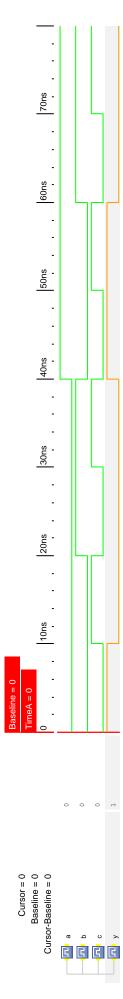# SillyFunction USF.EE.Dobariya

This is a SillyFunction design with three inputs a, b, and c with an output y.

This is a combinational circuit using blocking assignments, AND, OR gates, and Inverters.

Here, we get combinational output after gate operations in the order NOT, AND, and OR for this design code.

Cursor = 0
Baseline = 0
Cursor-Baseline = 0

Baseline = 0
TimeA = 0

| | 10ns | 20ns | 30ns | 40ns | 50ns | 60ns | 70ns |

a   0
b   0
c   0
y   1