ControlPath.Group2.USF.EE

Control path controls the complete state machine transition and synchronises the data path. It is driven by the same clock input and an asynchronous reset signal. 'Zi' is responsible for the transition of the states 'Zi' is the output from the counter i.e., it acts as a flag that is active for every counter cycle. Further, 'op' is concatenation of (Dop,Aop,Qop&Sop) which controls the particular that is active at a particulate state. When reset is high, the circuit is set to default state where, ready is activated to '1' and op is set to 0. in the next clock cycle, op is set to start the multiplication operation and moves from state SM and then to SF.