WSM32_USF.EE.Group2.

The design is for a Word Serial Multiplier of 32 bit inputs. Which is same as World Serial Multiplier of 8-bit. The multiplier has 2 inputs DD and QQ which are initially store in the respective registers. It The data flow in the registers are controlled and synchronised via a counter with output 'zi' which inturn controls the state transitions. The output is delayed as it undergoes serial addition In this we get delayed output 223B CDB9 A1BF 749A at 69 ns, which is the multiplication of 5311AB12 and 698011A5.