A_RTL_USF.EE.Group 2.Dobariya

The design describes A-Register, the more-significant half of the product register. It has 2 inputs with a clock. One is F which is the output of the ALU and performs conditional operation and Another is 2-bit Aop which is [5:4] bit of op. For "00" value of Aop output A stays the same, for "01", load arithmetically shifted right operation has been done. For "10","11" the output A is zero. This output is given to ALU and it also stored in concenated P = AQ.