Q_RTL_USF.EE_Group2

The design describes Q-Register, the multiplier Register. Here, it has 4 inputs with a clock. One is multiplier QQ. Second input is 2-bit Qop which is [3:2] bits of op
It has q[-1] as a input with predefined value '0'. And fourth input is shift right logic[F0] to perform the shift right operation. In this, output stays same for the "00" value of Qop. When it is "01" and F0 is high it performs shift right logic operation. And at "10","11" it loads the value .Here, the input is there at 5 ns but output starts at 7.5 ns because of rising edge of the clock.