WSM8x8.Group2.USF.EE

The design describes a Word Serial Multiplier of 8 bit inputs. The multiplier has 2 inputs DD and QQ which are initially stored in the respective registers. The MSB bit of product output is first stored in A-register.
The dataflow in the registers are controlled and synchronised via a counter with output 'zi' which inturn controls the stat transitions. Due to this, the output is delayed as it undergoes serial addition.
The counter is used to wait until all serial additions are complete and when zi signal is high, we get the output for the multiplication, The next operation starts once 'st'(start) signal is '0' i.e., rdy flag is '1'.