Verilog Experiment - Part 1

Experiment 1 – Schematic Capture for 7 Segment Display

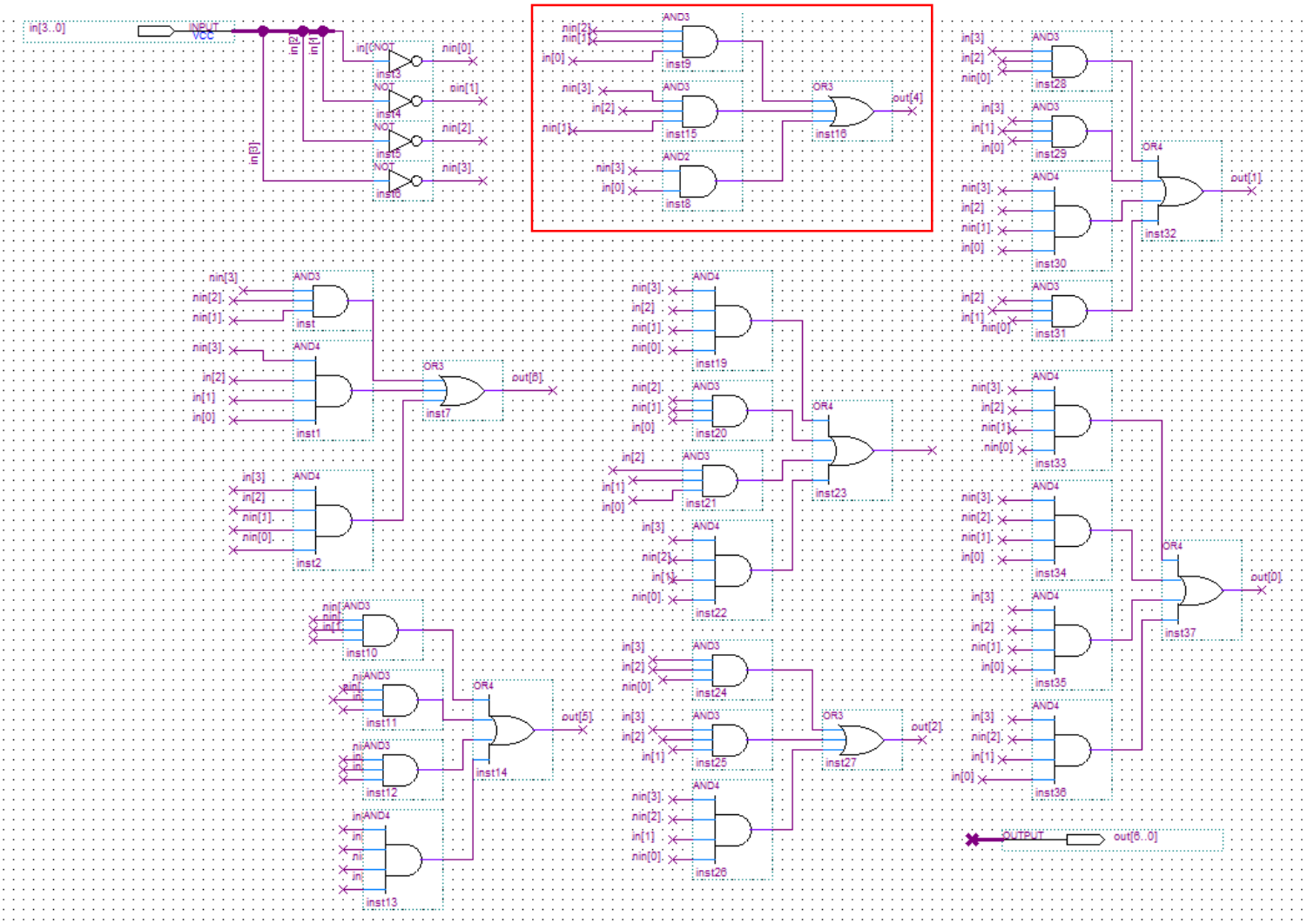
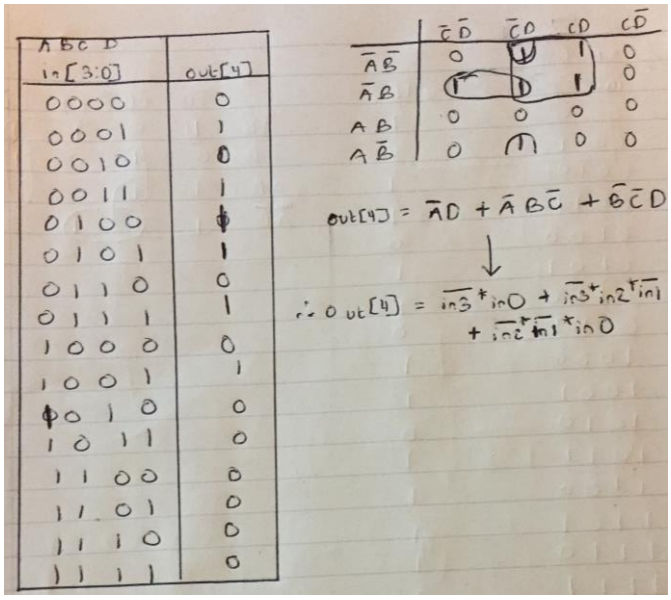


Figure 1 - Entire Schematic Diagram for 7-Segment Decoder



On the left is the derivation for output 4 of the 7-Segment decoder which is boxed in red in Figure 1.

	Input Port	Output Port	RR	RF	FR	FF
1	SW[0]	HEX0[0]	8.196	8.204	8.767	8.785
2	SW[0]	HEX0[1]	8.411	8.635	8.977	9.236
3	SW[0]	HEX0[2]		8.586	9.030	
4	SW[0]	HEX0[4]	8.407			9.232
5	SW[0]	HEX0[5]	8.618			9.368
6	SW[0]	HEX0[6]	8.250	8.410	8.816	9.011
7	SW[1]	HEX0[0]	7.769	7.790	8.316	8.314
8	SW[1]	HEX0[1]	8.112	8.275	8.654	8.789
9	SW[1]	HEX0[2]	8.033			8.696
10	SW[1]	HEX0[4]		8.271	8.651	
11	SW[1]	HEX0[5]	8.192	8.374	8.738	8.897
12	SW[1]	HEX0[6]	7.950	8.049	8.494	8.565
13	SW[2]	HEX0[0]	8.487	8.553	9.090	9.215
14	SW[2]	HEX0[1]	8.873			9.627
15	SW[2]	HEX0[2]	8.747	8.932	9.350	9.594
16	SW[2]	HEX0[4]	8.859	9.019	9.463	9.611
17	SW[2]	HEX0[5]	8.873	9.100	9.473	9.759
18	SW[2]	HEX0[6]	8.700	8.796	9.302	9.386
19	SW[3]	HEX0[0]	7.962	8.000	8.694	8.680
20	SW[3]	HEX0[1]	8.358	8.556	8.847	9.006
21	SW[3]	HEX0[2]	8.223	8.380	8.955	9.060
22	SW[3]	HEX0[4]		8.540	8.831	
23	SW[3]	HEX0[5]	8.345	8.544	9.075	9.222
24	SW[3]	HEX0[6]	8.180	8.314	8.669	8.764

Figure 2A – Slow 0C 1100mv Model

	Input Port	Output Port	RR	RF	FR	FF
1	SW[0]	HEX0[0]	8.651	8.673	9.140	9.170
2	SW[0]	HEX0[1]	8.895	9.147	9.416	9.648
3	SW[0]	HEX0[2]		9.082	9.407	
4	SW[0]	HEX0[4]	8.902			9.648
5	SW[0]	HEX0[5]	9.090			9.786
6	SW[0]	HEX0[6]	8.741	8.912	9.268	9.419
7	SW[1]	HEX0[0]	8.226	8.255	8.691	8.701
8	SW[1]	HEX0[1]	8.570	8.761	9.038	9.205
9	SW[1]	HEX0[2]	8.493			9.112
10	SW[1]	HEX0[4]		8.759	9.050	
11	SW[1]	HEX0[5]	8.667	8.873	9.136	9.323
12	SW[1]	HEX0[6]	8.422	8.531	8.889	8.974
13	SW[2]	HEX0[0]	8.987	9.059	9.480	9.606
14	SW[2]	HEX0[1]	9.360			10.044
15	SW[2]	HEX0[2]	9.249	9.464	9.743	10.011
16	SW[2]	HEX0[4]	9.358	9.535	9.860	10.027
17	SW[2]	HEX0[5]	9.384	9.633	9.875	10.177
18	SW[2]	HEX0[6]	9.195	9.304	9.696	9.795
19	SW[3]	HEX0[0]	8.486	8.529	9.093	9.088
20	SW[3]	HEX0[1]	8.883	9.104	9.256	9.443
21	SW[3]	HEX0[2]	8.750	8.935	9.357	9.494
22	SW[3]	HEX0[4]		9.085	9.252	
23	SW[3]	HEX0[5]	8.879	9.098	9.485	9.656
24	SW[3]	HEX0[6]	8.710	8.850	9.084	9.189

Figure 2B – Slow 85C 1100mv Model

Figure 2 shows the worst-case input to output propagation delays for various combinations of rise and fall times and two temperature extremes.

RR – input rising, output rising

RF – input rising, output falling

FR – input falling, output rising

FF – output falling, input falling

There are some gaps in the table for certain combinations due to some of the circuit logic. For example, a buffer has either RR or FF and cannot have FR or RF. On the other hand, an inverter can have RF or FR and cannot have RR or FF.

There are propagation delays due to parasitic capacitance in the transistors as it takes time for them to charge and discharge.

Propagation delay can be approximated using the RC constant. So at higher temperatures, the resistance increases, so RC increases which relates to a higher propagation delay at higher temperatures as shown in the above figure. Temperature also affects material properties such as threshold voltage and other parameters which also affect propagation delay time.

Flow Summary	
Flow Status	Successful - Fri Nov 18 11:08:50 2016
Quartus Prime Version	16.0.0 Build 211 04/27/2016 SJ Standard Edition
Revision Name	ex1_top
Top-level Entity Name	ex1_top
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	4 / 32,070 (< 1 %)
Total registers	0
Total pins	11 / 457 (2 %)
Total virtual pins	0
Total block memory bits	0 / 4,065,280 (0 %)
Total DSP Blocks	0 / 87 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

Figure 3 – Compilation Report

Figure 3 shows that only a small number of resources are used. In this case 4 ALMs and 11 pins