



Suchintita Ghosh

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Education

B.Tech ECE, **GPA: 9.33**
HSC **95.8%**
SSC **97.2%**

VIT Vellore, Exp. 2026
DAV Public School, WB 2021
Shamayita Convent School, WB 2019

Technical Skills

Design/Verification: Verilog, MATLAB, FPGA, Simulink, Cadence

Embedded Systems: Embedded C, Assembly Language, Interrupts, Timer Programming

Communication Protocols: UART, SPI, I2C

Languages: C/C++, Java, Python, R

Projects

RISCV RV32I Design and SPI Integration

github.com/RTLDesign

Quartus Prime

- Implemented and benchmarked three RISC-V microarchitectures—Single-cycle, Multicycle, and Pipelined—using Verilog.
- Designed a unified testbench framework to compare cycle counts, register/memory outputs, and instruction execution patterns across architectures.
- Integrated a custom SPI Master IP core into the pipelined design as a memory-mapped peripheral.
- Verified end-to-end SPI data transfer through instruction-driven transactions and waveform validation.

FIR and IIR Filter Design and Implementation

github.com/RTLDesign

MATLAB, Quartus Prime, Platform Designer (Qsys), Eclipse IDE, Altera DE2-115 (FPGA)

- Designed filters in MATLAB, converted to fixed-point C for Nios II processor.
- Compared performance using FFT, memory, delay, and execution time.

Op Amp Design

github.com/RTLDesign

Cadence

- Designed and optimized op-amp circuits, extracted gain, bandwidth, and stability.

Smart Driver Fatigue Detection System

github.com/Embed

- Developed a driver monitoring system with real-time microsleep alerts.

Research

Approximate Arithmetic with Stochastic Bitstreams (-ongoing)

github.com/RTLDesign

- Exploring stochastic computing for power-efficient logic circuit design.

Certifications

Introduction to Electronics, Georgia Tech (**90.88%**)

coursera.org/electronics

Achievements and Extracurricular

Merit Scholarship Award for academic year 2022–23

Anchored the Inauguration Ceremony of Rotaract Club in 2025.

Core member of IEEE-CS for year 2023-24.