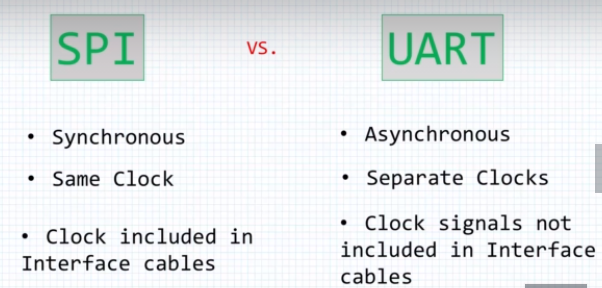
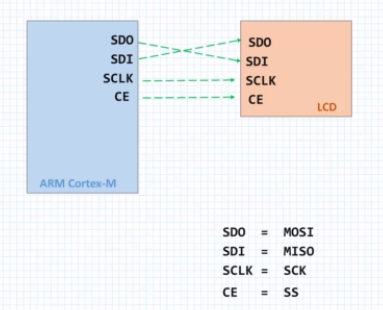
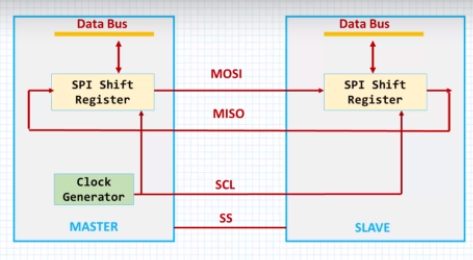
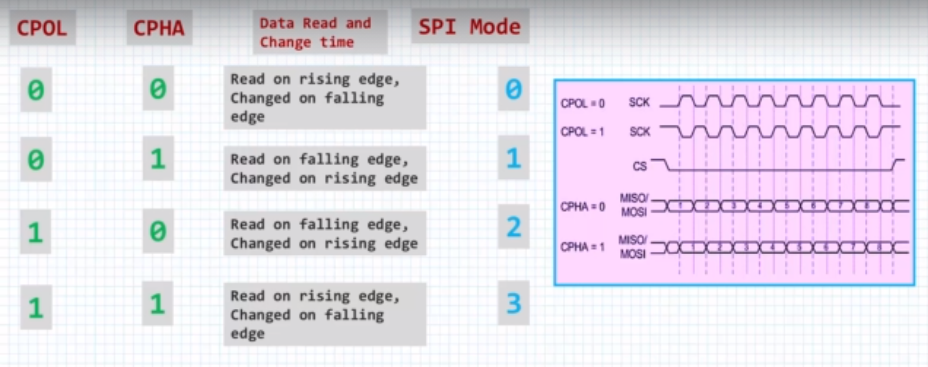
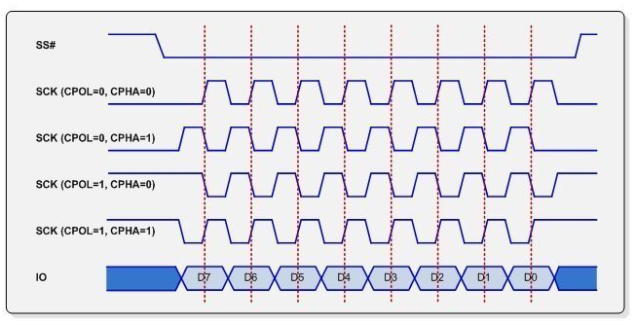
SPI – Serial Peripheral Interface

1. Also known as Synchronous Serial Interface (SSI)
2. Devices needs to be configured as Master or Slave
3. 
4. In UART, devices with +/-5% of Baud Rate can communicate with each other.
5. 
6. In the above image 2 PINs are used data transfer
7. There is another popular type of communication called **3 wire SPI**
   1. In this there is only 1 wires for data instead of 2
   2. A device should support 3 wire SPI internally, to configure it to work in this mode
8. 
9. There is two shift registers in both master and slave
10. Clock for both of the shift register are generated by the clock generator (SCL) , this can be configured to Falling or Rising Edge triggered
11. Serial OUT of the Master is connected to the Serial IN of the slave’s SPI shift register, similarly the Serial OUT of the slave is connected to the Serial IN of the Master’s SPI shift register
12. Shift registers are 8bit long, after clock pulse, the contents of the Shift registers are interchanged
13. If the Master wants to send the data to slave, the master needs to place the data in the shift register and generate 8 clock pulses, then the data will be transferred to the slave device, same cycle of process happens of the slave wants to send the data to the master
14. 
15. CPOL- clock polarity
16. CPHA- clock phase
17. CPOL =0 means idle value of the clock is zero
18. CPOL =1 means idle value of the clock in one
19. CPHA =0 means sample data on the leading or the first clock edge
20. CPHA=1 means sample data on the trailing or the second clock edge
21. 
22. SPI Modes:
    1. Mode 1: climbing mountain aka Raising edge from idle mode
    2. Mode 2: descend mountain aka Falling edge to idle mode
    3. Mode 3: descend cave aka falling from idle mode
    4. Mode 4: climb cave aka raise to idle mode