ABHIRAMI RAJENDIRAN
M.Tech Student
VLSI Design
VIT CHENNAI

9445896233
abhirami.dew@gmail.com
New No 24, Jawahar Street End
KK Nagar West, Chennai –TN

Academic Details:

Year	Degree	Institute	Marks
2017 – Present	M.Tech , VLSI Design	VIT Chennai	CGPA 8.58
2010-2014	B.Tech ECE	SRM University	CGPA 8.34
2010	CBSE - AISSCE (Class 12)	Kendriya Vidyalaya	71%
2008	CBSE - AISSE (Class 10)	SBSM Girls Higher Secondary School	88.2%

Objective: To pursue a career in the VLSI industry with the engineering skills I have acquired for progress in cutting edge research and technology.

Internships

ELECTRONICS CORPORATION OF INDIA LTD | INTERN

Learnt about various equipment manufacturing and fabrication processes in the electronics hub of the country and in depth exploration of PLC and their uses in the instruments manufactured.

NUCLEAR FUEL CORPORATION | DEPARTMENT OF ATOMIC ENERGY | INTERN

Learnt and observed the various furnaces operating there and equipments used in steel plant. Designed a model SCADA virtual system for their furnace using Cimplicity software.

DEFENCE RESEARCH AND DEVELOPMENT ORGANIZATION | SUMMER INTERN

Learnt about various equipments, missiles, weapons, instruments. Studied about missile propulsion systems and their advantages, drawbacks and improvisation with leading scientists.

ACI SYSTEMS PVT LTD | FULL TIME INTERN

Worked on automatic number plate recognition system. Designed a NPRS for four wheelers using Matlab coding and achieved 60 % correlated output.

Major Projects

Review of Digital Filter Banks for Hearing Aid System on Chip Application | Research Based Project

Compared various digital filter banks on the basis of their complexity, time delay and filter coefficients. Concluded about the octave filter bank being the best option for hearing aid application. Currently working on the filter bank synthesis and reduction of time delay.

Implementation of Elliptic Curve Cryptography in GF (2^163) - Network Security Based | Research Based Project

ECC algorithm implementation is done in Verilog. This algorithm is used for encryption and data security purposes in various platforms.

FPGA Hardware Implementation of Low power Carry Select Adder | Research Based Project

The CSA design can be architecturally modified to reduce the delay. Since adders form a major part of any arithmetic network, optimization of the same is highly useful for various ALU designs.

Design of Full Adder circuits for Low power Digital IC Design Applications | Research Based Project

CMOS 32nm and FINFET 32nm technology node implementation of various adiabatic logic families in Cadence –Virtuoso.

Mini Projects

Design of Automatic LPG Stove for energy conservation Applications | Innovative Project

Designed a mini circuit for automatic functioning of the LPG stove. With the idea taking a deep root in my mind, I plan to integrate this in the form an Analog IC with various sensors like gas, temperature and pressure integrated into one piece.

ALU Design | ASIC Design Project

Designed an 8 bit ALU which performs basic operations using Verilog. Simulated the design using NCLAUNCH, Synthesized the code in CADENCE –RC, designed the layout in CADENCE –ENCOUNTER, performed timing analysis, placement, routing and completed the design with the extraction of GDS-2 file.

Image Processing Filter Bank Application | VLSI DSP Project

Designing a filter bank for better image analysis using decimation, interpolation, DCT, wavelet Transform.

Scholastic Achievements:

• Outstanding Achiever Award in 2010 -2014 batch at SRM University, Chennai

• 1st in KV Regional Science Exhibition and represented south zone at the 36th Jawaharlal Nehru national science Exhibition held in Lucknow for - AUTOMATIC LPG GAS STOVE DESIGN

• Winner of App life idea – Open source idea platform in Wipro's nationwide event

• All India Rank -1 in AIISH (All India Institute of Speech and Hearing) Mysore Selection Process

• All India Rank -10 in Indian Institute of Remote Sensing Selection Process

• VLSI MAKETHON- 2017 Winner, cash prize of Rs 13000

• Merit certificate for obtaining distinction and best speaker at SBSM Girls High school

• Certificate of Appreciation from Dr Ambedkar Law University for participating in a Seminar on Environment protection and Initiatives.

• Delivered a Guest lecture at a seminar conducted by Central Marine Fisheries Research Institute, ICAR. Delivered a Guest lecture at a seminar conducted by GAIA International Organization.

• Invited to join Environmental research as a Researcher by Dr P Nammalvar Rajan, Chairman GAIA International Organization.

• Shortlisted for Synopsys IC Design Contest across India and underwent 3 day training program at Synopsys Bangalore

---

Conferences & Workshops Attended

• THINK Nano 2017 conference – IISC Bangalore – Poster Presentation Event

• System Design with FPGA workshop – VIT Chennai

• System Verilog and SOC workshop – VIT Chennai

• Mentor Graphics workshop –VIT Chennai

Relevant Courses:

Digital IC design , Analog IC design , Digital design with FPGA , ASIC design , IC technology ,Advanced Computer Arithmetic, Embedded systems , low power IC design , VLSI testing and testability, VLSI DSP, Remote sensing, EDC, Physics of VLSI ,CAD for VLSI

Technical Skills:

Programming Languages: C, Verilog, (learning Scripting –PERL, System Verilog, TCL in current Semester)

Software Packages: Matlab, Xilinx, Cimplicity –SCADA software; Platforms: Linux and Windows.

EDA Tools: Cadence- [NCLAUNCH, SIMVISION, ENCOUNTER, RC], Synopsys – TCAD, Tanner, LTSpice

---

Extra-curricular & Sports Achievements:

• 3rd in Chennai cluster Chess meet ; represented my school at the KV Regional sports meet and part of University team throughout from 2010-present

• 1st in throw ball and member of University team at SRM.

• 1st in Flower Decoration event, All India Drawing competition

• Best poster design award at SRM University

• 2nd in map marking event, presentation event called PREZENTIM

• 3rd in violin competition held at Kalyani natya kalalaya