GOVERNMENT COLLEGE OF ENGINEERING & CERAMIC TECHNOLOGY
AN AUTONOMOUS INSTITUTE
AFFILIATED TO MAKAUT (FORMELY KNOWN AS WBUT)

Theory / B. Tech. / CSE / SEM - III / Code – CS 302 / 2018-19

Paper Name: Digital Logic

Full Marks: 75 **Time Allotted: 3 hours**

The figures in the margin indicate full marks. Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
[MCQ Type Questions][Compulsory]

1. Choose the correct alternative of the following questions. Answer all questions. **10 x 1 = 10**

i) The memory, which is ultraviolet erasable and electrically programmable is

a) RAM b) EEROM

c) EPROM d) PROM

ii) Which of the following is reflected code ?

a) 8421 b) Excess-3

c) Gray d) ASCII

iii) The minimum number of 2X1 multiplexer required to generate a 2 input AND gate is

a) 1 b) 2

c) 4 d) 5

iv) The race around condition does not occur in Flip Flop

a) J-K b) T

c) Master slave d) none

v) Identify the carry expression of full adder circuit

a) X'Y+ZX' b)XY+XZ+ZX

c) X'Y+XZ'+ZX d) X'Y'+X'Z+ZX

vi) The maxterm corresponding to decimal 9 is

a) $AB'C'D$ b) $A+B'+C'+D$

c) $A'+B+C+D'$ d) $A'BC'D'$

vii) The number of J-K flip flops required to design a mod-16 ripple counter is

a) 5 b) 3

c) 4 d)10

viii) A two input Ex-OR gate can be used as an inverter when one of its input is kept at logic

a) 0 b) 1

c) either 0 or 1 d) none of these

ix) A message is 010101. Even parity generator is used. So the parity bit added to the message bits is

a) 0 b) 1

c) 0 & 1 d) none of these

x) Latch is a memory cell of

a) 1 bit b) 2 bits

c) 3 bits d) none of these

GROUP – B
[Short Answer Type Questions]
Answer any *four* of the following

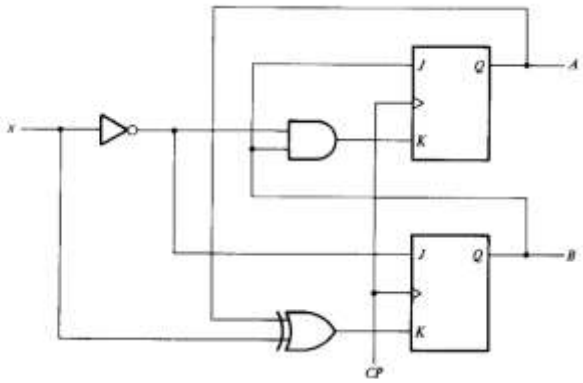
4 x 5 = 20

2. Why is multiplexer called data selector ? Implement a Full adder with two 4X1 multiplexers. Show block diagram only. [5]
3. What is don't care? Minimize following expression using K-Map
   F (A, B, C,D) =∑ m (3,4,5,7,9,13,14,15) +∑d(0,2,8) [5]
4. a) Implement Y= $\overline{AB}$ +A+ $\overline{(B+C)}$ using NAND gates only.
   b) Given the two binary numbers X=1010100 , Y=1000011 perform the subtraction X-Y using 2's complement. [3+2]
5. Do the following conversion using excitation table: S-R Flip Flop to J-K Flip Flop. [5]
6. a) Design 4 × 16 decoder using 3 × 8 decoders.
   b) Implement 2-input XOR function using minimum number of 2-input NAND gates. [3+2]
7. Draw the block diagram of a 4 bit shift register and draw its response for a sequence of bits presented at the input 11010.

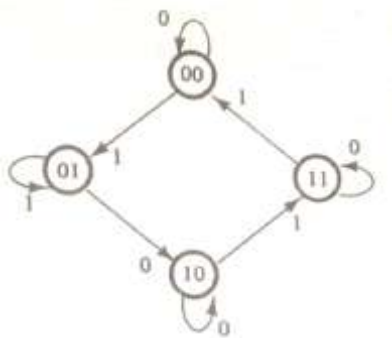
GROUP – C
[Long Answer Type Questions]
Answer any *three* of the following

3 x 15 = 45

8. a) Design and implement a 1 bit comparator using logic gates.
   b) A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is zero otherwise. Design a 3-input majority circuit by finding its truth table.
   c) Implement a full adder with half adders and a logic gate. [5+5+5]
9. a) Distinguish between ROM, PLA as elements realizing Boolean function.
   b) A combinational circuit is defined by the functions
   $F_1(A,B,C) = \sum (3,5,6,7)$ $F_2(A,B,C) = \sum (0,2,4,7)$
   Implement the circuit with a PLA having three inputs, four product terms, and two outputs.
   c) Draw a logic diagram of master-slave JK f/f. Why is it called so ? [7 + 5 + 3]
10. a) An 8 : 1 MUX has inputs A, B, C connected to select lines S_2, S_1, S_0 respectively. The data inputs I_0 to I_7 are connected as, $I_1 = I_2 = I_7 = 0$, $I_3 = I_5 = 1$, $I_0 = I_4 = D$, $I_6 = D^I$. Determine the Boolean expression the MUX output.
    b) Design a combinational circuit with three inputs and one output. The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise.
    c) Find the expression of difference and borrow for a full subtractor circuit using truth table. [5+5+5]
11. a) For the sequential circuit shown in the following figure find the state table and state diagram.



b) For the clocked sequential circuit whose state diagram is given below, derive the excitation table. From the table design the circuit using JK flip flop. [(4+4)+(2+5)]



12. a) Define the following parameters of IC digital logic families:
(i)Fan out (ii) Propagation delay (iii) Noise Margin
Use the parameters to compare different IC logic families.
b) The truth table given below specifies a combinational circuit with two inputs (A_1,A_0) and two outputs (F_1,F_2): [(6+3)+6]

A_1	A_0	F_1	F_2
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	0

Implement the circuit with 4X2 ROM.

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