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5E3251-S

B. Tech. (Sem. V) (Main) Examination, December - 2011
Computer Science
5CS1 Computer Architecture (Common for Computer & IT)

Time : **3** Hours]

[Maximum Marks : **80**
[Min. Passing Marks : **24**

Instructions to Candidates :

Attempt any five questions selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. *(Mentioned in form No. 205)*

1. _____NIL_____   2. _____NIL_____

UNIT - I

1   (a)   Explain the following terms with reference to non Von-Neamann machines./

   (i)   SISD

   (ii)   SIMD

   (iii) MISD

   (iv)   MIMD

8

   (b)   A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

   (i)   How many selection input are there in each multiplexers ?

   (ii)   What size of multiplexer are needed ?

   (iii) How many multiplexer are there in the bus ?

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OR

1. (a) Draw the block diagram for the hardware that implements

   t + pq : A ← A+B

   where A and B are two n-bit resisters and t, p and q are control variables show the logic gate for the control function.

   8

   (b) Design a N-bit combinational circuit decrementer using four full-adder circuits.

   8

UNIT - II

2. Write a program to evaluate the arithmetic statement :

$$X = \frac{A - B + C * (D * E - F)}{G + H * K}$$

   (i) Using a general register computer with three address instruction.

   (ii) Using a general register computer with two address instruction.

   (iii) Using an accumulator type computer with one address instructions

   (iv) Using a stack organized computer with zero-address operation instructions.

   16

OR

2. (a) The memory unit of a computer has 256 K words of 32 bit each. The computer has an instruction format with four field : an operation code field, a mode field to specity one of seven addressing modes, a register address field to specify one of 60 processor registers and a memory address. Specify the instruction format and the number of bit in each field if the instruction is in one memory word.

   10

   (b) A computer has 32-bit instruction and 12-bit addresses. If there are 250 two address instruction, how many one address instruction can be formulated ?

   6

UNIT - III

3   (a) Derive an algorithm in flowchart term for adding and subtracting two fixed-point binary numbers when negative numbers are in signed-is compliment representation.

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(b) Design an array multiplier that multiplies two 4-bit number. Use AND gates and binary address.

8

OR

3   (a) Show that when we multiply two n-digit number in base r no overflow occurs. rtuonline.com
The multiplication gives a product of 2nd digits in length.

8

(b) Derive an algorithm in flow chart form for the non restoring method of fixed-point binary division.

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UNIT - IV

4   (a) Construct a memory system having static 1K×4 RAM. How many such RAM's will be required to
(i)   construct 1K×8 RAM bank ?
(ii) 4K × 4 RAM memory bank ? Show the block diagram and the address decoding circuit.

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(b) Write short note on : Virtual memory.

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OR

4   (a) An address space is specified by 24 bits and the corresponding memory space by 16 bits.
(i)   How many words are there in the address space ?
(ii) How many words are there in the memory space ?
(iii) If a page consists of 2K words, how many pages and block are there in the system ?

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(b) In a two level virtual memory, $t_{A1} = 10^{-7}$ S and $t_{A2} = 10^{-2}$ S. What must be the hit ratio H be in order for the access efficiency to be at least 90% of its maximum possible value ?

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UNIT - V

5   (a)   Design a parallel priority interrupt hardware for a system with eight interval sources.

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(b)   Why does DMA have priority over the CPU when both request a memory transfer ?

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OR

5   (a)   List the advantage and disadvantage with respect to program design complexity, IO bandwidth, and interface hardware costs for the following IO control methods.
(i)   programmed IO
(ii)   DMA
(iii) IOPs.

6

(b)   Why are the read and write control line in a DMA controller bidirectional ? Under what condition and for what purpose are they used as inputs ? Under what condition and for what purpose are they used as outputs ?

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