610404/610904

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B. Tech. VI - Sem. (Main) Exam., (Academic Session 2021- 2022)
Computer Science & Engineering
6CS4 – 04/6IT4-04 Computer Architecture and Organization
Common with CSE & IT

Time: 2½ Hours **Maximum Marks: 120**
Min. Passing Marks:

Instructions to Candidates:

Part – A: *Short answer questions (up to 25 words) 6 × 3 marks = 18 marks. Candidates have to answer **six** questions out of **ten.***

Part – B: *Analytical/Problem solving questions 3 × 10 marks = 30 marks. Candidates have to answer **three** questions out of **seven.***

Part – C: *Descriptive/Analytical/Problem Solving questions 3 × 24 marks = 72 marks. Candidates have to answer **three** questions out of **five.***

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

Q.1 Justify the following statement: The efficiency of Booth's multiplication algorithm is dependent on the operands.

Q.2 What is rounding? Explain with an example.

Q.3 What do you mean by locality of reference?

Q.4 Define instruction cycle. Name the steps.

Q.5 What do you mean by data path?

Q.6 Write down the steps for instruction fetch?

Q.7 Find out the number of gate delays for final carry and sum in a 16-bit carry look-ahead adder circuit.

Q.8 What are the disadvantages of direct mapping technique?

Q.9 Mention the components of a bit stage cell in a carry look-ahead circuit.

Q.10 A cache has a 95% hit ratio, an access time of 100 ns on a cache hit, and an access time of 800 ns on a cache misses. Compute the effective access time.

PART – B

Q.1 Write an assembly programs that can evaluate the expression X=(A*B+C*D)/(E-F) in a machine that supports -

(i) Two-address instruction format

(ii) One-address instruction format

Q.2 The following two signed numbers (negative numbers are represented using 2's compliment form are given. Find their product using Booth's algorithm -

A = (11011101); B = (11010111)

Q.3 Derive an expression for the average access time for a single-level cache memory system as well as for a two-level cache memory system.

Q.4 A memory system has a two-level cache memory. Their access time and hit ratio are given to be 15 ns and 45 ns respectively and 80% and 90% respectively. The main memory access time is given to be 200 ns. Assuming that 60% of the accesses are for read and main memory write accesses are 50% slower than read accesses. Find out the average access time. (Assume 200 ns is for memory read access)

Q.5 What do you mean by set associative mapping? With a neat diagram, explain its working principle.

Q.6 Draw the schematic diagram of the architecture of a single internal CPU, clearly showing the general purpose, special purpose registers and the data path.

Q.7 A memory system has 512K words each of 16-bits. The block size of cache is given as 4 words. Find out the number of bits in the TAG, BLOCK and WORD fields of a main memory address assuming that the mapping techniques is direct mapping. The cache memory has 2K words and it is word addressable.

PART – C

Q.1 Explain the state diagram of finite state machine for cache.

Q.2 A computer system has a main memory consisting of 1 M (220) 32-bit words. It also has an 8K words cache organized in the block-set-associative manner, with 2 blocks per set and 64 words per block. Suppose CPU generates the 20-bit Hexadecimal address AB23C to access a 32-bit word, answer the following -

(a) Specify the set number to which the given address maps.

(b) Mention the tag bits in the given address.

(c) How many tags need to be checked for a matching in the given scenario?

Q.3 Describe in words and by means of a block diagram, how multiple matched words can be read out from an associated memory?

Q.4 A computer employs RAM chips of 256 × 8 and ROM chips of 1024 × 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM and four interface units, each with four registers. A memory-mapped 1/10 configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers -

(a) How many RAM and ROM chips are needed?

(b) Draw a memory-address map for the system.

(c) Give the address range in hexadecimal for RAM, ROM and interface.

Q.5 Design a 4 bit carry look-ahead adder. Define the carry generate and propagate functions with the components of a basic cell and explain the gate delays required for obtaining the outputs.
