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B.TECH. V SEM (NEW SCHEME) MAIN EXAMINATION 2023-24

ARTIFICIAL INTELLIGENCE & MACHINE LEARNING-V

5AM4-02) - Computer Organization and Architecture

Common to CS, AI AD, AM, CA, CD, DS, IO, IT, MC, CM, CY)

Time : 3 Hours]

[Max. Marks : 70

[Min. Passing Marks :

Instructions to Candidates :

Part–A : Short Answer Type Questions (up to **25** words) 10 × 2 = 20 marks. All 10 questions are compulsory.

Part–B : Analytical/Problem Solving questions 5 × 4 = 20 marks. Candidates have to answer 5 questions out of 7.

Part–C : Descriptive/Analytical/Problem Solving questions 3 × 10 marks = 30 marks. Candidates have to answer 3 questions out of 5.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.

Use of the following supporting materials is permitted during examination. (Mentioned in form no. 205).

1_____

2_____

10×2=20

Part–A

1. Describe the term Register with suitable example. 2

2. What do you mean by micro-operation ? 2

3. With a suitable example, explain airthmetic micro-operation. 2

4. What is the need of control word in a computer sytem ? 2

5. Explain the use of memory address register and memory data register. 2

6. Discuss the need of input-output processor. 2

7. Solve $(1101.10)_2 - (1000.10)_2$ using 2's complement subraction method. 2

8. Write the full form of RISC and CISC. 2

9. Explain the use of instruction register. 2

10. What do you mean by memory transfer ? Give suitable example. 2

Part–B

5×4=20

1. What is the need of addressing modes ? Explain following addressing modes : 4

   (i) Direct

   (ii) Register

   (iii) Indirect.

2. Categorize the types of RAM Design block diagram of 512 × 16 RAM. How many address line and data line will this RAM has ? 4

3. Convert following airthmetic expression into reverse polish notation : 4

$$A \times B + A \times (B \times D + C \times E)$$

4. Give the concept of the following : 4

   (i) Page map table

   (ii) Pipeline

   (iii) SIMD.

5. Show the block diagram of the hardware that implement the following register transfer language : 4

$$yT_2 : R_2 \leftarrow R_1 + R_2$$

6. Let initial value of reigster R is 1101110. What will be contents of register R after performing logical shift left, circular shift right and airthmetic shift right. 4

7. Explain diferent types of computer memory with the help of memory hierarchy. 4

Part–C 3×10=30

1. Describe Flynn taxonomy of parallel machine models. An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200 Evaluate the effective address if addressing mode of instruction is : 10

   (i) Direct

   (ii) Immediate

   (iii) Relative.

2. Demonstrate the working of following types of address mapping in relation to cache memory : 10

   (i) Associative mapping

   (ii) Direct mapping

   (iii) Set associative mapping.

3. Explain the block diagram of DMA chip. Write meaning of every pin of chip. With a neat diagram explain working of DMA. 10

4. With a suitable example, explain 1-address, 2-address and 3-address instructions related to CPU organization. 10

5. Solve (+13) × (–7) using Booth multiplication algorithm. 10

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