5E3251

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B. Tech. (Sem. V) (Main/Back) Examination, December - 2013
Computer Science
5CS1 Computer Architecture (Common for Computer & IT)

Time : 3 Hours] [Total Marks : 80
[Min. Passing Marks : 24

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used / calculated must be stated clearly.

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. NIL 2. NIL

UNIT - I

1 (a) If a computer has 128 operation codes and 512 k addresses, how many bits would be required for
(i) Single address instruction
(ii) Two address instruction
6

(b) What is instruction ? What are different parts of an instruction ? Explain the significance of each part of an instruction with an example.
6

(c) What do you mean by instruction set completeness ?
4

OR

1 (a) What is addressing mode ? Explain different addressing modes with suitable examples. 7

(b) Explain Von Neumann Architecture. What are its drawbacks ? 7

(c) What is the data transfer rate of PCI bus ? 2

UNIT - II

2 (a) What are the different conflicts that will arise in pipeline ? How do you remove the conflict ? Describe. 8

(b) Why do we require instruction pipelining ? Explain its working procedure. Discuss the pipeline performance measures. 8

OR

2 (a) Differentiate between synchronous and asynchronous data transfer method. 8

(b) Give the difference between RISCand CISC processor. Describe in detail. 8

UNIT - III

3 (a) Discuss how Booth's algorithm treats positive and negative multiplier uniformly. 6

(b) With the help of a block diagram discuss the construction and working of 8 bit carry look ahead adder. Also compute total time needed to perform one addition using gate delay of each gate 8 μs and no delay are involved in the connecting wires. 10

OR

3 (a) Using Booth's algorithm, Multiply (+14) and (–12) when the numbers are represented in 2's complement form.

8

(b) What is serial adder ? Discuss it briefly with diagram.

4

(c) Explain floating point addition and substraction with suitable example.

4

UNIT - IV

4 (a) How many 256 × 8 ROM chips are required to produce a memory capacity of 4000 bytes ? How many address lines are required to access 4000 bytes ? How many of these addresses will be common to all these chips ?

6

(b) What is Cache mapping ? Explain directmapping for 256 × 8 RAM and 64 × 8 Cache memory.

6

(c) Discuss the general characteristics of memory system. What is the use of virtual memory and discuss its concept.

4

OR

4 (a) A disk pack of 20 recording surfaces and has 400 cylinders. There is an average of 300 sectors per track. Each sector contain 512 bytes of data.

(i) What is the maximum number of bytes that can be stored in this pack ?

(ii) What is data transfer rate in bytes per second at a rotational speed of 3600 rpm?

8

(b) Explain the organization of a 1 k × 1 memory with neat sketch.

8

UNIT - V

5 (a) What is Direct Memory Access ? Explain the working of DMA. 8

(b) What are different type of DMA transfer ? Explain. 8

OR

5 Write short notes on :

(a) Priority interrupt

(b) IOP processor. 2×8=16
