# 16-bit Program Counter (PC)

## DDCO Assignment 2b

## October 11, 2017

A crucial part of a microprocessor is the Program Counter and its associated circuitry, the design and implementation of which is the objective of the current assignment. For a microprocessor to load and execute an instruction, it first needs to fetch the instruction from the memory. To do so, there has to be a register in the microprocessor which stores the memory address of the next instruction to be fetched. That register is the Program Counter (PC).

Typically, the microprocessor fetches and executes instructions sequentially—so after fetching an instruction from an address, the instruction from the next consecutive address is fetched and so on. But occasionally, there can be jumps—the next instruction to be fetched and executed may be several instructions ahead or behind the current instruction. Likewise, the circuitry associated with the PC register needs to support two operations: (1) increment the PC contents by one, (2) add/subtract given value to PC contents.

The PC register is of length 16-bits. After the reset signal is applied, its contents should be zero. Considering the PC module as a black box, it has the following inputs: clk, reset, inc, add, sub, offset of which only offset is a wire vector of length 16. The only output is pc a 16-bit wire vector of PC register contents. The increment and add/subtract operations each take one clock cycle, so one or add/subtract operation can be performed every clock cycle[1], as outlined below.

When inc is high, the increment operation is to be performed. The add, sub, offset inputs are ignored and the contents of the PC register are simply incremented by one. When add or sub is high, the add or subtract operation respectively is performed, during which the value offset is added to or subtract from the PC register contents, and the result is stored back in the PC register. When inc, add and sub are all low, PC register value remains unchanged. It is guaranteed that at most one of inc, add or sub will be high in a clock cycle.

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[1]Depending upon the inputs received in the current clock cycle, the increment or add/subtract can be performed and made available at the inputs to the PC register in the current clock cycle itself. But the contents of the PC register will change only at the positive clock edge and so the updated register output will be seen only in the next clock cycle but during which the next operation can be computed. In this way one operation can be performed every clock cycle.

# 1 Design and Simulation

You can use the lib.v supplied for basic components. The pc module can be tested using the supplied tb_pc.v with the commands to simulate:

```
iverilog -o tb_pc lib.v pc.v tb_pc.v
vvp tb_pc
```

followed by waveform observation with the command:

```
gtkwave tb_pc.vcd
```

The general approach and the tools used remain the same as last assignment.