Rajeev Marada

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PROFESSIONAL SUMMARY

Dedicated VLSI engineer with advanced certification from IISc Bangalore and hands-on experience in digital design, verification, and UVM methodology. Proven ability to translate complex theoretical concepts into efficient, real-world hardware solutions, demonstrated through published research and a granted patent. Passionate about developing reliable, high-performance hardware for AI and next-generation computing challenges.

EDUCATION

PG Level Advanced Certification in VLSI Chip Design, *Indian Institute of Science (IISc)* Feb 2024 – Dec 2024 | Bangalore, IN
- Completed an intensive 11-month program, achieving an 80% overall score.
- Relevant Coursework: Analog & Digital Integrated Circuit Design, Advanced Digital Design & FPGA-based Design, RISC-V Architecture.

Bachelor of Technology in Electronics and Communication Engineering, Jun 2019 – May 2023 | Chennai, IN
SRM Institute of Science and Technology
- Graduated with a CGPA of 9.4/10.0.
- Relevant Coursework: Digital Design, ARM-based Embedded System Design, VLSI Design Methodology.

PROFESSIONAL EXPERIENCE

Programmer Analyst, *Cognizant Technology Solutions* Aug 2024 – Present | Chennai, IN
- Automated key business workflows within the Intelligent Process Management team by developing and deploying solutions on the APPIAN low-code platform.
- Collaborated on cross-functional projects to analyze and optimize enterprise-level processes, contributing to enhanced business efficiency.

Junior Design Verification Engineer, *Insemi Technology Services* Jul 2023 – Oct 2023 | Bangalore, IN
- Developed a comprehensive UVM testbench to validate a Dual-Port RAM design, creating constrained-random test cases that achieved 100% functional coverage.
- Analyzed protocol compliance by writing SystemVerilog assertions and functional coverage, successfully identifying and debugging design flaws.

Intern, *Maven Silicon* Dec 2022 – Jan 2023 | Bangalore, IN
- Deepened understanding of digital and system-level design fundamentals, especially finite state machine (FSM) architecture, and enhanced practical skills in module integration and testbench planning.
- Designed and implemented a compliant AMBA AHB-APB bridge in Verilog to manage communication between high- and low-frequency SoC subsystems.

Intern, *CoreEl Technologies – Sandeepani School of Embedded System Design* Jun 2022 – Jul 2022 | Bangalore, IN
- Learned SystemVerilog verification workflows, building key testbench components—drivers, monitors, scoreboards, assertions—and applied digital design principles for module development.
- Developed and validated a SystemVerilog testbench for a full adder DUT, achieving 100% functional and code coverage through rigorous assertion-based verification.

KEY PROJECTS

RISC-V Based Hardware Accelerator for ECG Classification Feb 2025 – Apr 2025
- Engineered a heterogeneous SoC integrating a RISC-V processor and a custom neural network via the AXI Stream protocol, achieving 92% accuracy in real-time ECG classification through Q1.15 fixed-point arithmetic optimization.
- Validated the complete SoC and accelerator design through simulation and deployment on FPGA hardware, demonstrating robust real-time performance and ensuring practical hardware deployability.

Neural Network Inference Engine for Handwritten Digit Classification May 2024 – Dec 2024
- Designed and implemented a Verilog RTL 3-layer neural network inference engine with custom ROM-based weights and FIFO input, achieving over 85% Semeion dataset accuracy through efficient fixed-point hardware conversion.
- Performed simulation, functional verification, synthesis, and implementation in Xilinx Vivado, establishing timing closure and implementation readiness for FPGA-based deployment.

UVM Testbench for APB Protocol Verification Dec 2023 – Jan 2024
- Architected a modular UVM testbench, developing reusable master/slave agents and environment components, to rigorously validate APB protocol compliance.
- Achieved 100% functional and code coverage and confirmed design robustness through complete assertion coverage, ensuring error-free operation.

Error Correction Module for SoC Data Integrity Jan 2023 – May 2023
- Led development of a novel SEC-DED-DAEC error-correcting module and integrated it into an AHB-APB bridge to ensure data integrity for system-on-chip pathways.
- Optimized the reversible logic implementation to achieve a 5.67% reduction in power consumption and a 4.52% improvement in critical path delay over other novel designs, culminating in an IEEE publication.

PATENT

A System for Controlling an Autonomous Vehicle and a Method Thereof Mar 2025
- **Patent Number:** IN 564400 | **Status:** Granted
- Addressed the critical safety risk of driver incapacitation by developing a real-time controller for vital-sign sensors and designing an actuator feedback loop, resulting in a successful prototype that could automatically detect medical distress and initiate a safe autonomous takeover.

PUBLICATIONS

Improving data integrity with reversible logic-based error detection and correction module on AHB-APB bridge, *Conference Paper - IEEE* May 2023

A Survey on Affordable Internet of Things (IoT) Enabled Healthcare Systems, Jun 2022
Journal Article - Grenze International Journal of Engineering & Technology (GIJET)

TECHNICAL CONFERENCES

IEEE International Conference on Recent Advances in Electrical, Electronics, Ubiquitous Communication, and Computational Intelligence, *(RAEEUCCI 2023)* Apr 2023

Twelfth International Conference on Advances in Computer Engineering, *(ACE 2022)* May 2022

CERTIFICATIONS & ONLINE COURSES

SystemVerilog for Verification Part 1: Fundamentals, *Udemy* Apr 2023
- Acquired foundational knowledge of SystemVerilog and its application in digital verification workflows.

Verification Methodology Overview, *Maven Silicon* Nov 2022
- Gained a comprehensive overview of hardware verification strategies, focusing on real-world DUT testing approaches.

VLSI Design Methodologies, *Maven Silicon* Oct 2022
- Developed a thorough understanding of digital design, Verilog coding, and core concepts in modern VLSI architectures.

Development of Real-Time Systems, *Coursera/EIT Digital* Mar 2022
- Explored the design and importance of real-time systems for reliable, time-critical embedded applications.

Arduino Training, *Internshala* Feb 2022
- Gained a foundation in electronics concepts and implemented Arduino circuits for IoT and automation projects.

PCB Design Training, *Internshala* Nov 2021
- Designed foundational PCB layouts using Autodesk Eagle, applying principles of circuit design, via placement, and multi-layer board construction.

Blockchain Basics, *Coursera/University at Buffalo, SUNY* Aug 2021
- Studied core mechanisms and practical applications of blockchain technology, cryptocurrency, and decentralized systems.

WORKSHOPS & TECHNICAL TRAINING

Kaizen IoT Workshop, *Lema Labs* Mar 2022
- Designed and implemented a home automation system using MQTT protocol for IoT device communication.

Intel Distribution of OpenVINO Toolkit Online Training, *Intel* Mar 2021
- Gained exposure to deployment practices for AI, machine learning, and computer vision models using Intel's OpenVINO toolkit through hands-on demonstrations and expert-led instruction.

TECHNICAL SKILLS

Domains: Digital Design & Verification | SoC Architecture | Neuromorphic Computing

Languages: SystemVerilog | Verilog | Python | C | C++ | LaTeX

Methodologies: Universal Verification Methodology (UVM)

Tools & EDA: Xilinx Vivado | ModelSim | Questa Sim | Cadence Virtuoso | MATLAB

HONORS & AWARDS

Finalist, Hybrid Hack 2021 ("Charge On Go") Sep 2021
- Co-developed a novel vehicle-mounted hybrid power system to generate electricity during transit and supply it back to the grid.
- Simulated the system's electrical performance using Python and HOMER Pro, projecting an annual energy generation of 465.15 kWh per unit based on an idealized motion dataset.

VOLUNTEER EXPERIENCE

National Service Scheme (NSS) Volunteer Jun 2019 – Mar 2020
- Collaborated with NSS team members and contributed ideas for community outreach and improvement projects.
- Helped organize and lead medical camps focused on care and health awareness for underserved groups.
- Assisted in coordinating anti-drug awareness campaigns and local educational events for youth and families.
- Took initiative in environmental activities, including water conservation, tree plantation, and cleanliness drives.

SOFT SKILLS

Resilience and Perseverance | Adaptability | Critical Thinking | Teamwork and Collaboration

INTERESTS

Photography | Music | eSports | Cricket