

Fig: Functional Block Diagram of 8085 Microprocessor

**1. ALU**

The ALU performs the actual numerical and logic operation such as ‘add’, ‘subtract’, ‘AND’, ‘OR’ etc.

Uses data from memory and from Accumulator to perform arithmetic operation and always stores result of operation in Accumulator.

The ALU consists of accumulator, flag register and temporary register.

**a. Accumulator**

The accumulator is an 8-bit register that is a part of arithmetic/logic unit (ALU). This register is used to store 8-bit data and to perform arithmetic and logical operations. The result of an operation is stored in the accumulator.

The accumulator is also identified as register A.

**b. Flag register**

8085 has 8-bit flag register. There are only 5 active flags.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| S | Z |  | AC |  | P |  | CY |

Fig: 8085 flag register

Flags are flip-flops which are used to indicate the status of the accumulator and other register after the completion of operation.

These flip-flops are set or reset according to the data condition of the result in the accumulator and other registers.

**i. Sign flag(S):**

Sign flag indicates whether the result of a mathematical or logical operation is negative or positive.

If the result is negative, this flag will be set (i.e. S=1) and if the result is positive, the flag will be reset (i.e. S=0).

**ii. Zero flag (Z):**

Zero flag indicates whether the result of a mathematical or logical operation is zero or not.

If the result of current operation is zero, the flag will be set (i.e. Z=1) otherwise the flag will be reset (Z=0).

This flag will be modified by the result in the accumulator as well as in the other register.

**iii. Auxiliary carry flag (AC):**

In operation when a carry is generated by bit D3 and passes on to bit D4, the AC flag will be set otherwise AC flag will be reset.

This flag is used only internally for BCD operation and is not available for the programmer to change the sequence of program with the jump instruction.

**iv. Parity flag (P):**

This flag indicates whether the current result is of even parity (no. of 1’s is even) or odd parity (no. of 1’s is odd).

If even parity, P flag will be set otherwise reset.

**v. Carry flag (CY):**

This flag indicates whether during an addition or subtraction operation carry or borrow is generated or not.

If carry or borrow is generated, the flag will be set otherwise reset.

**2. Timing and control unit**

This unit produces all the timing and control signal for all the operation.

This unit synchronizes all the MP operations with the clock and generates the control signals necessary for communication between the MP and peripherals.

**3. Instruction register and decoder**

The instruction register and decoder are part of ALU. When an instruction is fetched from memory, it is loaded in the instruction register.

The decoder decodes the instruction and establishes the sequence of events to follow.

The IR is not programmable and cannot be accessed through any instruction.

**4. Register array**

The register unit of 8085 consists of

            -Six general-purpose data registers B,C,D,E,H,L

            -Two internal registers W and Z

            -Two 16-bit address registers PC (program counter) and SP (stack pointer)

            -One increment/decrement counter register

            -And, one multiplexer (MUX)

The six general-purpose registers are used to store 8-bit data. They can be combined as register pairs BC, DE, and HL to perform some 16-bit operations.

The two internal registers W and Z are used to hold 8-bit data during the execution of some instructions, CALL and XCHG instructions.

SP is 16-bit registers used to point the address of data stored in the stack memory. It always indicates the top of the stack.

PC is 16-bit register used to point the address of the next instruction to be fetched and executed stored in the memory.

**5. System bus**

**a. Data bus**

It carries ‘data’, in binary form, between MP and other external units, such as memory.

Typical size is 8 or 16 bits.

**b. Address bus**

It carries ‘address’ of operand in binary form.

Typical size is 16-bit.

**c. Control Bus**

Control Bus are various lines which have specific functions for coordinating and controlling MP operations.

E.g.: Read/Write control line.

**6. Interrupt Control**

Interrupt is a signal, which suspends the routine what the MP is doing, brings the control to perform the subroutine, completes it and returns to main routine.

May be hardware or software interrupts. Some interrupts may be ignored (maskable), some cannot (non-maskable).

E.g. INTR, TRAP, RST 7.5, RST 6.5, RST 5.5

**7. Serial I/O Control**

The MP performs serial data input or output (one bit at a time). In serial transmission, data bits are sent over a single line, one bit at a time.

The 8085 has two signals to implement the serial transmission: SID (serial input data) and SOD (serial output data).

Q ) **8085 Microprocessor Features:**

The features of 8085 Microprocessor include :

1.It is an 8-bit microprocessor i.e. it can accept, process, or provide 8-bit data simultaneously.

2.It operates on a single +5V [power supply](https://www.eeeguide.com/electric-power-industry/) connected at Vcc; power supply ground is connected to Vss.

3.It operates on clock cycle with 50% duty cycle.

4.It has on chip [clock generator](https://www.eeeguide.com/microprocessor-based-ramp-type-dvm/). This internal clock generator requires tuned circuit like LC, RC or crystal. The internal clock generator divides oscillator frequency by 2 and generates clock signal, which can be used for synchronizing external devices.

5.It can operate with a 3 MHz clock frequency. The 8085A-2 version can operate at the maximum frequency of 5 MHz.

6.It has 16 address lines, hence it can access (216) 64 Kbytes of memory.

7.It provides 8 bit I/O addresses to access (28 ) 256 I/O ports.

8.In 8085, the lower 8-bit address bus (A0 -A7) and data bus (D0 -D7) are Multiplexed to reduce number of external pins. But due to this, external hardware (latch) is required to separate address lines and data lines.

9.It supports 74 instructions with the following addressing modes :

a) Immediate b) Register c) Direct d) Indirect e) Implied

10.The [Arithmetic Logic Unit](https://www.eeeguide.com/microprocessor-based-digital-filter/) (ALU) of 8085 performs :

(a)8 bit binary addition with or without carry

(b)16 bit binary addition

(c)2 digit BCD addition.

d)8-bit binary subtraction with or without borrow

(e)8-bit logical AND, OR, EX-OR, complement (NOT), and bit shift operations.

11.It has 8-bit accumulator, flag register, instruction register, six 8-bit general purpose registers (B, C, D, E, H and L) and two 16-bit registers. (SP and PC). Getting the operand from the general purpose registers is more faster than from memory. Hence skilled programmers always prefer general purpose registers to store program variables than memory.

12.It provides five hardware interrupts : TRAP, RST 7.5, RST 6.5, RST 5.5 and INTR.

13.It has serial I/O control which allows [serial communication](https://www.eeeguide.com/sensors-based-computer-data-systems/).

14.It provides control signals (IO/M, RD, WR) to control the bus cycles, and hence external bus controller is not required.

15.The external hardware (another microprocessor or equivalent master) can detect which machine cycle microprocessor is executing using status signals (IO/M, S0, S1) This This feature is very useful when more than one processors are  
using common system resources (memory and I/O devices).

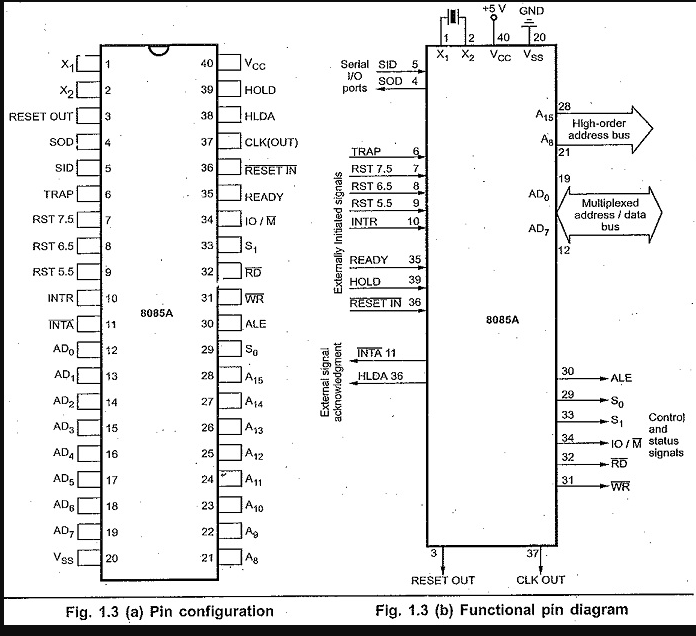
16.It has a mechanism by which it is possible to increase its interrupt handling

17.The 8085 has an ability to share system bus with [Direct Memory Access](https://www.eeeguide.com/?s=Direct+Memory+Access) This feature allows to transfer large amount of data from I/O device to memory or from memory to I/O device with high speeds.

18.It can be used to implement three [chip](http://www.circuitstoday.com/) microcomputer with supporting I/O devices like IC 8155 and IC 8355.

## 8085 Microprocessor Pin Diagram:

Fig. 1.3 (a) and (b) shows 8085 pin configuration and functional 8085 Microprocessor Pin Diagram respectively. The signals of 8085 can be classified into seven groups according to their functions.



1. Power supply and frequency signals.
2. Data bus and address bus
3. Control bus
4. Interrupt signals
5. Serial I/O signals
6. DMA signals
7. Reset signals

### **Power Supply and Frequency Signals**

**(1) Vcc :** It requires a single +5 V power supply.

(**2) Vss** : Ground reference.

(**3) X1 and X2 :** A tuned circuit like LC, RC or crystal is connected at these two The internal [clock generator](https://www.eeeguide.com/pulse-width-modulation/) divides oscillator frequency by 2, therefore, to operate a system at 3 MHz, the crystal of tuned circuit must have a frequency of 6 MHz.

**(4) CLK OUT :** This signal is used as a system clock for other devices. Its frequency is half the [oscillator frequency](https://www.eeeguide.com/beat-frequency-oscillator/).

### **Data Bus and Address Bus**

**A) AD0 to AD7 :** The 8 bit data bus (D0 – D7) is multiplexed with the lower half (A0 – A7) of the 16 bit address bus. During first part of the [machine cycle](https://www.eeeguide.com/dc-machine-diagram/) (T1), lower 8 bits of memory address or I/O address appear on the bus. During remaining part of the machine cycle (T2 and T3) these lines are used as a bi-directional data bus.

**B) A8 to A15 :** The upper half of the 16 bit address appears on the address lines A8 to A15. These lines are exclusively used for the most significant 8 bits of the 16 bit address lines.

### Control and Status Signals

**A) ALE (Address Latch Enable) :** We, know that AD0 to AD7 lines are multiplexed and the lower half of address (A0 – A7) is available only during T1 of the machine cycle. This lower half of address is also necessary during T2 and T3 of machine cycle to access specific location in memory or I/O port. This means that the lower half of an address must be latched in T1 of the machine cycle, so that it is available throughout the machine cycle. The latching of lower half of an address bus is done by using external latch and ALE signal from 8085 Microprocessor Pin Diagram.

**B) RD and WR :** These signals are basically used to control the direction of the data flow between processor and memory or I/O device/port. A low on RD indicates that the data must be read from the selected memory location or I/O port via data bus. A low on WR indicates that the data must be written into the selected memory location or I/O port via data bus.

**C) IO/M, S0 and S1 :** IO/M indicates whether I/O operation or memory operation is being carried out. S1 and S0 indicate the type of machine cycle in progress.

**D) READY :** It is used by the microprocessor to sense whether a peripheral is ready or not for data transfer. If not, the processor waits. It is thus used to synchronize slower peripherals to the microprocessor.

### **Interrupt Signals**

The 8085 has five [hardware](https://www.eeeguide.com/plc-hardware-components/) interrupt signals : RST 5.5, RST 6.5, RST 7.5, TRAP and INTR. The microprocessor recognizes interrupt requests on these lines at the end of the current instruction execution.

The INTA (Interrupt Acknowledge) signal is used to indicate that the processor has acknowledged an INTR interrupt.

### **Serial I/O Signals**

**A) SID (Serial I/P Data) :** This input signal is used to accept serial data bit by bit from the external device.

**B) SOD (Serial 0/P Data)** : This is an output signal which enables the [transmission](https://www.eeeguide.com/choice-electronic-signal-transmission/) of serial data bit by bit to the external device.

### **DMA Signal**

**A) HOLD :** This signal indicates that another master is requesting for the use of address bus, data bus and control bus.

**B) HLDA :** This active high signal is used to acknowledge HOLD request.

### Reset Signals

**A) RESET IN :** A low on this pin

Sets the program counter to zero (0000H).

Resets the interrupt enable and HLDA flip-flops.

Tri-states the data bus, address bus and control bus. (Note : Only during RESET is active).

Affects the contents of processor’s [internal registers](https://www.eeeguide.com/plc-structure/) randomly.

On reset, the PC sets to 0000H which causes the 8085 Microprocessor Pin Diagram to execute the first instruction from address 0000H. For proper reset operation reset signal must be held low for at least 3 clock cycles. The power-on reset circuit can be used to ensure execution of first instruction from address 0000H.

**B) RESET OUT :** This active high signal indicates that [processor](http://www.circuitstoday.com/) is being reset. This signal is synchronized to the processor clock and it can be used to reset other devices connected in the system.