## Nihit Chattar

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| **PROFILE** |

* Currently Working as **ASIC Engineer** in Brocade Comm.
* Worked as **Product Development Engineer** in PMC-Sierra.
* Worked as **Design Engineer** in Vitesse semiconductors.
* Postgraduate in **Micro-electronics** (VLSI) from Indian Institute of Technology, Bombay.

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| **SKILL SET** |

Hardware Programming Languages: **Verilog, System Verilog**, Specman (E), VHDL

Verification Methodologies: **OVM, UVM**

Other Languages: C, Perl

Design Tools: NCSim, QuestaSim, ModelSim, Xilinx ISE, Verdi, RC, VCS, Vivado

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| **ACHIEVEMENTS** |

* Filed a **patent as co-inventor** on CRC computation methods - Venkat Praveen Kumar, Chattar Nihit and Rajput Dishant Singh “Parallel CRC computation with byte enables”.

Patent Publication No – 20120173952.

* Received two Performance Awards for MAC 40G/100G Testbench development.
* Secured All India **23rd rank** with 99.92 percentile in GATE 2007 in ECE.

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| **EDUCATION** |

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| **Degree** | **Institute** | **Year** | **CPI/%** |
| M.Tech (Microelectronics) | Indian Institute of Technology, Bombay | 2007-2009 | 9.15 |
| B.E. (Electronics & Telecommunication) | Institute of Engineering & Technology, DAVV, Indore. | 2003-2007 | 82.66% |
| Intermediate/+2 | Devi Ahilya Shishu Vihar | 2003 | 79.33% |

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| **WORK EXPERIENCE Total Duration: 5 years** |

**Organization:** Brocade comm. **Designation:** ASIC Engineer-3 **Duration:** 1 Year 4 months

**Project-1:** Test Bench development in **System Verilog** for verification of Flow Control Block in a FC-WAN extension FPGA.

**Responsibilities:**

* Implemented DUT **Model, scoreboards, frame generators and Monitors** for verification of FCB.
* Implemented **Test Cases** to verify Pause/PFC & Credit based flow controls. Also tested partial frame support. Found many crucial RTL bugs and some of them are well appreciated by the designers.

**Project-2:** Test Bench development in **System Verilog** using **UVM** for verification of L2-Aging Block.

**Responsibilities:**

* Designed and implemented Aging Scanner **Model and Monitor**.
* Implemented **Test Cases** to verify Aging scanner & expected Age-out Behavior.

Other **Responsibilities:**

* Behavioral modeling of Avago **TCAM memory** models in Verilog for simulation purpose.
* Top level verification of **XAUI-10G MAC using SV** for a FC-WAN extension FPGA.
* Gate level simulations of LAN & WAN data path for basic Test Cases.

**Organization:** PMC Sierra **Designation:** Product Development Engineer **Duration:** 2 Years

**Project-1:** Test Bench development in **Specman** **UVM** for verification of OTU Framer Block.

**Responsibilities:**

* Designed and implemented **drivers, monitors and sequences** on both line side and system side of OTU Framer block.
* Implemented **TestCases** in Specman for testing RX & TX path functionality of OTU Framer. Found many crucial bugs for OTU Framer, some of them were appreciated by the team.

**Project-2:** Test Bench development in **Specman** **UVM** for verification of MLD Block (SFI Protocols).

**Responsibilities:**

* Designed and implemented **drivers and monitors** for SFI-S, SFI 5.1 Blocks.
* Implemented **System Verilog** modules for 32-bit Precoders on both TX/RX line sides of LINEOTN SS. Also Implemented **SV** monitors for BERGEN components.
* Implemented **TestCases** in Specman for testing of SFI-S, SFI 5.1 blocks. Found many show-stopper issues for SFI-S & SFI5.1 blocks.
* Developed a thorough understanding on **MLD protocols** (SFI-S, SFI 5.1).

**Project-3**: **Synthesis** of PCIe subsystem using **RC**. Scan chain stitching of generated netlist.

**Organization:** Vitesse Semiconductors **Designation:** Design Engineer **Duration:** 1 year 9 months

**Project-1:** TestBench development in **SV OVM** for verification of MAC 40G/100G Block.

**Responsibilities:**

* Designed and implemented **agents, drivers, monitors, transfer functions and sequencers** on both line side and system side of MAC 40G/100G block. TB was generic and reusable at both block level as well as chip level.
* Implemented various **sequences** to generate all possible frame formats.
* Implemented **TestCases** in SV OVM for verification of MAC 40G/100G block. I have found around 60 bugs for MAC 40G/100G RX with **100% bug efficiency**.
* Developed a thorough understanding on 40G/100G **IEEE Standard** (802.3ba).

**Project-2:** CRC 40G/100G module design using **Verilog**.

**Details:** Designed and implemented **byte enabled CRC module working at 40G/100G using Verilog**.

**Responsibilities:**

* Studied various papers and patents on byte enabled CRC computation methods.
* Designed and implemented the CRC module in **Verilog**.
* Designed and implemented Te­­­­stbench using **SV OVM** to verify CRC module.

**Achievements**:

* Proposed a new method to implement byte enabled CRC module. It was well appreciated by the teammates as we found that this method uses **minimum design area** with positive slack time. We have filed a **Patent** for this method – “Parallel CRC computation with byte enables”.

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| **M.TECH THESIS** |

“**Study of Performance and Reliability of SANOS Flash Memory Cell with varying SiN Material Composition and Stack Thickness**”. Guide: Prof. Souvik Mahapatra.

A study was done on the performance and reliability of SANOS flash memory cell under NAND operation. The effect of varying SiN composition and dielectric thickness on the device performance is carried out and the underlying physics is discussed.

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| **PUBLICATIONS** |

**Journalpublication**:

1. Co-author of “Effect of SiN on Performance and Reliability of Charge Trap Flash (CTF) Under Fowler–Nordheim Tunneling Program/Erase Operation”, *IEEE EDL,* pp. 171, vol 30, No 2, 2009.
2. Co-author of “Impact of SiN Composition on SANOS Memory Performance and Reliability under NAND (FN/FN) Operation”, *IEEE TED,* pp. 3123, vol 56, No 12, 2009.

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| **B.E. THESIS** |

“**Implementation of Data Link Layer (DLL) using VHDL**”.

Successfully designed and implemented a Cyclic Redundancy Check (CRC) Algorithm, One Bit sliding Window Protocol and Go Back N protocol in VHDL for achieving reliable and efficient communication between two adjacent machines at Data Link Layer.

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| **POSITIONS OF RESPONSIBILITY HELD** |

a. Coremember of Social Committee, PMC-Sierra, 2011-2012.

b. **PG Representative**, EE Department, IIT Bombay for 2008-2009.