High Performance 4 Bit Braun Multiplier with 22T Hybrid Full Adder

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***Abstract*—Low power and high speed circuits have become important requirements in high performance VLSI design in the last few years. An Arithmetic Logic Unit basically consists of an adder and a multiplier. The basic component of any ALU is an adder and the operation performed by it is called as addition. And this adder is used as a building block to design a multiplier. Hence, multiplication becomes a fundamental unit of any DSP application like FFT, etc. As a result, new approaches to arithmetic circuit design are needed to achieve desirable output in terms of area, power and delay.**

The main objective is to design a High Performance Adder and Multiplier which will be working upto 2 GHz clock frequency. The proposed Hybrid Full Adder is designed using Pass Transistors, Transmission gates and Conventional Complementary Metal Oxide Semiconductor. For multiplication operation, Braun multiplier architecture has been implemented using the above mentioned adder. And the average propagation delay and power dissipated by both the circuits is also calculated.

Keywords—Braun Multiplier, Hybrid Full Adder, 2 GHz

I. Reference Circuit Details

The proposed FA is divided into four major modules: two for carry generation and the other two for sum *(Figure-2***[1]**. *depicts a schematic of the proposed design)*. A novel AND-OR module based on TG and CPL logic is implemented as part of the proposed carry generation part. The proposed FA's sum output is obtained by cascading two XOR modules.

Module 1 and 2 Operation:

Cin = 0 ⇒ Cout = A·B
Cin = 1 ⇒ Cout = A+B

Module 3 and 4 Operation:

Cin = 0 ⇒ Output = A ⊕ B
Cin = 0 and **A ⊕ B = 0 ⇒ Output = Cin**
Cin = 0 and **A ⊕ B = 1 ⇒ Output = Cin**

The schematic implementation of Braun Multiplier is based on the comparison results and uses a 22-T Full adder *(depicted in Figure-3***[2]***)*. The partial products are computed in parallel in the Braun multiplier, then collected using a cascade of different types of adders. It is made up of an array of AND gates and adders organized in an iterative structure that eliminates the need for logic registers. Braun multiplier has one ripple carry adder stage and (n-1) carry save adders for obtaining partial products. The carry save adder is a digital adder that calculates the sum of three or more n-bit binary numbers.

II. Reference Circuit Design

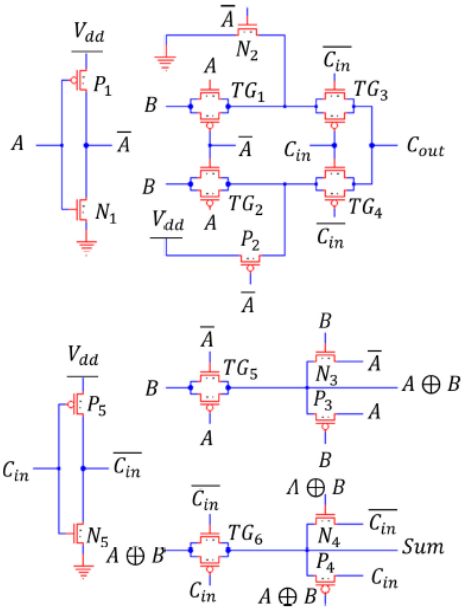

Fig 1: Hybrid Full Adder **[1]**

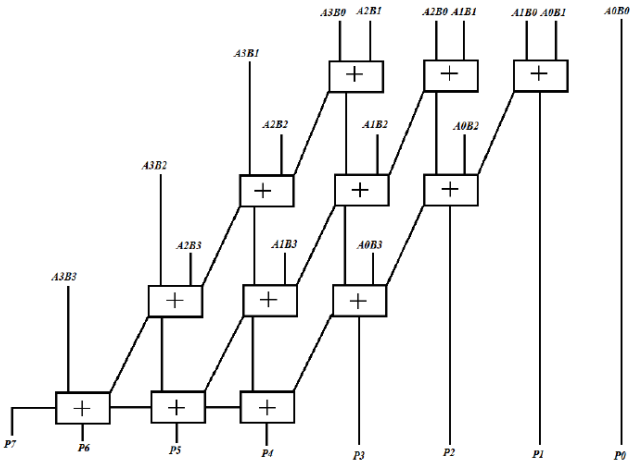

fig 2: 4 Bit Braun Multiplier **[2]**

III. Reference Waveforms and area estimate

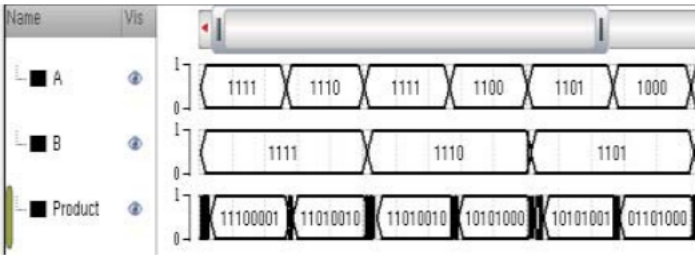

Fig 3: Expected output waveform of 4 Bit Braun Multiplier

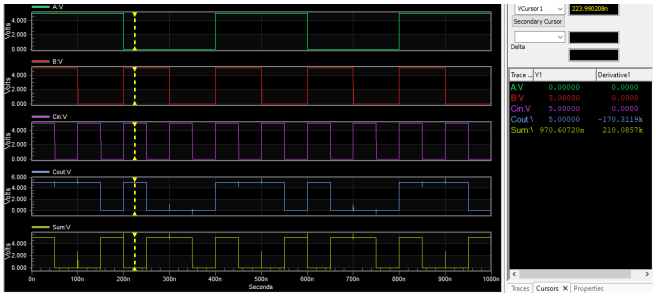

Fig 4: Expected output waveform of Hybrid FA

Area Estimate (4 Bit Braun Multiplier)	~31,861 nm^2

REFERENCES

[1] M. Hasan, M. J. Hossein, M. Hossain, H. U. Zaman and S. Islam, "Design of a Scalable Low-Power 1-Bit Hybrid Full Adder for Fast Computation," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 8, pp. 1464-1468, Aug. 2020, doi: 10.1109/TCSII.2019.2940558.

[2] Sadeghi, Mohsen and Zahedi, Mahya and Ali, Maaruf, The Cascade Carry Array Multiplier – A Novel Structure of Digital Unsigned Multipliers for Low-Power Consumption and Ultra-Fast Applications (July 1, 2019). Annals of Emerging Technologies in Computing (AETiC), Print ISSN: 2516-0281, Online ISSN: 2516-029X, pp. 19-27, Vol. 3, No. 3, Published by International Association of Educators and Researchers (IAER), 1st July 2019 , DOI: 10.33166/AETiC.2019.03.003.