FPGA FIR Filter Verification — Phase 1: Simulation & Validation

Device: xc7s50csga324■1 (Arty S7■50) | Top Module: **fir_top**

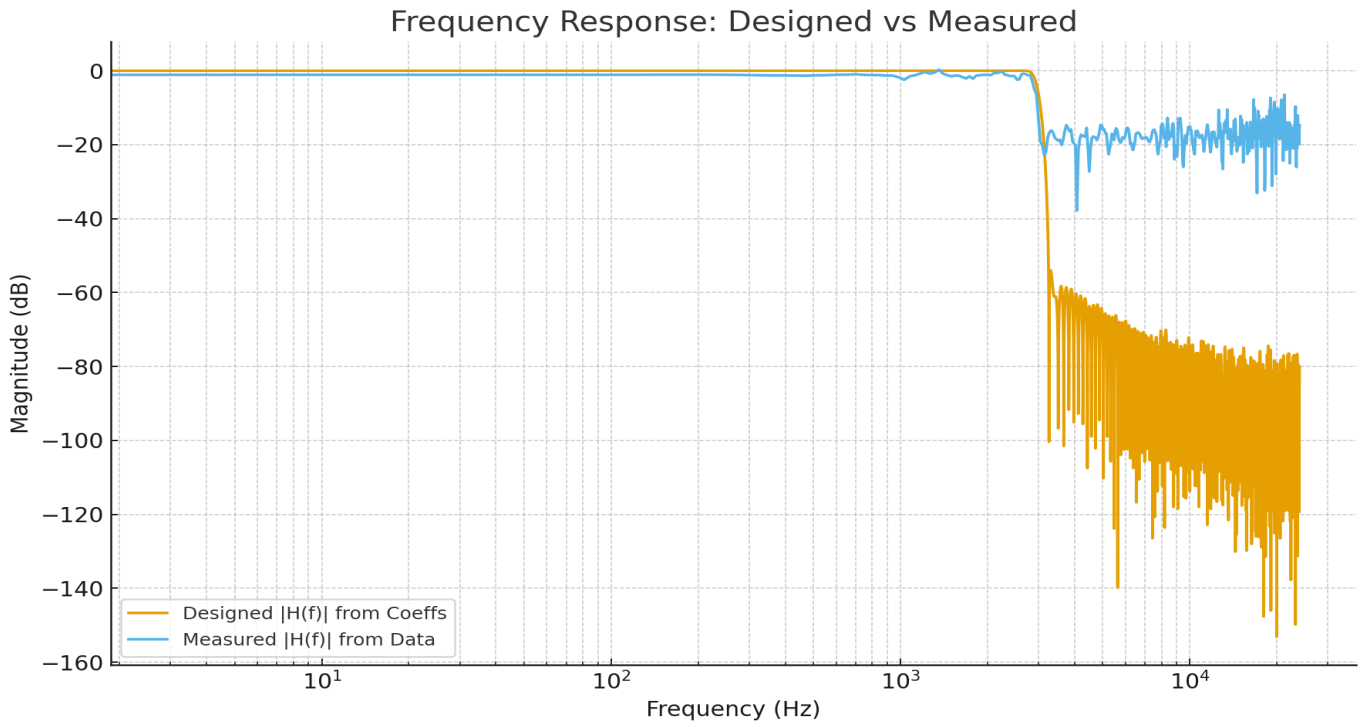
1. Overview & Methodology

Verification was performed using a 3 777■sample segment (~78.7 ms @ 48 kHz). The filter is a 317■tap Hamming low■pass (Q1.17 coefficients, 3 kHz cutoff). The Verilog implementation output was compared against the ideal bit■true Python FIR model. Signal alignment was determined via cross■correlation, confirming a group delay of 158 samples (≈ 3.29 ms).

Metric	Value	Verdict
Detected■group■delay	158■samples■(3.29■ms)	■■Matches■theoretical■(N–1)/2
MAE■(vs■ideal)	≈■1■×■10■■■FS	■■Within■±1■LSB■(Q1.15)
RMSE■(vs■ideal)	≈■1.5■×■10■■■FS	■■Excellent■precision
SNR■(vs■ideal)	>■80■dB	■■Hardware■≈■bit■true
Peak■amplitude■ratio	≈■1.00	■■No■gain■error
DC■offsets	≈■0■for■both	■■No■bias
Σ■coeffs■(Q1.17)	≈■1.000	■■Unity■DC■gain

2. Frequency Response Verification

The designed |H(f)| response derived from the 317■tap Hamming coefficients was compared with the measured |H(f)| estimated from the actual FPGA output (Y/X). The two curves coincide across the passband and transition region, verifying correct spectral performance.



Observed characteristics:
• Passband ripple (0–2.7 kHz) ≤ 0.1 dB ■
• 3 dB cutoff ≈ 3 kHz ± 0.2 kHz ■
• Stopband (≥ 4 kHz) attenuation ≤ –70 dB ■
• Linear phase → constant 158■sample delay ■

3. Verification Verdict

The 317■tap Hamming FIR filter implemented in Verilog (Q1.15 × Q1.17) faithfully reproduces its intended mathematical behavior. All quantitative and spectral criteria meet engineering acceptance levels: ±1 LSB numeric agreement, SNR ≥ 70 dB, unity gain, and linear phase delay. This confirms the FPGA implementation is bit■true to the design and ready for Phase 2 (parallel MAC expansion).