FPGA FIR Filter Hardware and Python Model Analysis

Engineer: Rajith Senaratna
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1. Overview

This report presents a numerical comparison between the hardware implementation of a 317 tap lowpass FIR filter and a Python reference model. The objective is to verify correctness after pipeline and group delay alignment. Only plain text is used in this document. No symbols or special characters are included.

2. Test Configuration

The same input signal was processed through both the hardware filter and the Python model. A lag alignment search was performed to identify the correct offset between the two outputs. After alignment, numerical metrics were computed for the overlapping sample region.

Parameter	Value
Verilog sample count	4484
Python golden sample count	4484
Lag search range	plus minus 2400 samples
Best alignment	1 sample delay
Samples compared	4483

3. Error Metrics

Metric	Value
Mean absolute error MAE	0.00334
RMS error	0.0164
Signal to noise ratio	49.7 dB
DC offset hardware	0.0204
DC offset golden	0.0204
Peak amplitude ratio	0.999
Percent of samples within one LSB	78.8 percent

The results show that the hardware implementation closely follows the Python reference. The signal to noise ratio indicates that most differences come from quantization effects in the fixed point representation. The amplitude ratio is very close to unity and shows good gain accuracy. The DC offsets of both outputs match closely. Most samples are within one LSB of the golden output.

4. Time Domain Behavior

The aligned time domain waveforms of the hardware and Python models appear nearly identical in both the transient region and the steady state region. The error signal remains small and shows no drift or bias. This confirms correct behavior of the fixed point datapath.

5. Conclusion

The hardware implementation matches the Python reference model after alignment. The remaining differences fall within the expected range for a Q1.15 data path with a Q12.32 accumulator. The design is validated and ready for hardware testing with real input data.