FPGA FIR Filter – Phase 1 Hardware Verification Report

Device: xc7s50csga324-1 (Arty S7-50)
Top Module: fir_top

1. FPGA Resource Utilization

This table summarizes the resource usage obtained from Vivado synthesis for the FIR filter design. The utilization is minimal, indicating highly efficient resource mapping. Only one DSP48 slice is used, and overall logic utilization is below 1%.

Resource	Used	Available	Utilization (%)
LUT	108	32,600	0.33
FF	80	65,200	0.12
DSP48	1	120	0.83
Block RAM Tile	1.5	75	2.00
RAMB18	3	150	2.00
RAMB36	0	75	0.00

Interpretation: - LUT and FF utilization are extremely low (<1%), confirming minimal logic overhead. - Only one DSP48E1 slice is used for multiply-accumulate operations. - Three RAMB18 blocks (equivalent to 1.5 BRAM tiles) are used for sample and coefficient storage. - The design is compact and can easily scale for higher tap counts or multi-MAC parallelization.

2. Timing Summary

Timing analysis confirms that the FIR filter design easily meets the 100 MHz system clock constraint. Vivado reported positive slack values across setup, hold, and pulse width checks, indicating robust timing closure.

Metric	Value (ns)
Worst Negative Slack (WNS)	+78.945
Total Negative Slack (TNS)	0.000
Worst Hold Slack (WHS)	+0.144
Worst Pulse Width Slack (WPWS)	+3.000

Interpretation: - The Worst Negative Slack (WNS) of +78.945 ns indicates the design is far faster than the 100 MHz (10 ns) clock period. - Total Negative Slack (TNS) = 0.000 ns confirms no failing paths. - Hold and pulse-width checks also passed with positive margins. - Therefore, the achieved frequency is ≥ 100 MHz, and all constraints are fully met.

3. Engineering Verdict

The synthesized FIR filter design demonstrates exceptional efficiency and timing robustness: • Meets and exceeds 100 MHz timing target. • Utilizes only 1 DSP48 slice and a minimal amount of logic. • Resource utilization is under 2% across all categories. • The architecture is fully scalable for parallel MAC configurations in future phases.

This confirms the FIR core is ready for Phase 2 – **Synthesis and Parallel MAC Expansion**, where the design will be extended to a 4-MAC parallel structure for real-time audio throughput.