
# Ahsanullah University of Science & Technology

## Department of Computer Science & Engineering

**Course No** : CSE3110
**Course Title** : Digital System Design Lab.
**Assignment No** : 03
**Assignment Name** : Implementation Of SAP-1

**Date of Experiment** : 21th January 2023
**Date of Submission** : 05th February 2023

**Submitted To** : MD. Raqibul Hasan & Anika Rahman

**Submitted By-**
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**Lab Group:** A2
**Group** : 2
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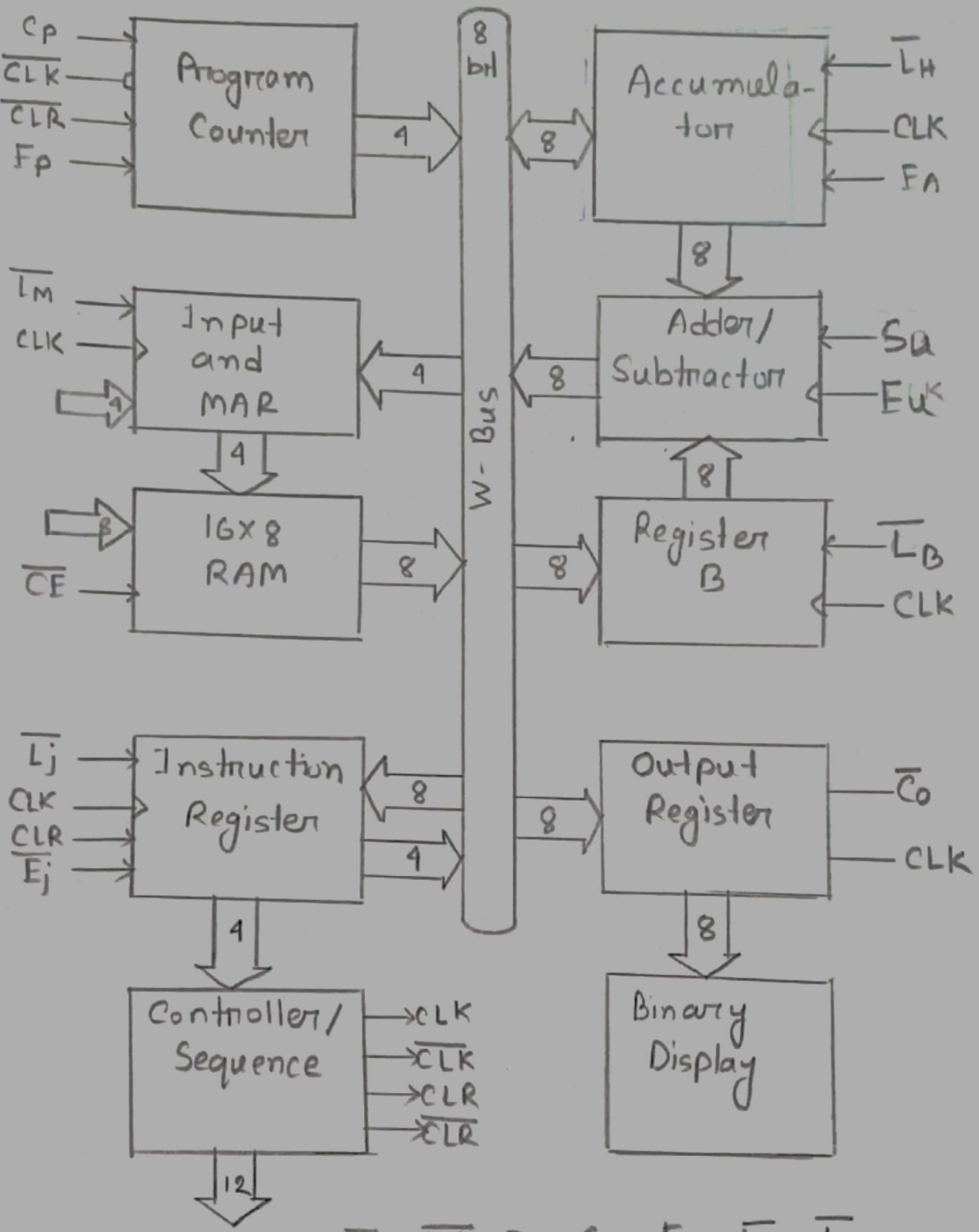
Name of the experiment: Implementation of SAP-1

Introduction: SAP-1 is the first stage in the evolution towards modern computers. The main purpose of SAP is to introduce all the crucial ideas behind computer operations. Being a simple computer, SAP-1 also covers many advanced concepts. SAP-1 is a bus organized computer. All registers are connected to W bus with the help of tri-state buffers. The full form of SAP is simple as possible.

Block Diagrams: (SAP-1)




$C_p, F_p, \overline{L_M}, \overline{CE}, \overline{L_j}, \overline{E_j}, \overline{L_A}, F_A, S_U, E_U, \overline{L_B}, \overline{L_O}$

Fig: SAP-1.

Program Counter:

Memory Address Register (MAR):

| $\overline{Lm}$ | Function |
|---|---|
| 0 | Load |
| 1 | hold |

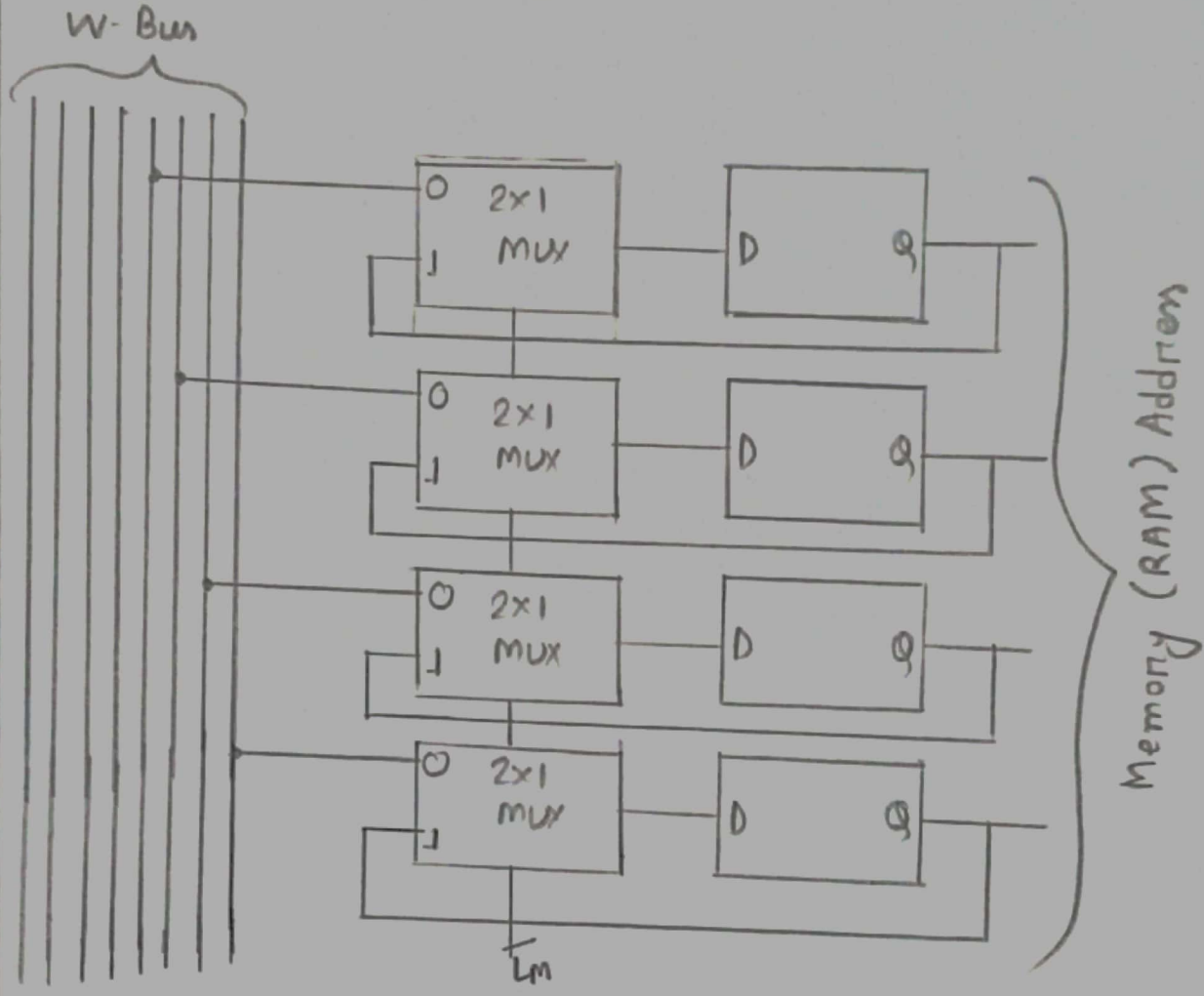
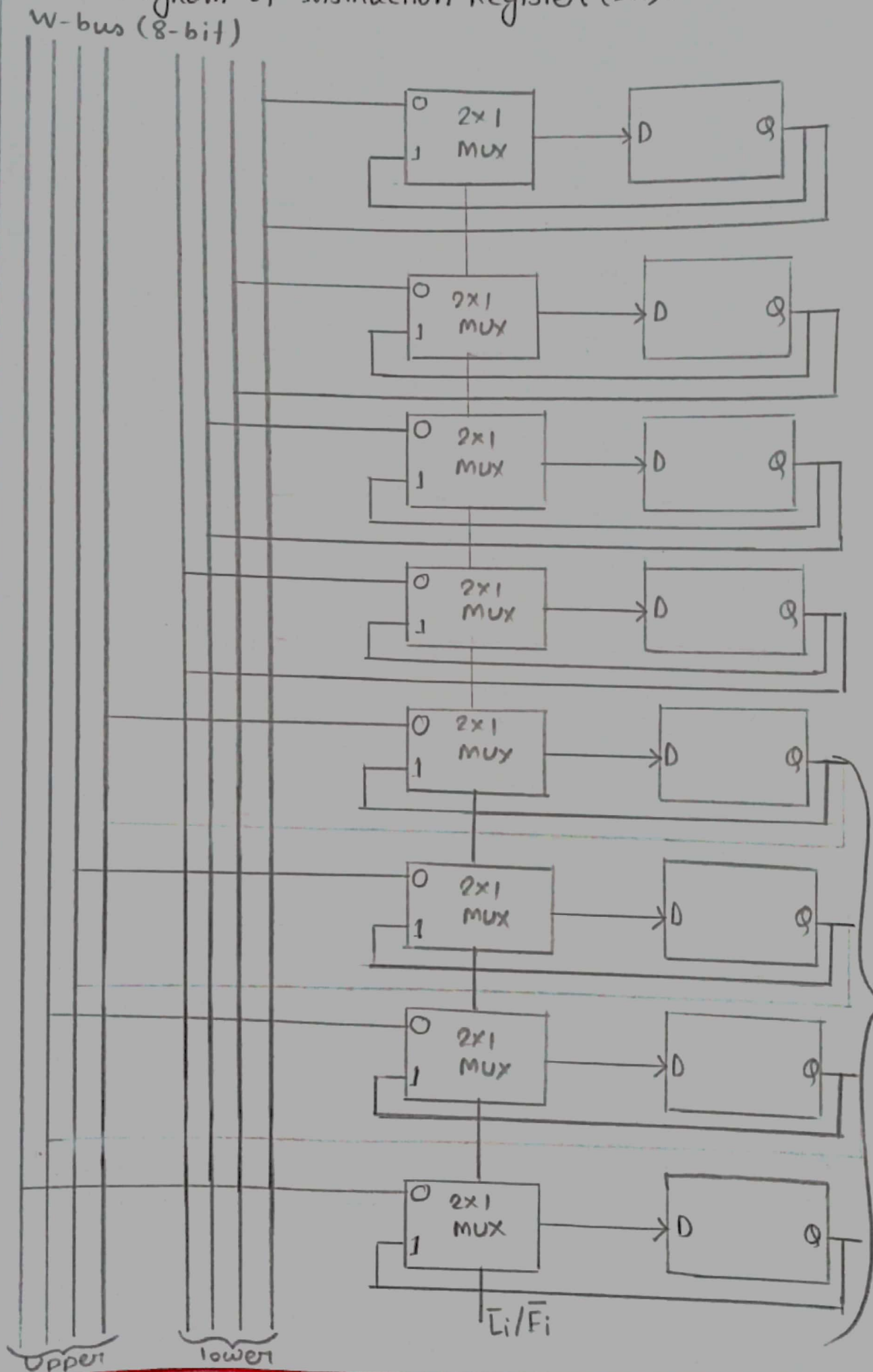
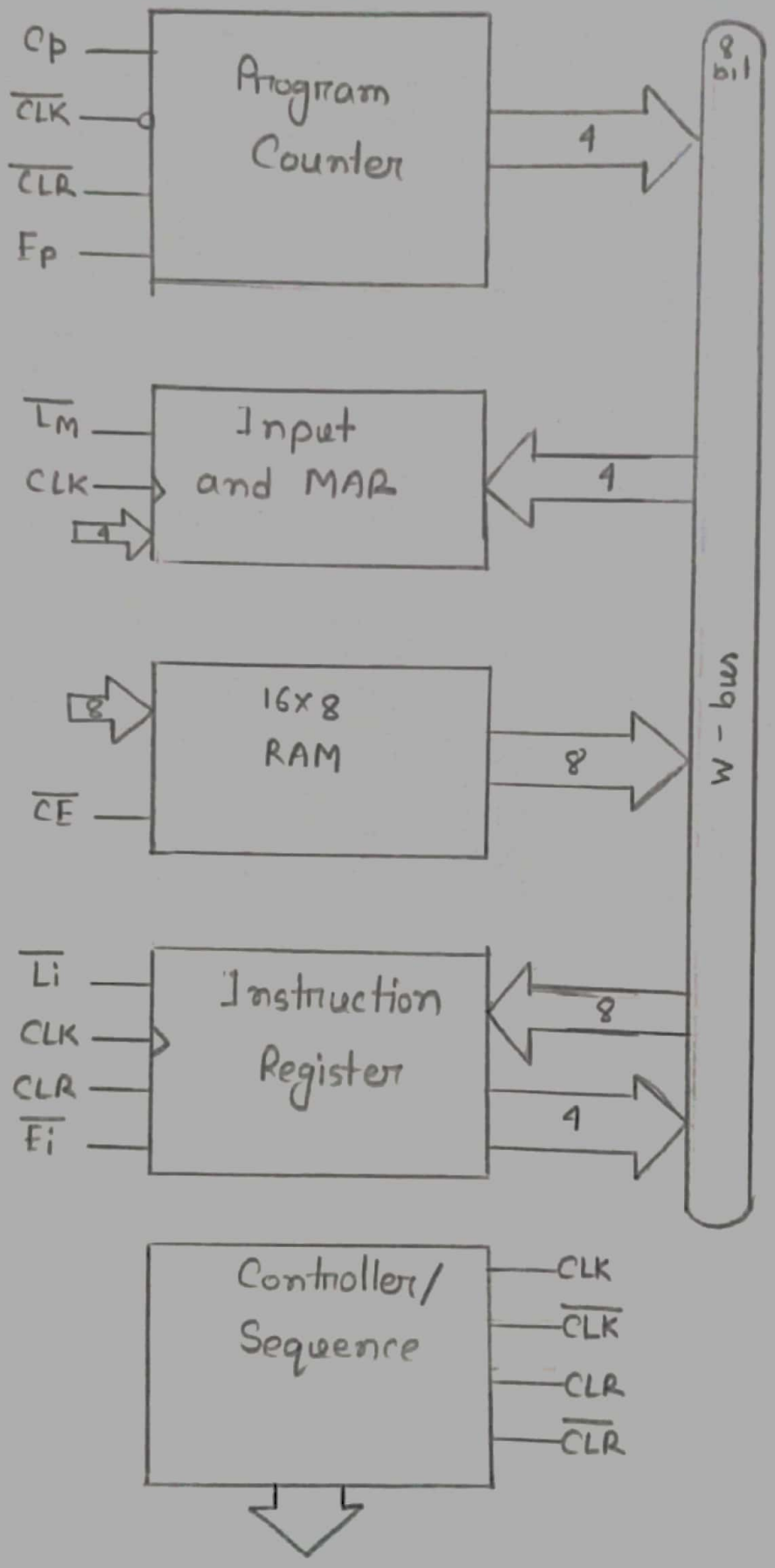



fig: MAR

Circuit Diagram of Instruction Register (IR):






$Cp.Ep.\overline{LM}.\overline{CE}.\overline{Li}.\overline{Ei}.\overline{LA}.EA.Su.Eu.\overline{LB}.\overline{Lo}$

Control Unit:

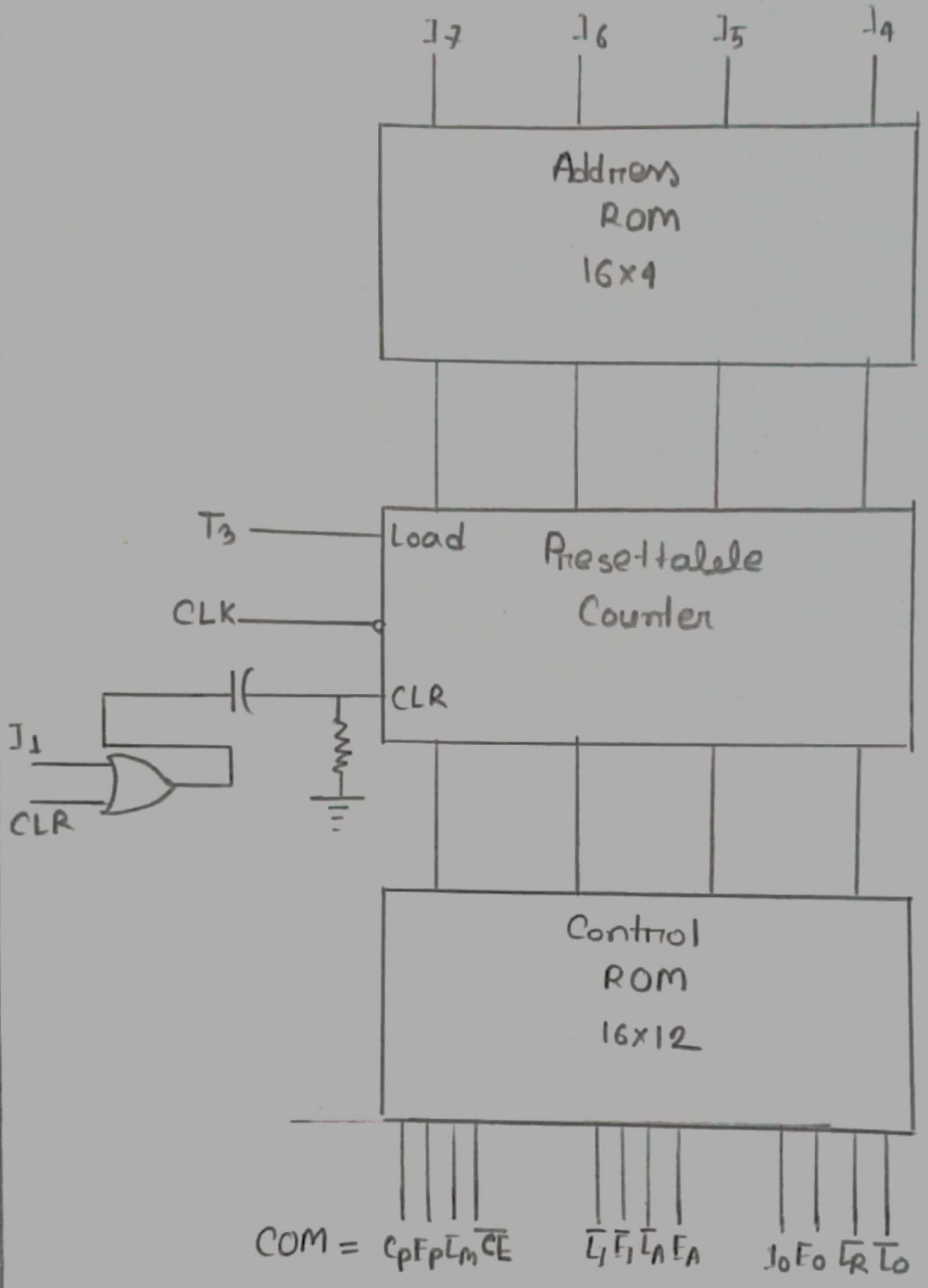
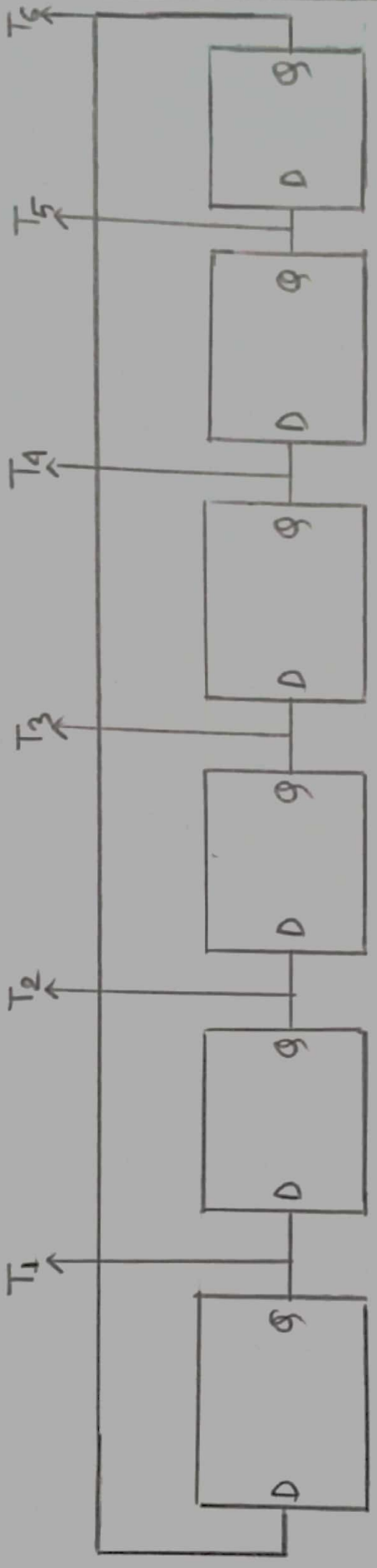
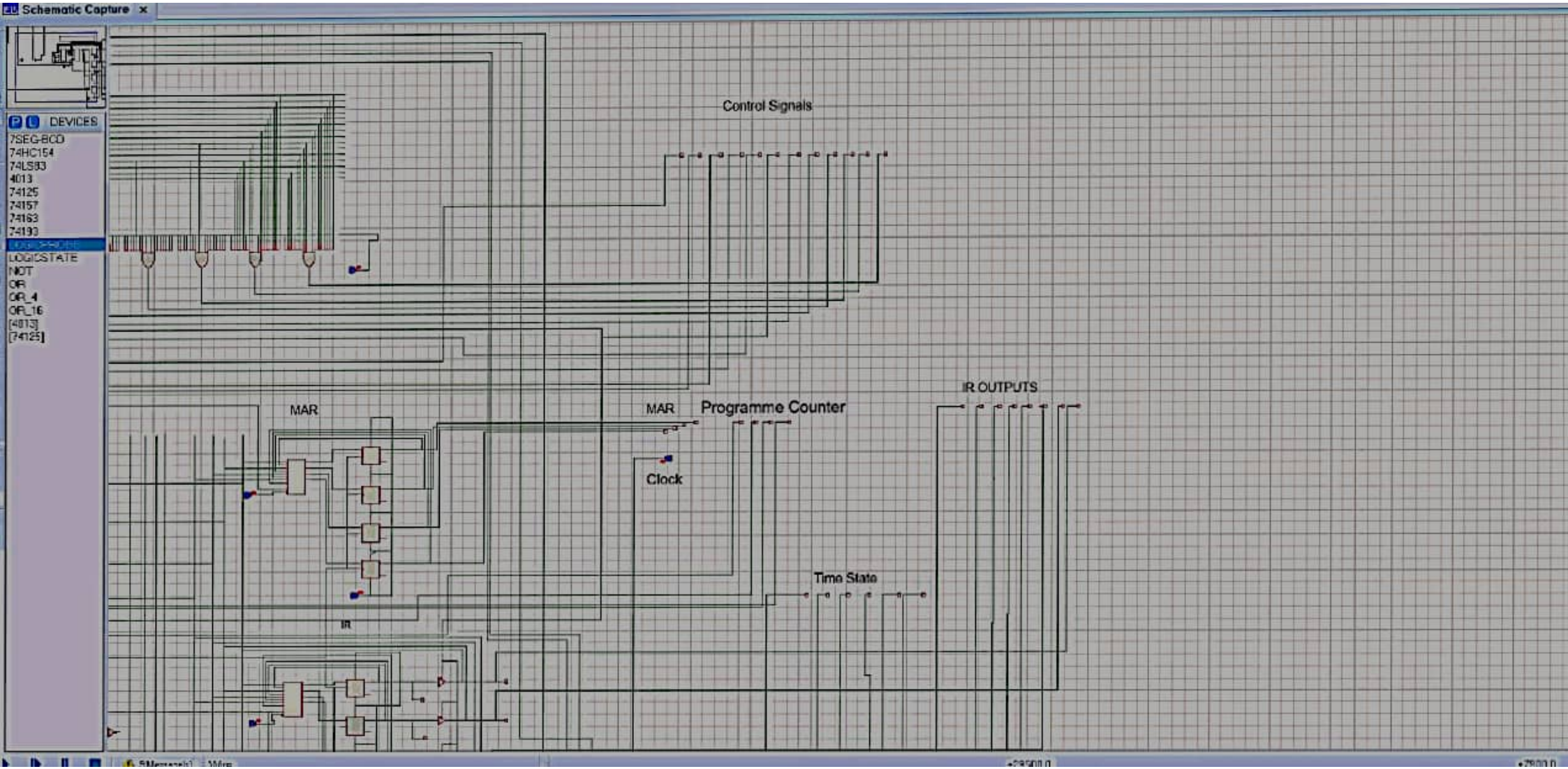
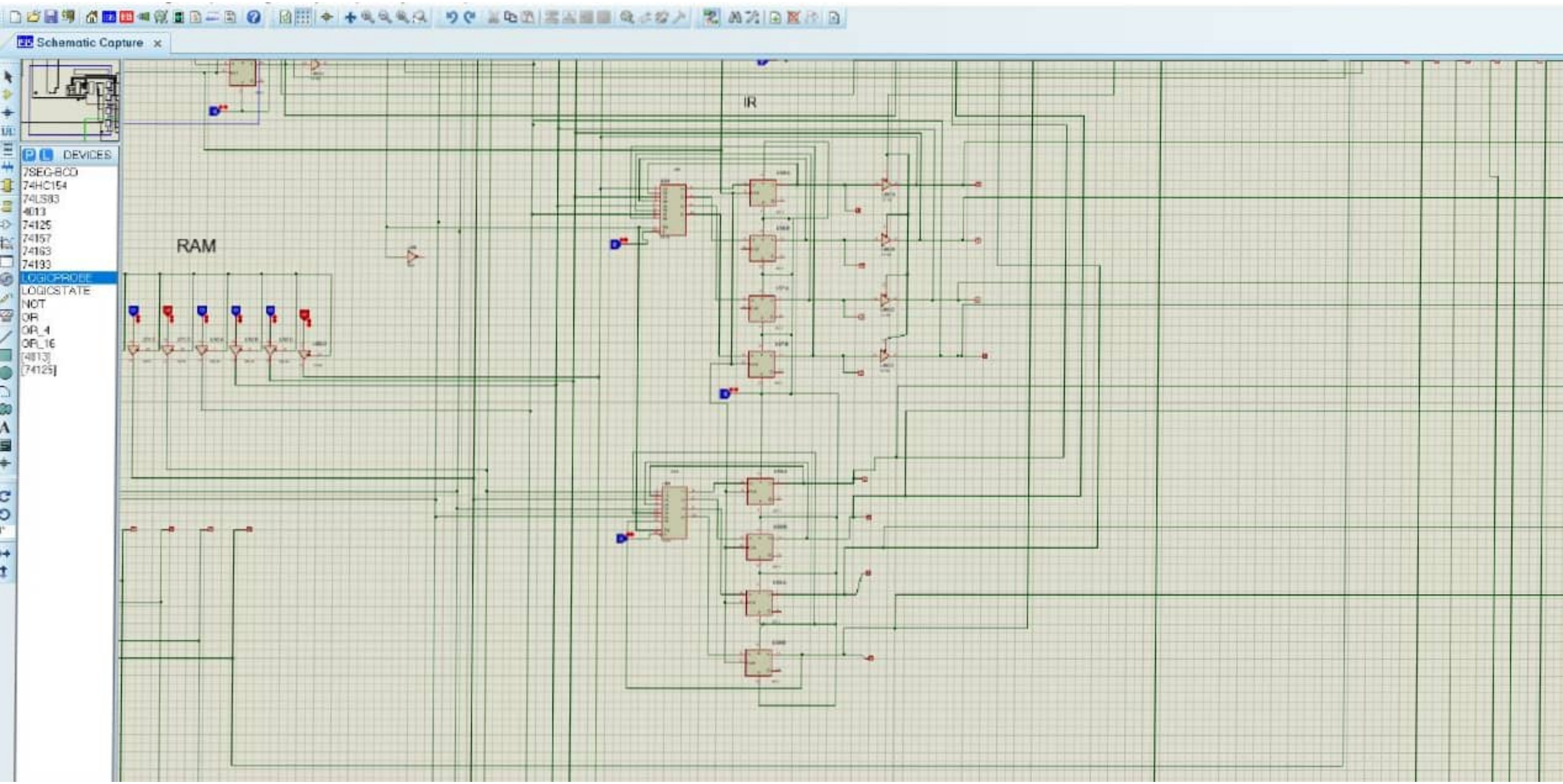


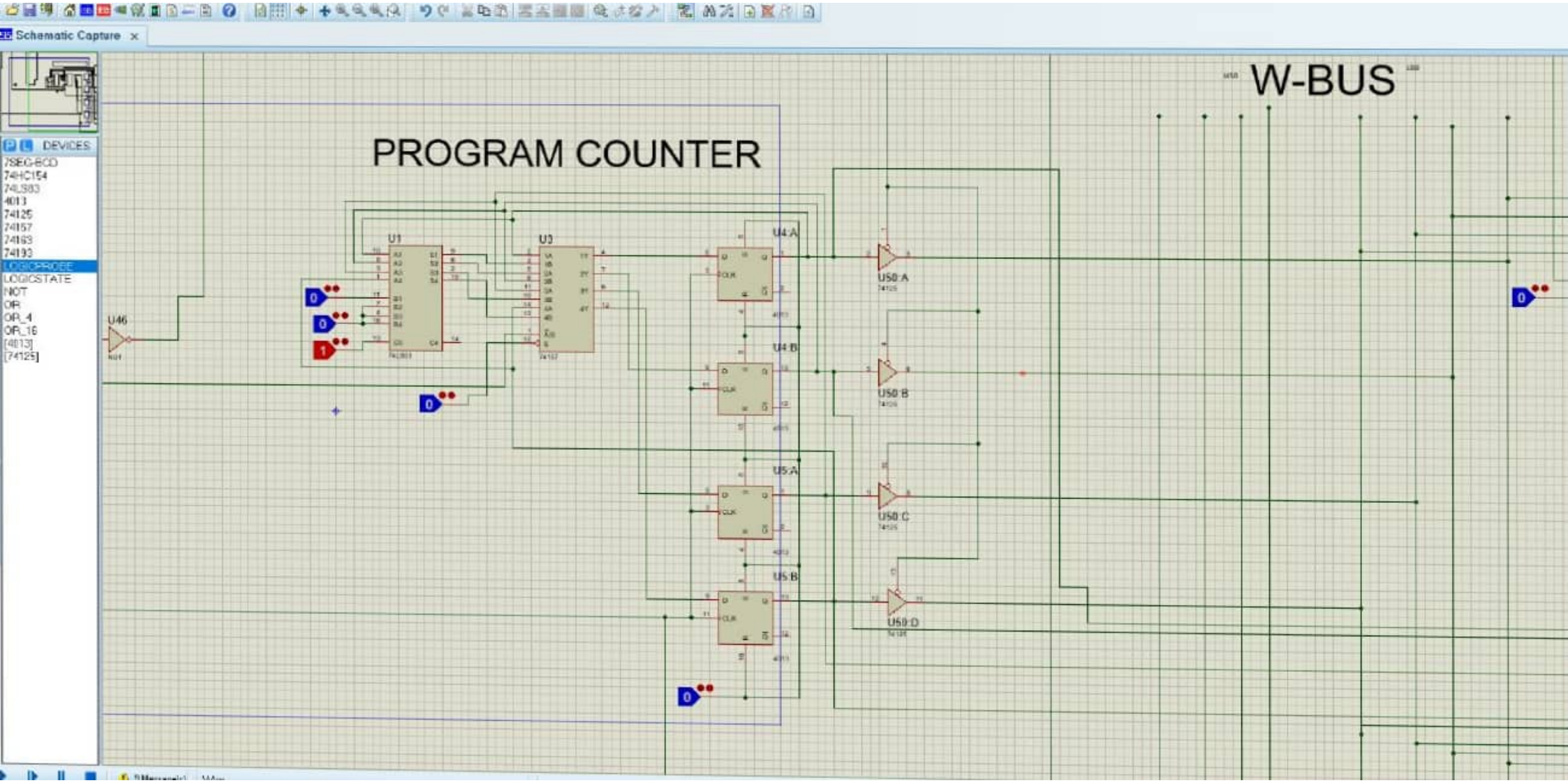

fig: Microprogrammed Control of SAP 1.

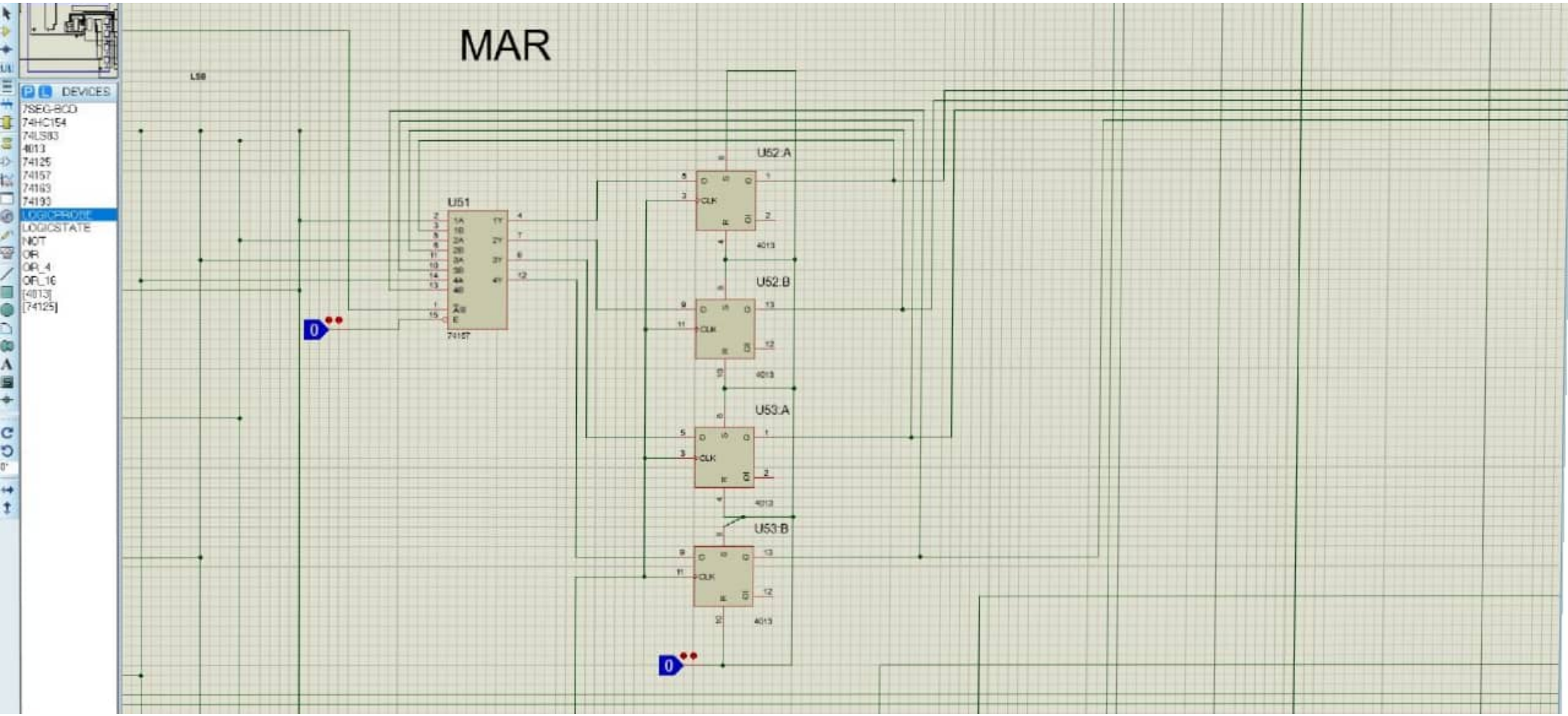
Ring Counter:

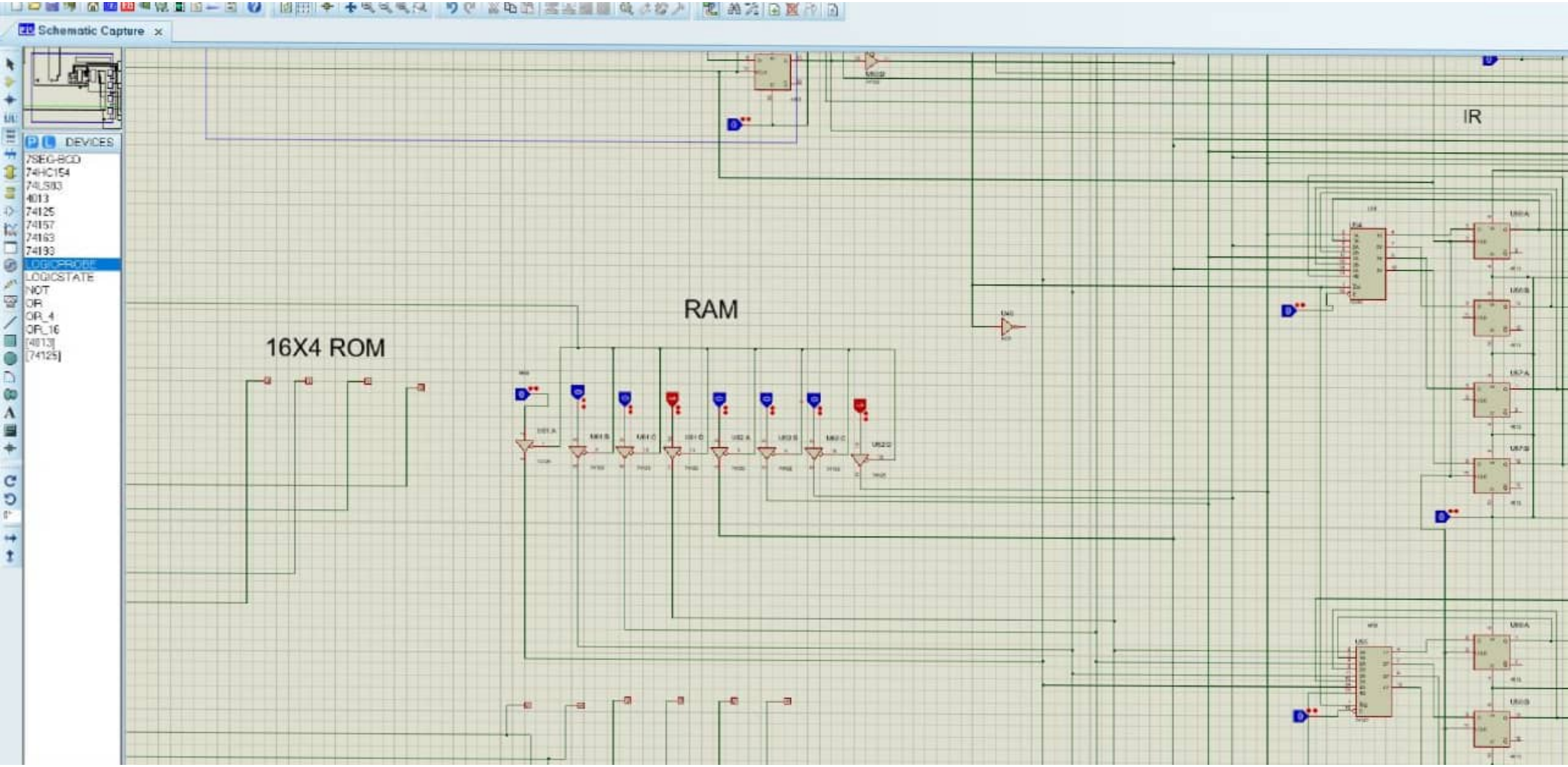


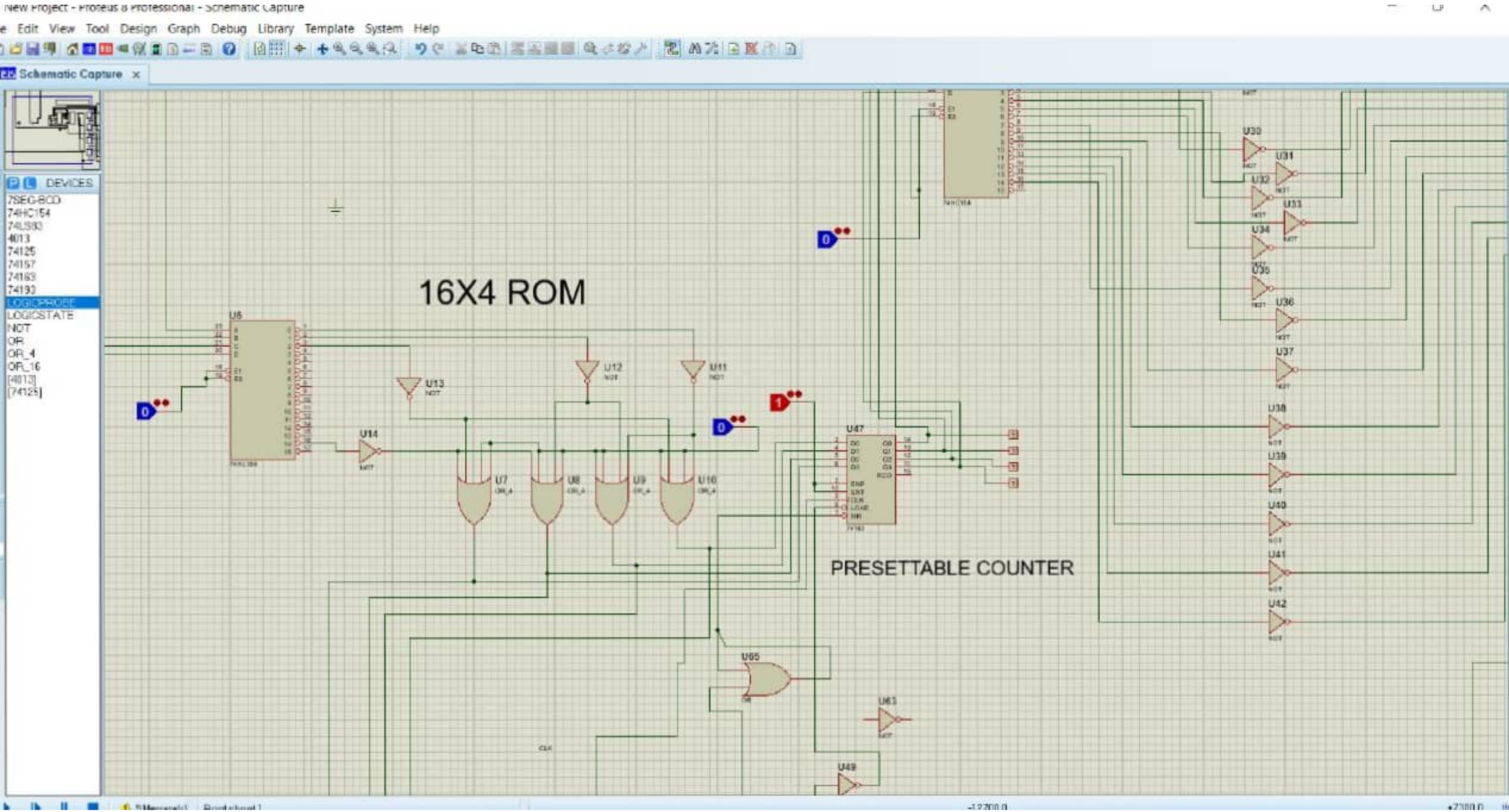

Schematic Capture
DEVICES
7SEG-BCD
74HC154
74LS83
4013
74125
74157
74163
74193
LOGICSTATE
NOT
OR
OR_4
OR_16
[4013]
[74125]
Control Signals
MAR
MAR
Programme Counter
IR OUTPUTS
Clock
Time State
IR

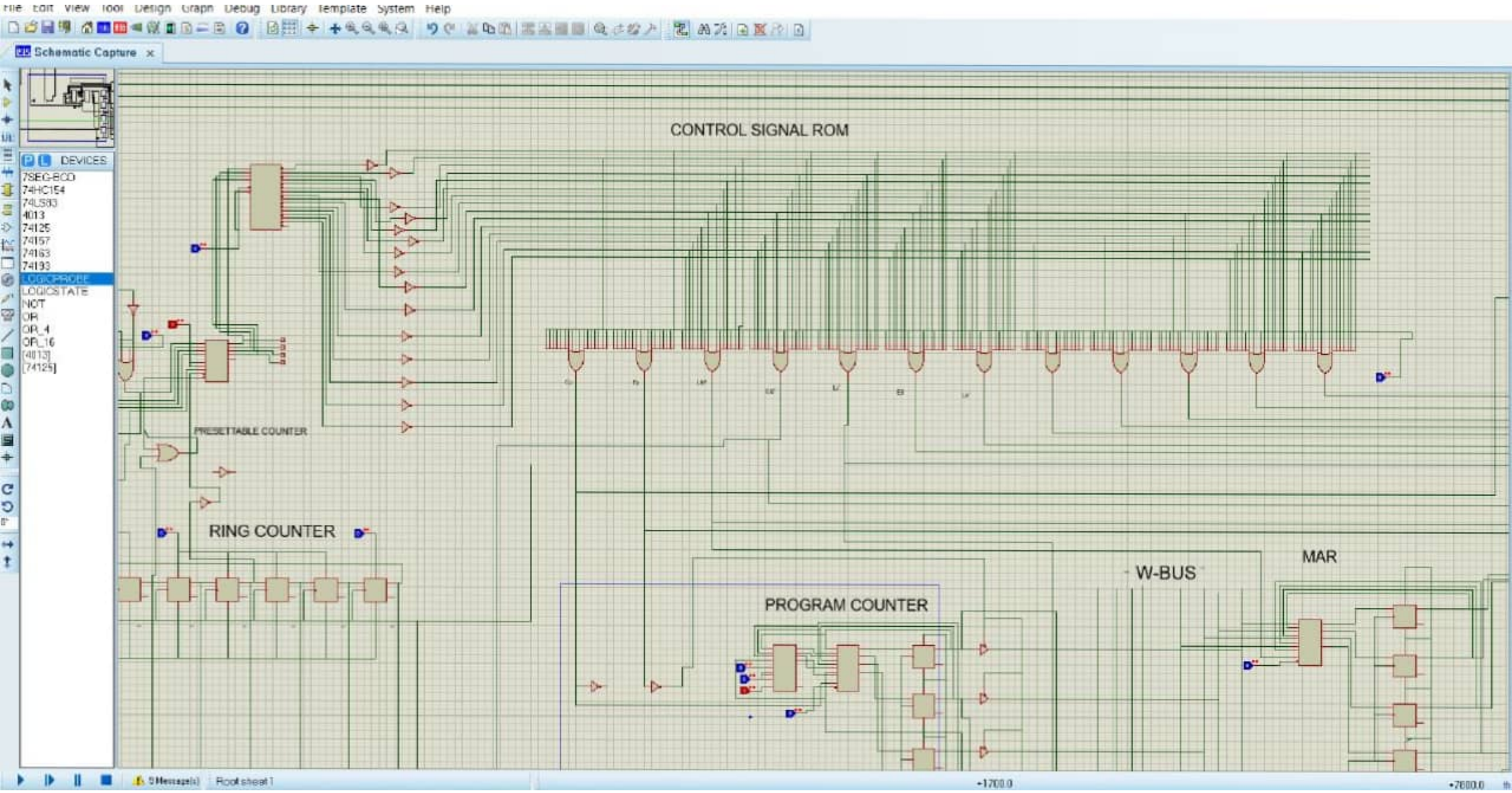

Schematic Capture
DEVICES
7SEG-BCD
74HC154
74LS83
4013
74125
74157
74163
74193
LOGICPROBE
LOGICSTATE
NOT
OR
OR_4
OR_16
[4013]
[74125]
RAM
IR

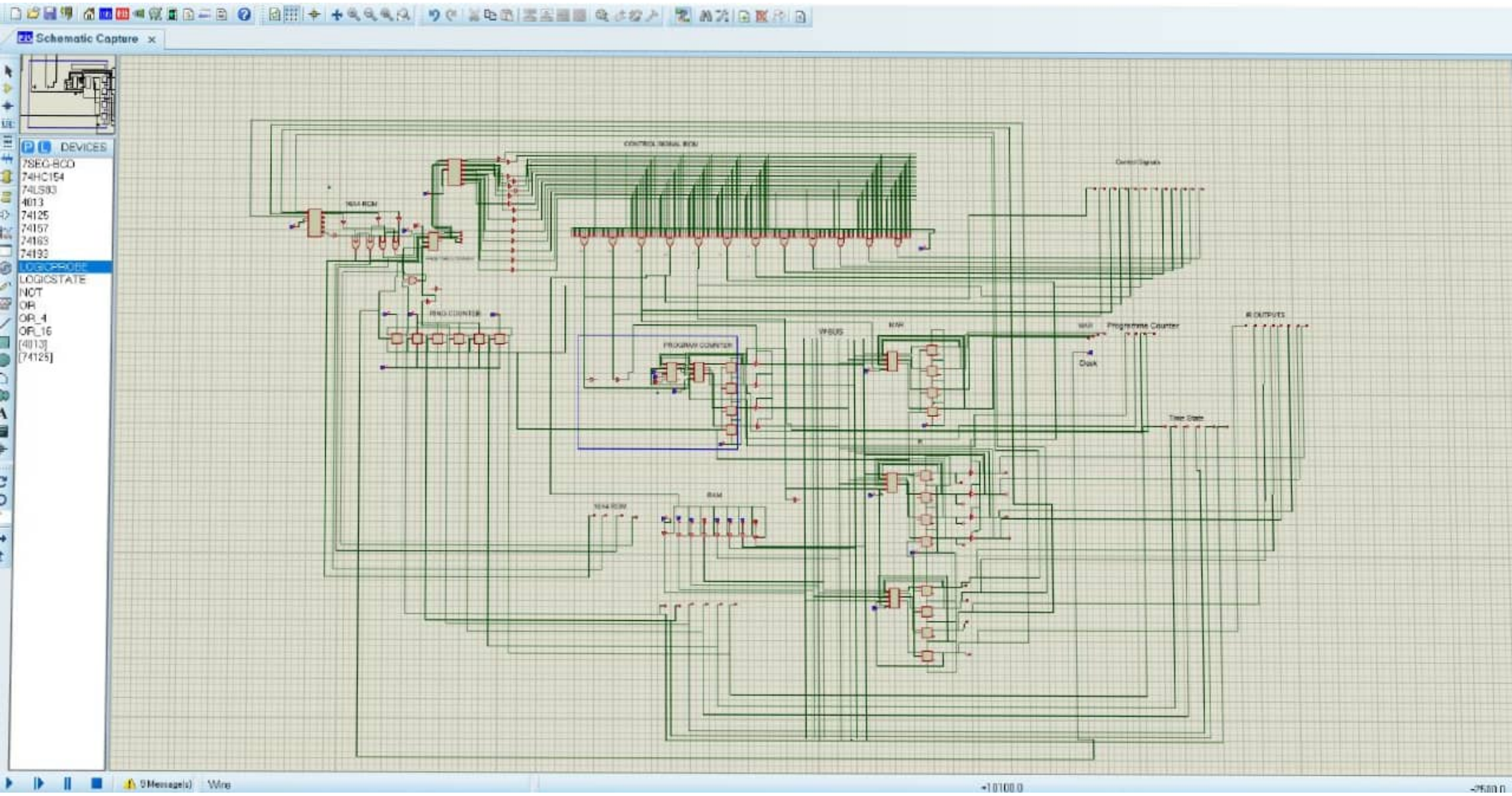

Schematic Capture
DEVICES
7SEG-BCD
74HC154
74LS83
4013
74125
74157
74163
74193
LOGICPROBE
LOGICSTATE
NOT
OR
OR_4
OR_16
[4013]
[74125]
PROGRAM COUNTER
W-BUS
U1
U3
U4:A
U4:B
U5:A
U5:B
U46
U50:A
U50:B
U50:C
U50:D
0
0
1
0
0
0


MAR
DEVICES
7SEG-BCD
74HC154
74LS83
4013
74125
74157
74163
74193
LOGICPROBE
LOGICSTATE
NOT
OR
OR_4
OR_16
[4013]
[74125]
U51
74157
U52:A
U52:B
U53:A
U53:B
4013
CLK
0


Schematic Capture
DEVICES
7SEG-BCD
74HC154
74LS83
4013
74125
74157
74163
74193
LOGICPROBE
LOGICSTATE
NOT
OR
OR_4
OR_16
[4013]
[74125]
16X4 ROM
RAM
IR


New Project - Proteus 8 Professional - Schematic Capture
Edit View Tool Design Graph Debug Library Template System Help
Schematic Capture
DEVICES
7SEG-BCD
74HC154
74LS93
4013
74125
74157
74163
74193
LOGICPROBE
LOGICSTATE
NOT
OR
OR_4
OR_16
[4013]
[74125]
16X4 ROM
PRESETTABLE COUNTER
U6
U7
U8
U9
U10
U11
U12
U13
U14
U30
U31
U32
U33
U34
U35
U36
U37
U38
U39
U40
U41
U42
U47
U49
U65
U83


File Edit View Tool Design Graph Debug Library Template System Help
Schematic Capture
DEVICES
7SEG-BCD
74HC154
74LS83
4013
74125
74157
74163
74193
LOGICPROBE
LOGICSTATE
NOT
OR
OR_4
OR_16
[4013]
[74125]
CONTROL SIGNAL ROM
PRESETTABLE COUNTER
RING COUNTER
PROGRAM COUNTER
W-BUS
MAR
9 Message(s)
Root sheet 1
+1700.0
+7600.0


Schematic Capture
DEVICES
7SEG-BCD
74HC154
74LS83
4013
74125
74157
74163
74193
LOGICPROBE
LOGICSTATE
NOT
OR
OR_4
OR_16
[4013]
[74125]
CONTROL SIGNAL ROM
Control Signals
RING COUNTER
PROGRAM COUNTER
W BUS
RAM
Clock
Programme Counter
IR OUTPUTS
Time State
ALU
0 Message(s)
Wire

Conclusion:

There are some advantages of SAP-1 like flexibility. The architecture of SAP-1 is 8 bits of data bus and compromised of 16X8 memory. Therefor 16 memory location. It needs 4 address lines which either comes from PC during computer run phase or may come from the 4 addresses switches during the program phase. These features of SAP-1 allows to make complex operations done.