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## Experiment 2.3

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**Branch: CSE**

**Semester: 4th**

**Subject Name: MPI Lab**

**UID: 20BCS1812**

**Section/Group: 607A**

**Date of Performance: 28/03/2022**

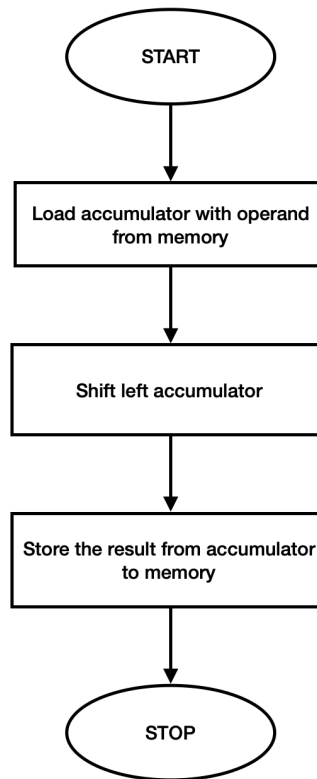
**Subject Code: 22E-20CSP-253**

**1) Aim/Overview of the practical:**

**a) Shift left by 1 bit of 8bit number**

**Apparatus/Simulator used: 8085 simulator**

## Flowchart:



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**Algorithm:**

1. **LDA 5050** loads H-L pair with data from 5050H memory location.
2. **RAL** shifts 1bit to left of accumulator.
3. **STA 5051** stores result at the memory location 5051H.
4. **HLT** end of the execution.

**Steps for experiment/practical/Code:**

**#BEGIN 0000H**

**LDA 5050H**

**RAL**

**STA 5051H**

**HLT**

**#ORG 5050H**

**#DB 59H**



### 3. REGISTERS:

Registers :										
Register	Value	7	6	5	4	3	2	1	0	
Accumulator	B2	1	0	1	1	0	0	1	0	
Register B	00	0	0	0	0	0	0	0	0	
Register C	00	0	0	0	0	0	0	0	0	
Register D	00	0	0	0	0	0	0	0	0	
Register E	00	0	0	0	0	0	0	0	0	
Register H	00	0	0	0	0	0	0	0	0	
Register L	00	0	0	0	0	0	0	0	0	
Memory(M)	3A	0	0	1	1	1	0	1	0	

Resister	Value	S	Z	*	AC	*	P	*	CY	
Flag Resister	00	0	0	0	0	0	0	0	0	

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	B200
Program Counter(PC)	0007
Clock Cycle Counter	40
Instruction Counter	5

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction							
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0



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## RESULT

BEFORE EXECUTION:

5050H: 59

AFTER EXECUTION:

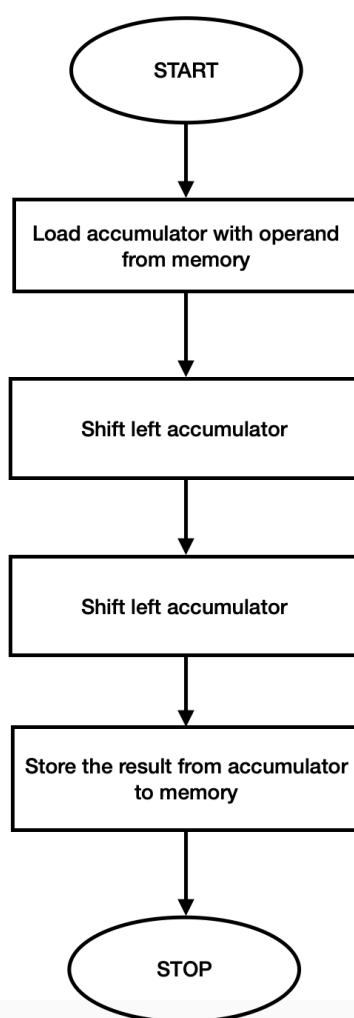
5051H: B2

**Aim/Overview of the practical:**

**b) Shift left by 2 bit of 8bit number.**

**Apparatus/Simulator used: 8085 simulator**

**Flowchart:**





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**Algorithm:**

- 1. LDA 5050 loads H-L pair with data from 5050H memory location.**
- 2. RAL shifts 1bit to left of accumulator.**
- 3. RAL shifts 1bit to left of accumulator.**
- 4. STA 5051 stores result at the memory location 5051H.**
- 5. HLT end of the execution.**

**Steps for experiment/practical/Code:**

**#BEGIN 0000H**

**LDA 5050H**

**RAL**

**RAL**

**STA 5051H**

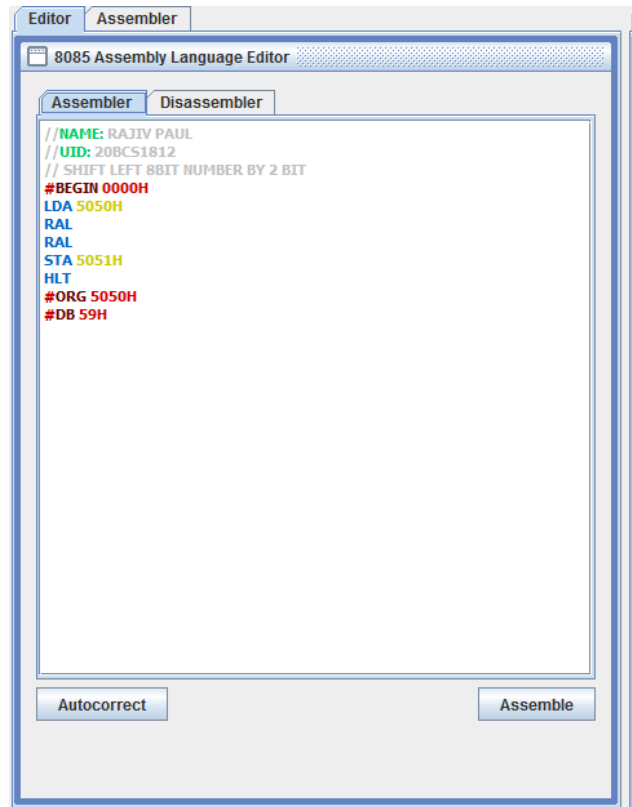
**HLT**

**#ORG 5050H**

**#DB 59H**

## Simulation:

### 1. CODE IN EDITOR WINDOW:





### 3. REGISTERS:

Registers
Memory
Devices

☐ Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	64	0	1	1	0	0	1	0	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	3A	0	0	1	1	1	0	1	0

Register	Value	S	Z	*	AC	*	P	*	CY
Flag Register	01	0	0	0	0	0	0	0	1

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	6401
Program Counter(PC)	0008
Clock Cycle Counter	44
Instruction Counter	6

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

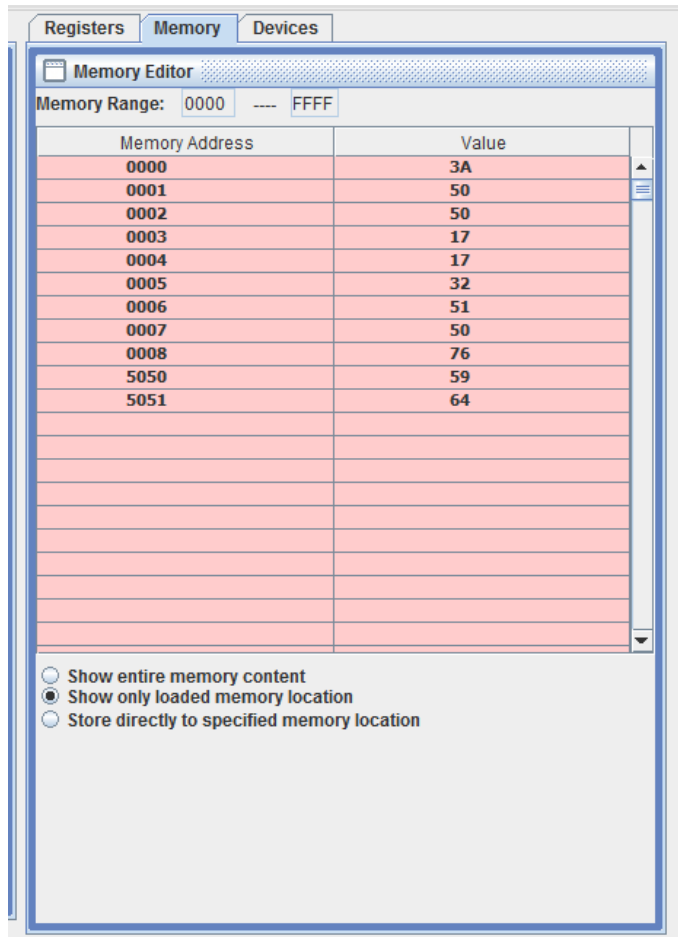
SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

#### 4. MEMORY:



The Memory Editor window displays a table of memory addresses and values. The table has two columns: 'Memory Address' and 'Value'. The 'Memory Range' is set to '0000' to 'FFFF'. The table contains the following data:

Memory Address	Value
0000	3A
0001	50
0002	50
0003	17
0004	17
0005	32
0006	51
0007	50
0008	76
5050	59
5051	64

Below the table, there are three radio buttons for selection:

- ☐ Show entire memory content
- ☒ Show only loaded memory location
- ☐ Store directly to specified memory location

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## RESULT

BEFORE EXECUTION:

5050H: 59

AFTER EXECUTION:

5051H: 64

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**Learning outcomes (What I have learnt):**

- 1.Learnt about 8085 simulator**
- 2. Learnt how to shift left by 1bit and 2bit of 8bit number.**
- 3. Learnt about RAL and its function.**
- 4.**
- 5.**

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**Evaluation Grid (To be created as per the SOP and Assessment guidelines by the  
faculty):**

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Sr. No.	Parameters	Marks Obtained	Maximum Marks
1.			
2.			
3.			