CONESTOGA
Connect Life and Learning

EECE 8000

Lab3

Objectives:

- Realizing an issue in real life.
- Implementing a solution.
- Implementing your design in Quartus II, using VHDL file.
- Connecting your FPGA.

Procedure:

Consider the following parking control system:

A parking lot is constructed of 6 levels, each level has 16 parking spaces. At the entrance there is red light indicator. When all the parking spaces (in the 6 levels) are occupied the red light indictor is ON and the green Light indicator is OFF, when there is an available parking space at any level the red light indictor is OFF and the green light indicator is ON.

Hint: This is a two stages design, you need to design only the second stage.

1. Create a new project targeting your FPGA (follow naming criteria)
2. Create a top level VHDL file containing 6 switch inputs, and 1 led Red output.
3. For the Library section you will need:
   library IEEE;
   use IEEE.STD_LOGIC_1164.ALL;

4. For the Entity section, use the following information:
   SW [0:5] – Input Switches.
   LEDR [2] – Red Output indicator.
   LEDG [3] – Green Output indicator.

5. In the architecture section, in a process block sensitive to the switch inputs, describe combinational logic for the system.
6. From the Processing menu, run Start->Start Analysis & Synthesis
7. Assign the LED and SW pins from Assignments -> Pin Planner
8. Place and route the design using Processing ->Start Compilation.
9. Download your design to your FPGA .
10. When your design is working on the FPGA, demonstrate it to the instructor.