Digital Design Principles

Octal Decoder

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Objective:

- Explore the use of concurrent constructs to model combinational logic circuits.
- Model an octal decoder circuit using conditional assignment.

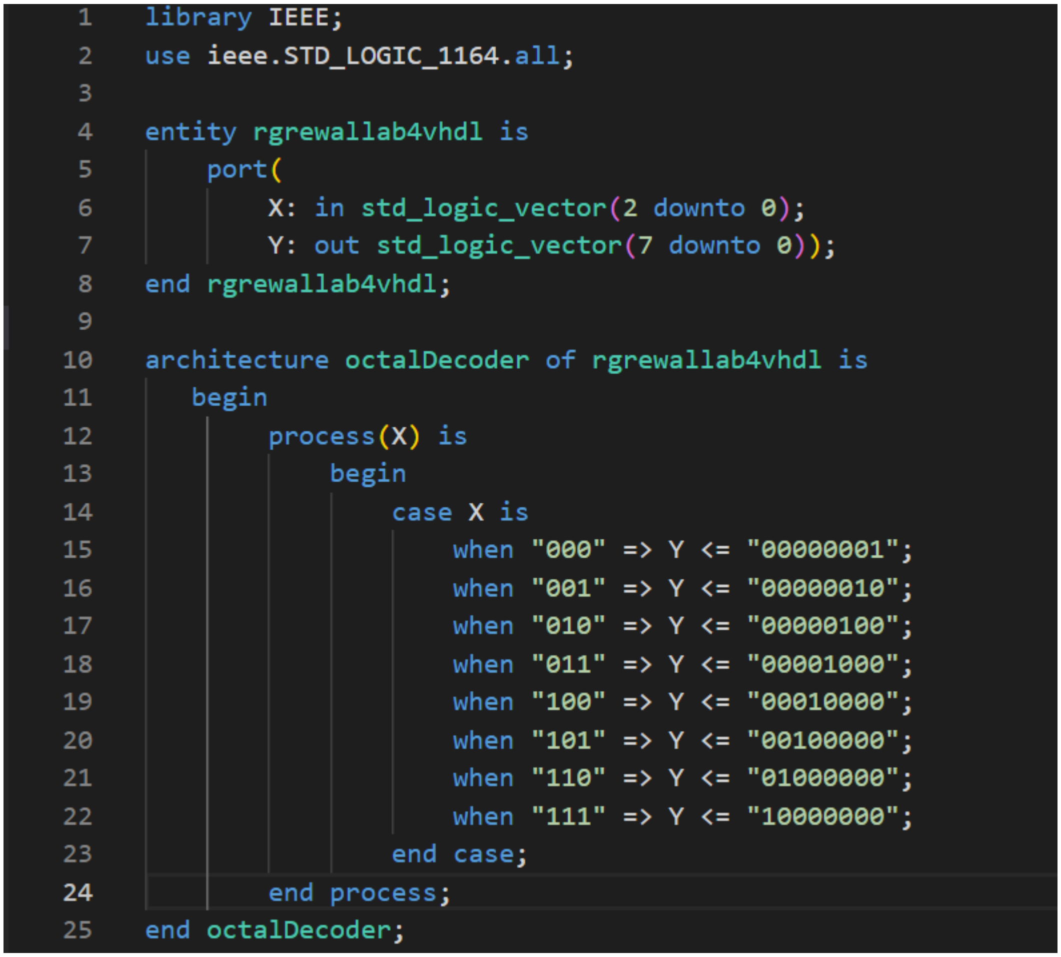
Truth Table:

X2	X1	X0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

VHDL Introduction:

To make the program in VHDL we will need to initialize the library and entity. Within the entity we will state the 3 input switches and the 8 output LEDs. Within the architecture of the program we will use case and when statement. Where for each different state the three inputs are the according led will be set to light up. The above truth table is the be followed to know which led is to be set accordingly.

VHDL program screenshot:

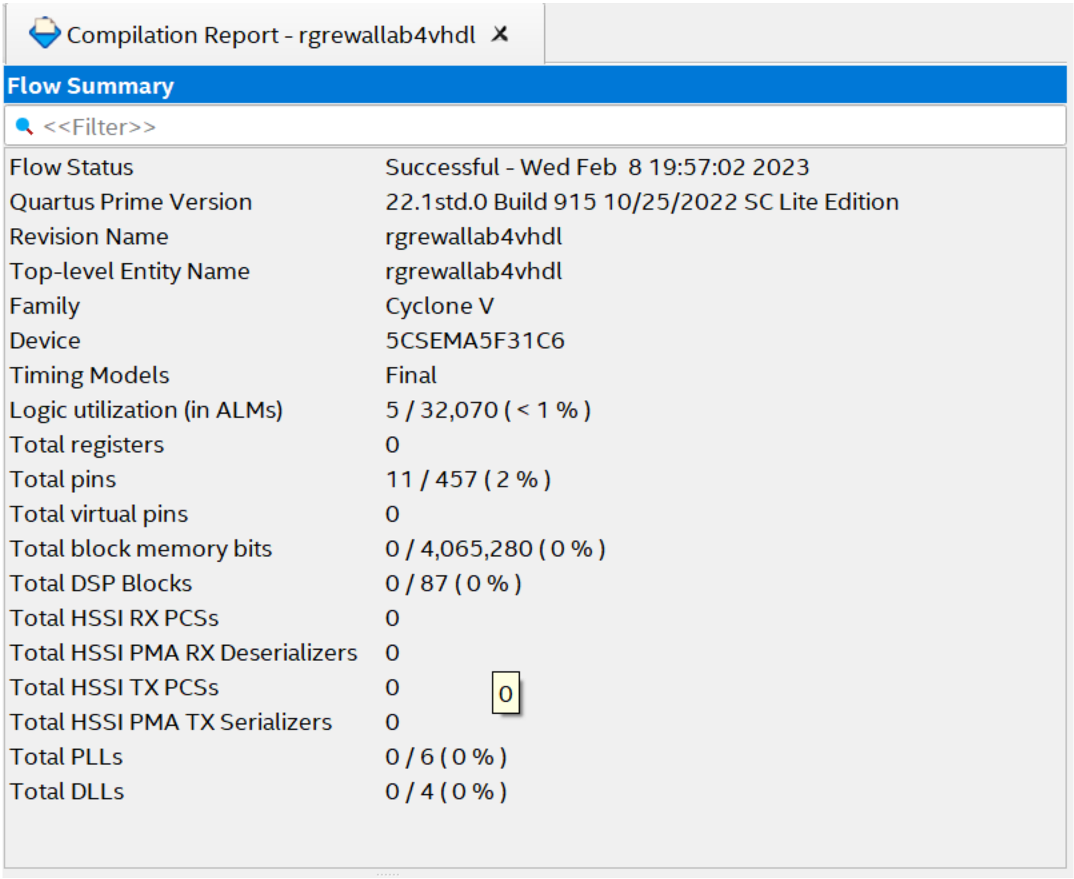


```
library IEEE;
use ieee.STD_LOGIC_1164.all;

entity rgrewallab4vhdl is
    port(
        X: in std_logic_vector(2 downto 0);
        Y: out std_logic_vector(7 downto 0));
end rgrewallab4vhdl;

architecture octalDecoder of rgrewallab4vhdl is
   begin
        process(X) is
            begin
                case X is
                    when "000" => Y <= "00000001";
                    when "001" => Y <= "00000010";
                    when "010" => Y <= "00000100";
                    when "011" => Y <= "00001000";
                    when "100" => Y <= "00010000";
                    when "101" => Y <= "00100000";
                    when "110" => Y <= "01000000";
                    when "111" => Y <= "10000000";
                end case;
        end process;
end octalDecoder;
```

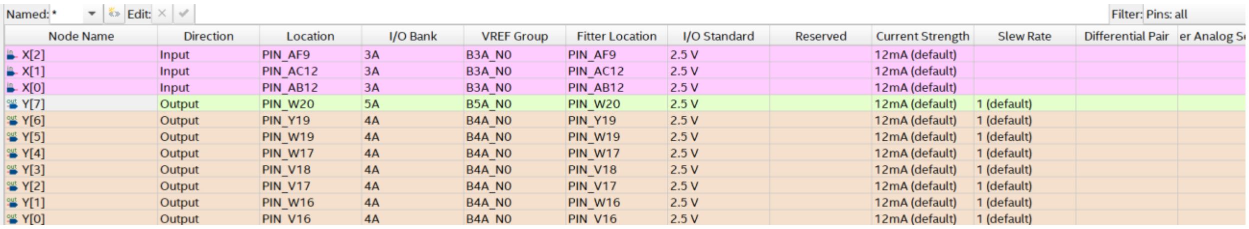
VHDL compilation report:



Flow Summary

Flow Status	Successful - Wed Feb 8 19:57:02 2023
Quartus Prime Version	22.1std.0 Build 915 10/25/2022 SC Lite Edition
Revision Name	rgrewallab4vhdl
Top-level Entity Name	rgrewallab4vhdl
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	5 / 32,070 (< 1 %)
Total registers	0
Total pins	11 / 457 (2 %)
Total virtual pins	0
Total block memory bits	0 / 4,065,280 (0 %)
Total DSP Blocks	0 / 87 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

Pin Planner screenshot:



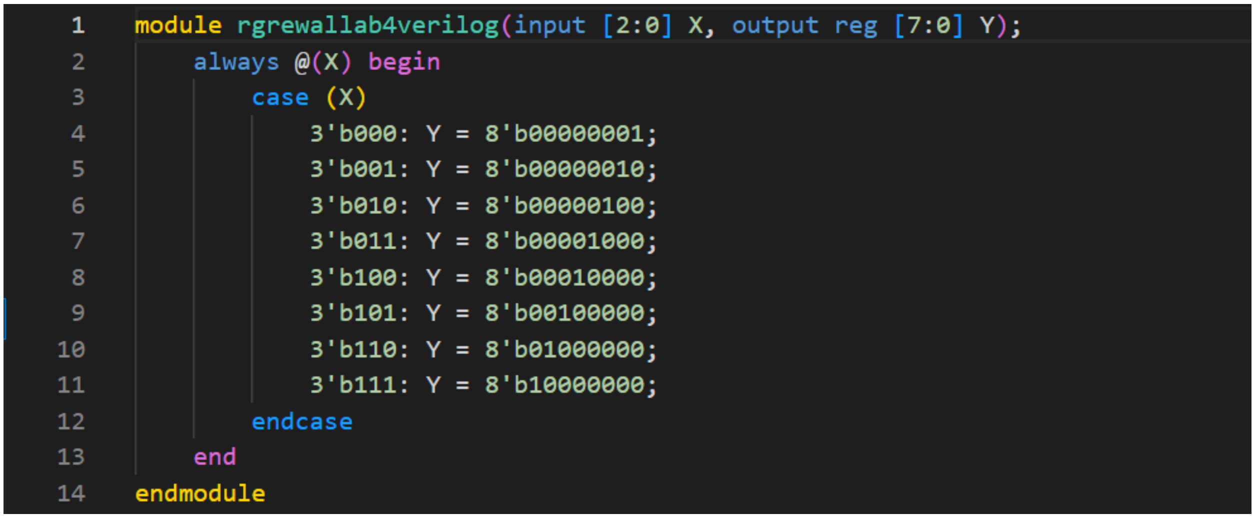
Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	er Analog S
X[2]	Input	PIN_AF9	3A	B3A_N0	PIN_AF9	2.5 V		12mA (default)			
X[1]	Input	PIN_AC12	3A	B3A_N0	PIN_AC12	2.5 V		12mA (default)			
X[0]	Input	PIN_AB12	3A	B3A_N0	PIN_AB12	2.5 V		12mA (default)			
Y[7]	Output	PIN_W20	5A	B5A_N0	PIN_W20	2.5 V		12mA (default)	1 (default)		
Y[6]	Output	PIN_Y19	4A	B4A_N0	PIN_Y19	2.5 V		12mA (default)	1 (default)		
Y[5]	Output	PIN_W19	4A	B4A_N0	PIN_W19	2.5 V		12mA (default)	1 (default)		
Y[4]	Output	PIN_W17	4A	B4A_N0	PIN_W17	2.5 V		12mA (default)	1 (default)		
Y[3]	Output	PIN_V18	4A	B4A_N0	PIN_V18	2.5 V		12mA (default)	1 (default)		
Y[2]	Output	PIN_V17	4A	B4A_N0	PIN_V17	2.5 V		12mA (default)	1 (default)		
Y[1]	Output	PIN_W16	4A	B4A_N0	PIN_W16	2.5 V		12mA (default)	1 (default)		
Y[0]	Output	PIN_V16	4A	B4A_N0	PIN_V16	2.5 V		12mA (default)	1 (default)		

Verilog introduction:

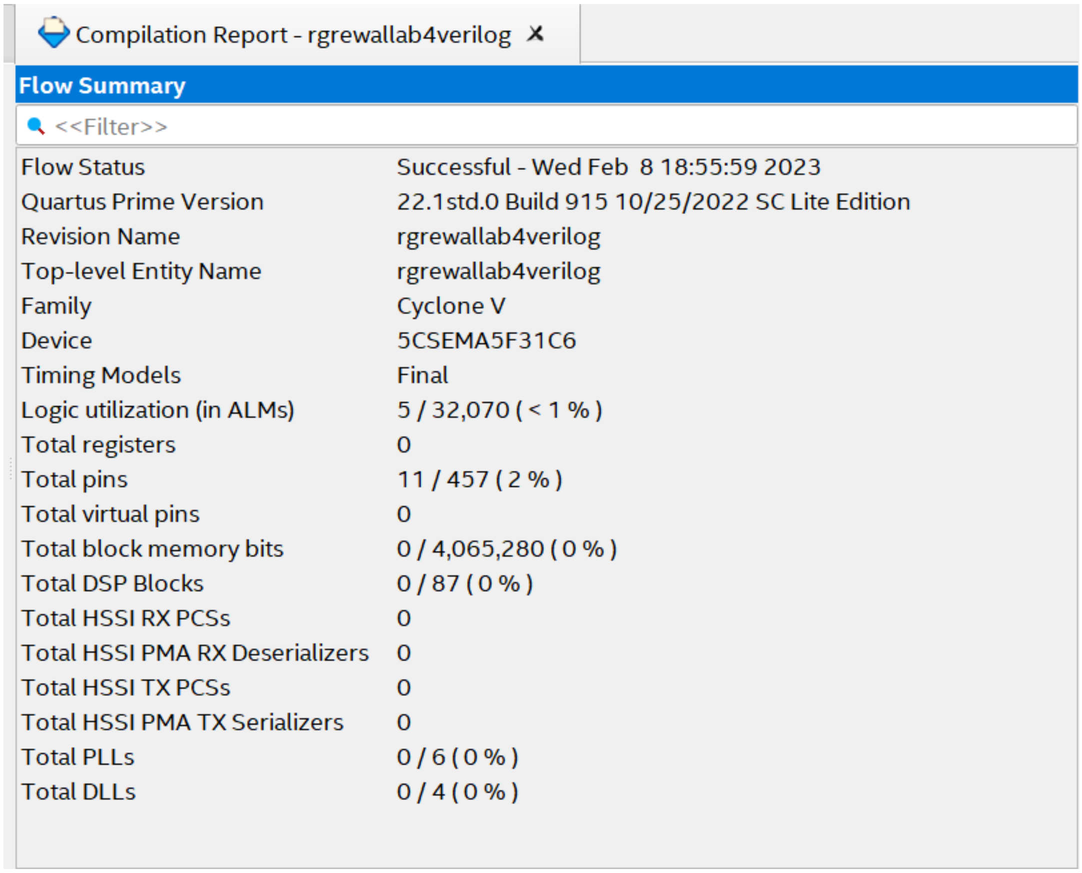
For the program in Verilog we will need to initialize the module with the parameters having the three inputs and eight outputs. Within the module block we use case where the output will assign the value according to the state of the input which matches to the truth table.

Verilog program screenshot:



```
module rgrewallab4verilog(input [2:0] X, output reg [7:0] Y);
    always @(X) begin
        case (X)
            3'b000: Y = 8'b00000001;
            3'b001: Y = 8'b00000010;
            3'b010: Y = 8'b00000100;
            3'b011: Y = 8'b00001000;
            3'b100: Y = 8'b00010000;
            3'b101: Y = 8'b00100000;
            3'b110: Y = 8'b01000000;
            3'b111: Y = 8'b10000000;
        endcase
    end
endmodule
```

Verilog compilation report:



Flow Status	Successful - Wed Feb 8 18:55:59 2023
Quartus Prime Version	22.1std.0 Build 915 10/25/2022 SC Lite Edition
Revision Name	rgrewallab4verilog
Top-level Entity Name	rgrewallab4verilog
Family	Cyclone V
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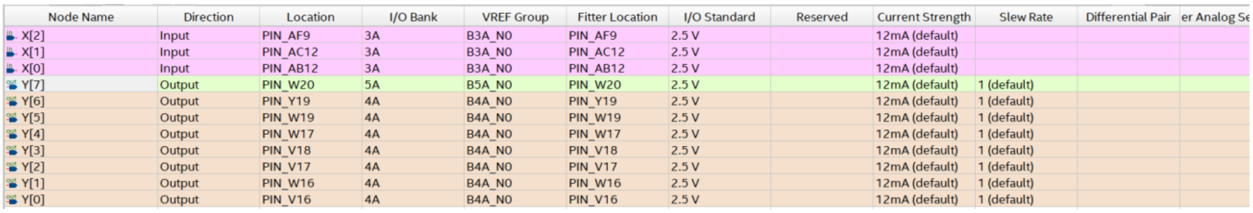
Verilog pin planner screenshot:



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Y[4]	Output	PIN_W17	4A	B4A_N0	PIN_W17	2.5 V		12mA (default)	1 (default)		
Y[3]	Output	PIN_V18	4A	B4A_N0	PIN_V18	2.5 V		12mA (default)	1 (default)		
Y[2]	Output	PIN_V17	4A	B4A_N0	PIN_V17	2.5 V		12mA (default)	1 (default)		
Y[1]	Output	PIN_W16	4A	B4A_N0	PIN_W16	2.5 V		12mA (default)	1 (default)		
Y[0]	Output	PIN_V16	4A	B4A_N0	PIN_V16	2.5 V		12mA (default)	1 (default)		

Conclusion:

Thus we can conclude that by both the programming languages we will use case statement and the one led which corresponds to the input will light up. The above truth table will be followed thus creating our octal decorder.