FINAL PROJECT

Second Progress Report – Palindrome Detection

INTRO TO VLSI DESIGN

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New Design Decisions:

Proceeding further from last progress report no significant new design alterations were made. The design suggested is the last progress report was implemented in magic using standard cells. The only design change was that we omitted the reset signal as the standard cells used for slip flops did not use them.

Bit slice design and Magic Implementation:

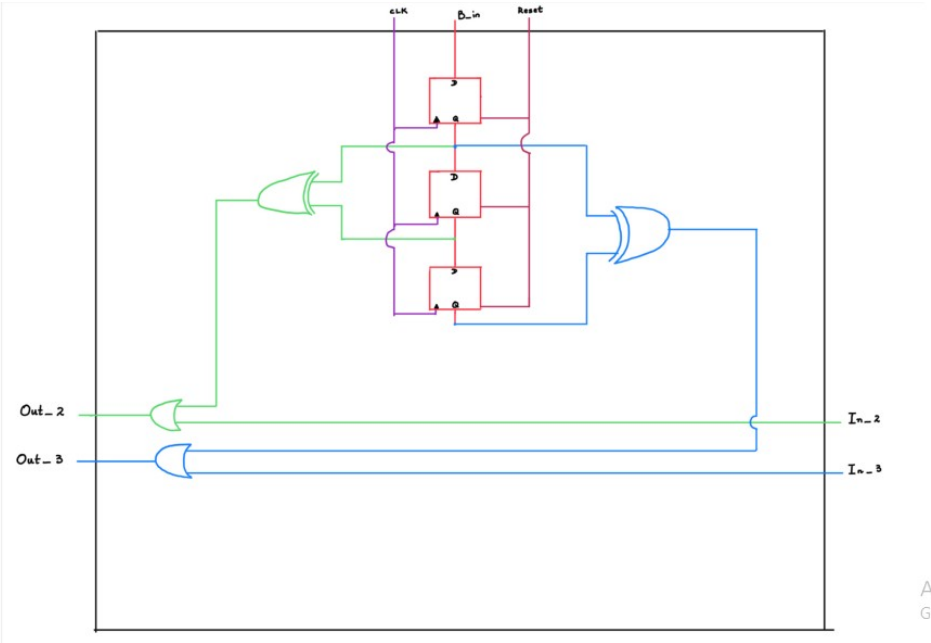

Fig 1.0

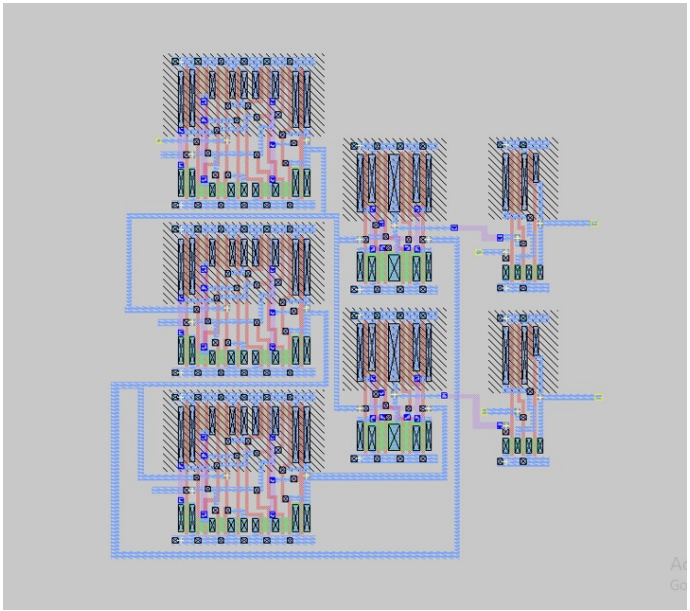

Fig 1.1

Complete chip design and layout:

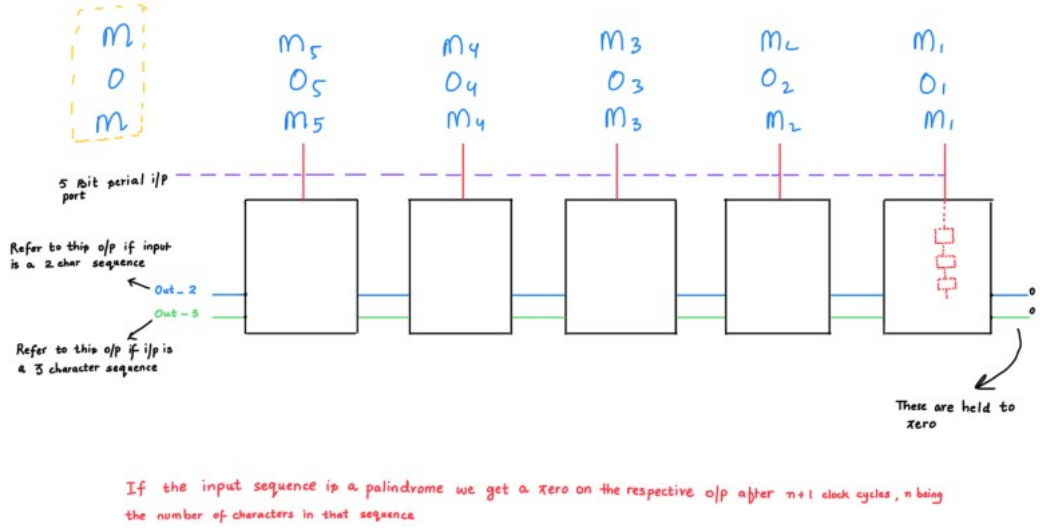

Fig 2.0

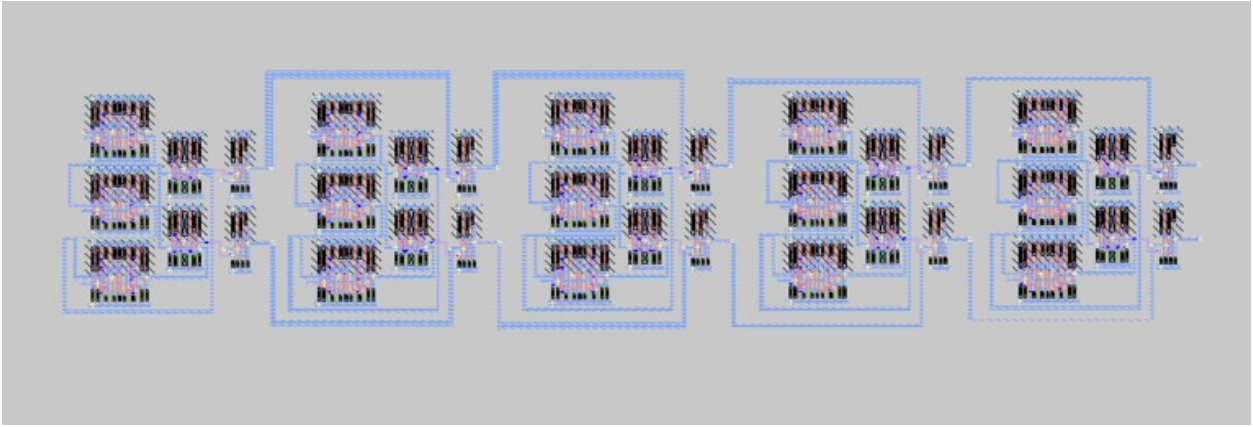

Fig 2.1

A single bit slice layout was first designed in magic as shown in fig 1.0 and then later the design was replicated to match the logic presented in fig 2.0. The final layout *(yet to be placed in the pad)* is shown in fig 2.1. It should be noted that the input to the first bit slice are held to zero, therefore the two metal wires on the right in figure 2.1 are left floating to represent these zero inputs here.

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Chip Pin design:

Below we have our chip design showing the routing between the bit slices *(bit slices shown in red)*, the output pins and the test pins. Test pins are also shown. Some of the pin decisions are yet to be finalized.

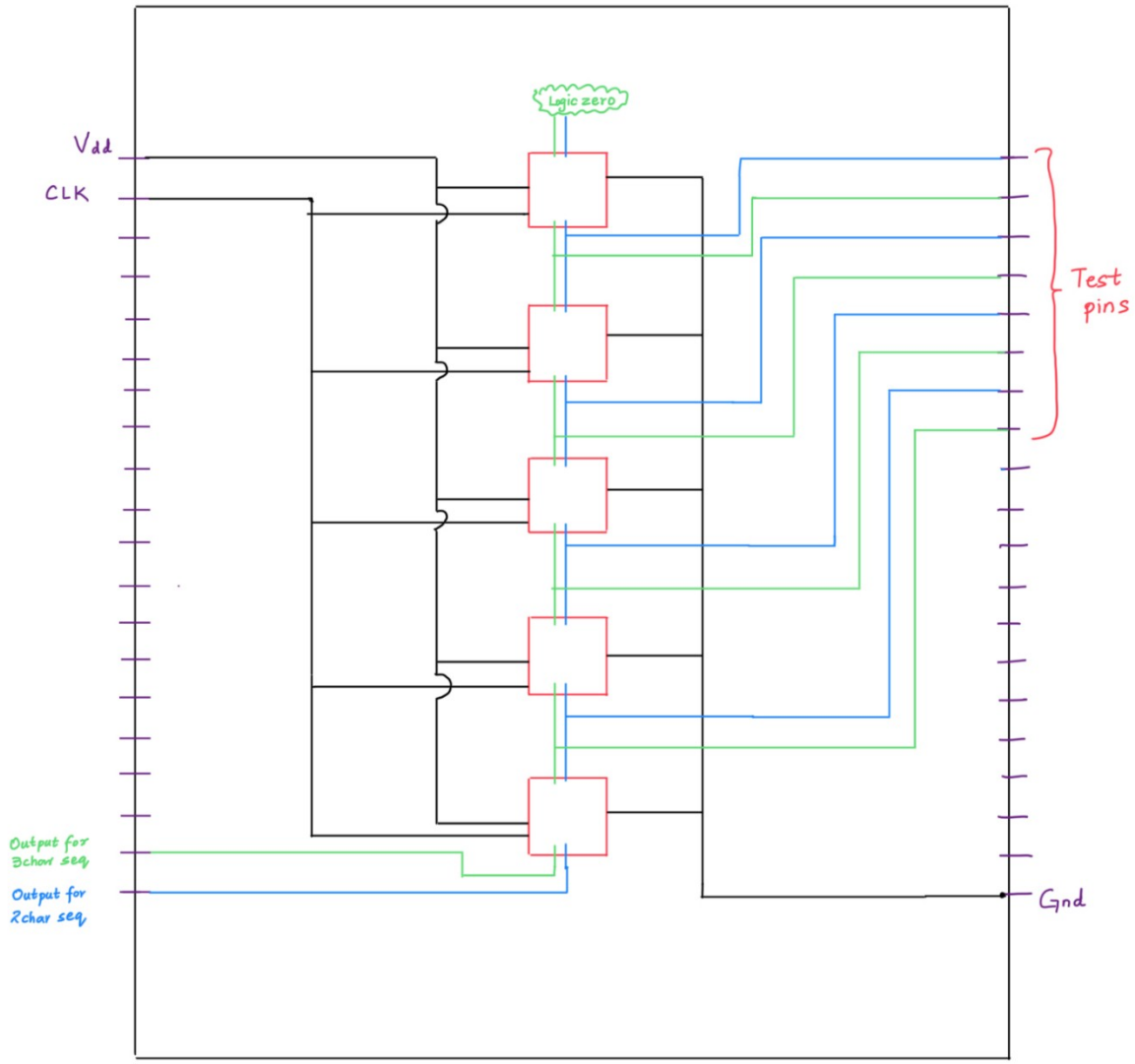


Fig 3.0

Pad layout:

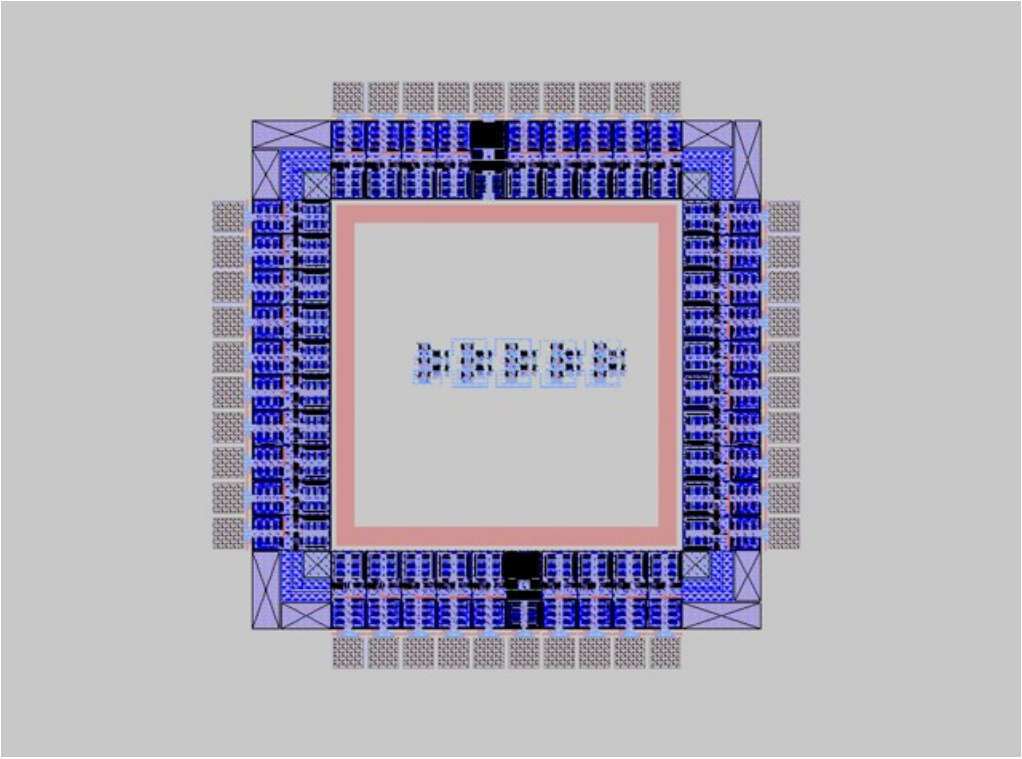


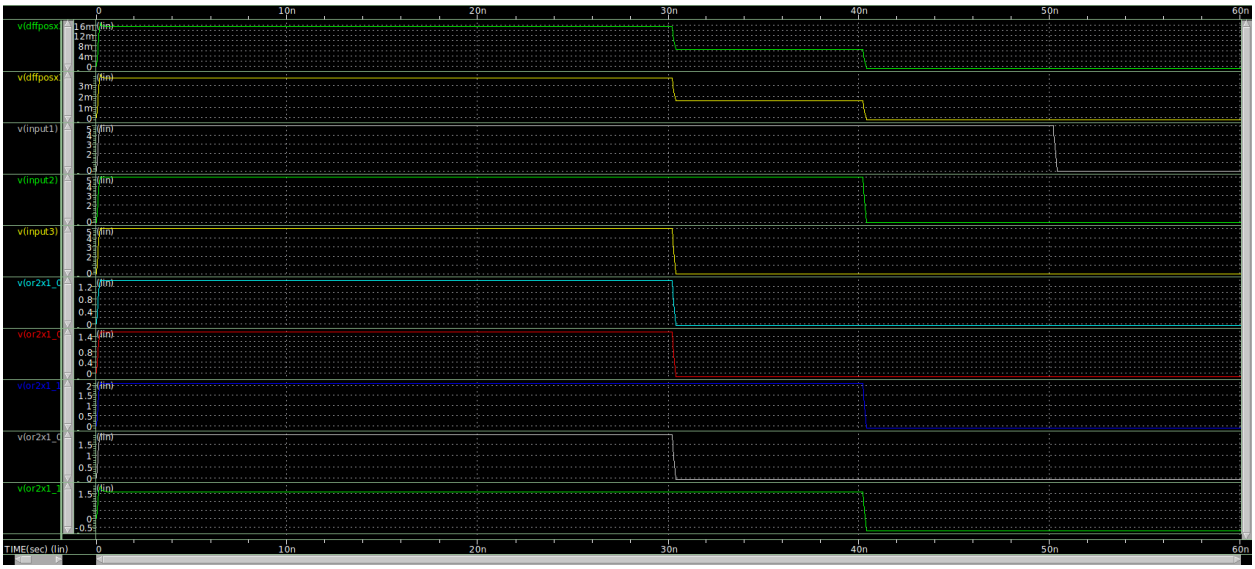
Fig 4.0

This is an arbitrary pad layout to just give an idea of what we are thinking. The connections are still to be made.

IRSIM/Spice and VHDL back annotation.

After the magic layout for the bit slices were completed, we extracted IRSIM/Spice files but for some reason IRSIM tool has not been working. We are in coordination to resolve this issue. The spice files were simulated for bitslice. We have encountered an error while simulating for n-bit as the job was getting aborted for any combinations of Input . Each of the group member is working on either issue to rectify the problem. The complete results for this will be included in the final report.

Once Spice simulations are successful VHDL back annotations can be done accordingly.
Below is the spice simulation of the bitslice



Work Distribution;

For this report work was distributed among the group members as follows;

Task	Done By
Magic layouts	Rajkumar
Chip Layout and Diagrams	Hamza
IRSIM	Rajkumar
Spice, VHDL & report	Hamza