CC3100 and CC3200 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines

User's Guide

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June 2014–Revised September 2014

Contents

List of Figures

List of Tables

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CC3100 and CC3200 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines

Embedded Processing Applications

ABSTRACT

This document provides the design guidelines of a 4-layer PCB board, for the CC31xx and CC32xx SimpleLink Wi-Fi family of devices. The CC31xx and CC32xx are easy to lay-out QFN packaged devices. The board's performance will be optimal if the designer follows these suggestions during the board's design. The first section is a brief overview of the SimpleLink Wi-Fi family of devices. The second section focuses on the PCB specification; the third section addresses components placement, and board layer information. The last section, on layout guidelines, covers the board's main sections such as RF, power, clock, digital I/O and the ground. Each section can be read independently.

In addition to this document, TI recommends verifying the schematic board design with the associated schematic checklist. This checklist can be obtained at: http://www.ti.com/lit/zip/swru370.

1 Device Overview

Start your design with the industry's first Internet-on-a-chip™. Created for the Internet of Things (IoT), the SimpleLink Wi-Fi family has several variants. The CC3100 SimpleLink Wi-Fi and IoT solution dramatically simplifies the implementation of Internet connectivity. This product integrates all protocols for Wi-Fi and Internet, which greatly minimizes host microcontroller (MCU) software requirements. CC3200 device is a wireless MCU that integrates a high-performance ARM® Cortex®-M4 MCU with the CC3100 network processor subsystem, allowing customers to develop an entire application with a single IC. With on-chip Wi-Fi, Internet and robust security protocols, no prior Wi-Fi experience is needed for faster development. SimpleLink Wi-Fi is a complete platform solution including various tools and software, sample applications, user and programming guides, reference designs and the TI E2E™ support community. The devices are available in an easy to lay-out QFN package. The layout for both devices are similar with a higher number of IOs routed for the CC3200.

2 PCB Specification

2.1 PCB Stack-Up

An example stack-up is shown in Figure 1, used for the construction of the CC3100BOOST Rev3.3-A. The user can alter the layer stack-up based on their requirements, but the impedance of the 50 Ω lines should be recalculated. Having the L1-L2 distance reduced helps improve the grounding and the RF decoupling. TI recommends keeping the L1-L2 distance similar to the recommended value.

Type	Layer		Height(um)
Mask			25
Copper	L1		35
FR-4			255
Copper	L2		35
FR-4			350
Copper	L3		35
FR-4			255
Copper	L4		35
Mask			25
		Total	1050
Total thickness ~ 1.1mm (+/- 10%)			

Figure 1. Example Stack-up

2.2 PCB Design Rules

Table 1. PCB Design Rules

Parameter	Value	Comments
Number of layers	4	
Thickness	1.1 mm ± 10%	For greater thickness increase the distance between L2 and L3
Size of PCB	2.0” x 1.7”	
Solder mask	Red	Can be replaced with any color
Dielectric	FR4	
Silk	White	Can be replaced with any color
Surface finish	ENIG	
Min track width	6 mils	Min track width can be reduced but cost would be higher
Min spacing	6 mils	Min spacing can be reduced but the cost would be higher
Mid drill diameter	8 mils	12 mil diameter drill is used on the Rev 3.3-A board
Copper thickness	1 oz	
Lead free / ROHS	Yes	
Impedance control	Yes	50 Ω controlled impedance trace of 18 mils width on L1 w.r.t L2 (GND). Air gap = 15mils **Note**: The above calculations are based on CPW-G (NOT microstrip).
Impedance variation	5%	

2.3 Layer Information

The 4 layer PCB is used with the configuration as shown in Table 2.

Table 2. 4 Layer PCB

Layer	Usage	Notes
1	Signal + RF	RF trace is a CPW on L1 w.r.t. L2 ground
2	GND	Reference plane for RF
3	Power + signal	The power planes for the power amplifier (PA), analog blocks and the main input supply are routed on this layer
4	Power + signal	

3 Layout information

The complete layout package is available for download on the TI website at http://www.ti.com/tool/cc3200-launchxl-rd and http://www.ti.com/tool/cc3100boost-rd. TI recommends that the customers copy the exact layout of the engine area to ensure optimum performance as measured on the CC3x00 reference boards.

3.1 Placement of Components

The components placement on the CC3100 BoosterPack is provided in Figure 2. This placement provides optimum performance of the device. Great care has to be taken for the power inductors components to ensure reduced emissions and optimum EVM and mask performance. The power inductors should be placed very close to the device and the power traces should be minimized. The CC3x00 device is sensitive to the layout of the DC-DC converter and it can impact the performance of the device. For the main inductors at the analog, power amplifier, and digital DC-DC output, see Table 3.

Table 3. Inductors

Inductor @	Value	Size	Current Rating	Recommended PN	Description
ANA DCDC OUT	2.2 µH	1008	1.3A	LQM2HPN2R2MG0L	INDUCTOR 2.2UH 20% 1008
PA DCDC OUT	1 µH	1008	1.5A	LQM2HPN1R0MJ0L	INDUCTOR 1UH 20% 1008
DIG DCDC OUT	2.2 µH	1008	1.3A	LQM2HPN2R2MG0L	INDUCTOR 2.2UH 20% 1008

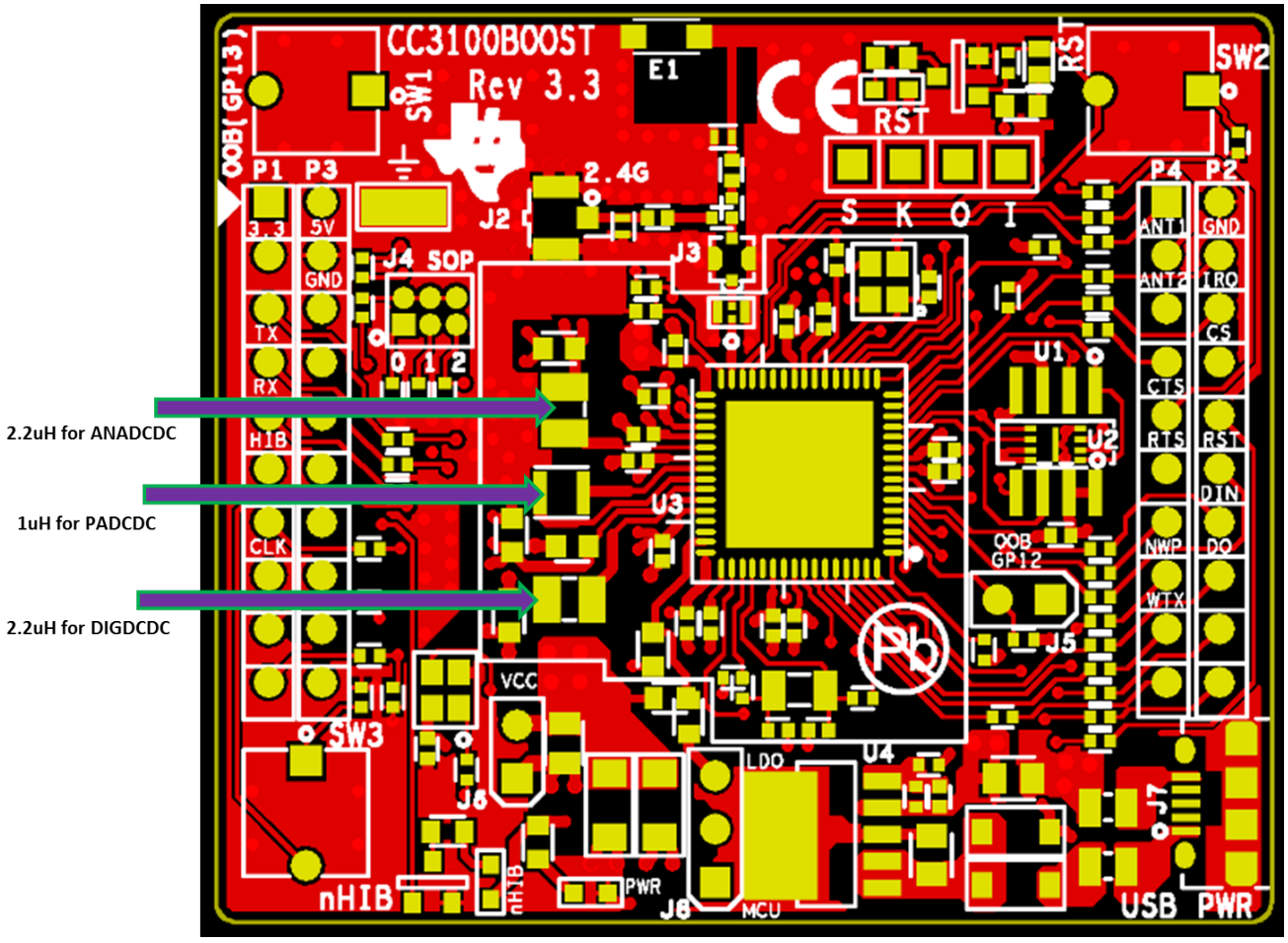


Figure 2. CC3100BOOST 3.3-A Placement Diagram

3.2 Layer Information

3.2.1 Layer-1

Most of the routing is performed on Layer-1 to avoid vias on the board (see Figure 3). The trace widths are maximized for high current pins and minimized for signal pins. For example, the signal pins can be routed with 6 mils (4 mils, if possible) and the power pins with 12 mils and above.

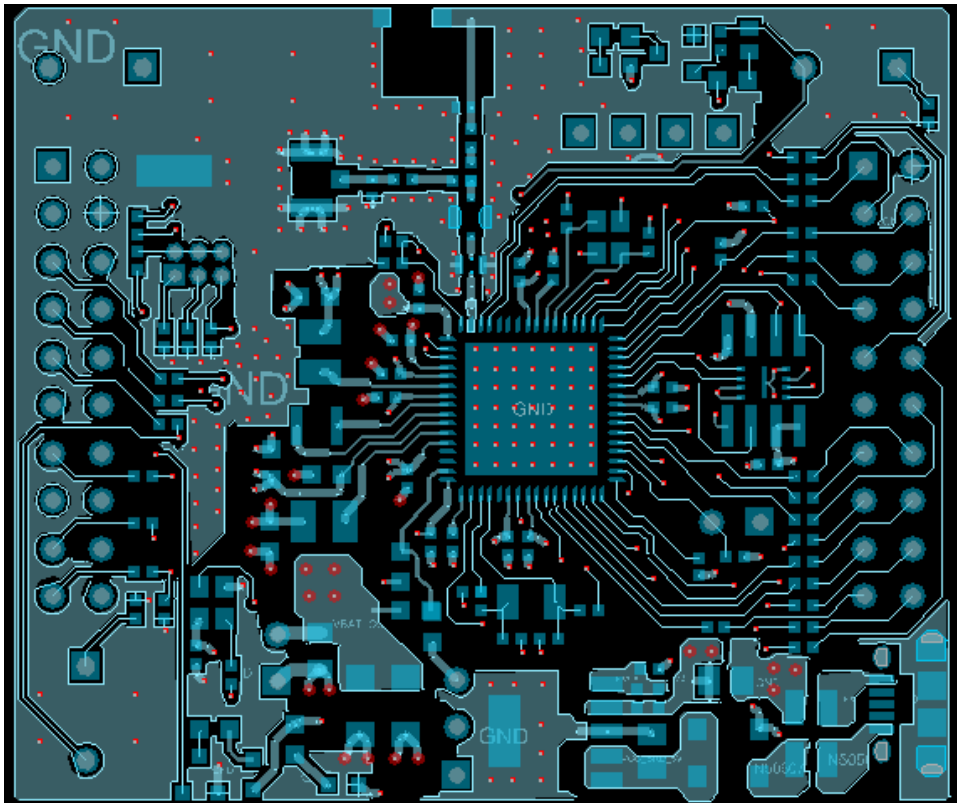


Figure 3. Layer-1

3.2.2 Layer-2

Layer-2 is primary ground plane for the board reference (see Figure 4). It has a void for the antenna section, which is per the antenna guidelines. This return current path for the input de-coupling capacitors (C11, C13 and C18) is routed on L2 using thick traces in order to isolate RF ground from noisy supply ground. This is also required to meet the IEEE spectral mask specifications.

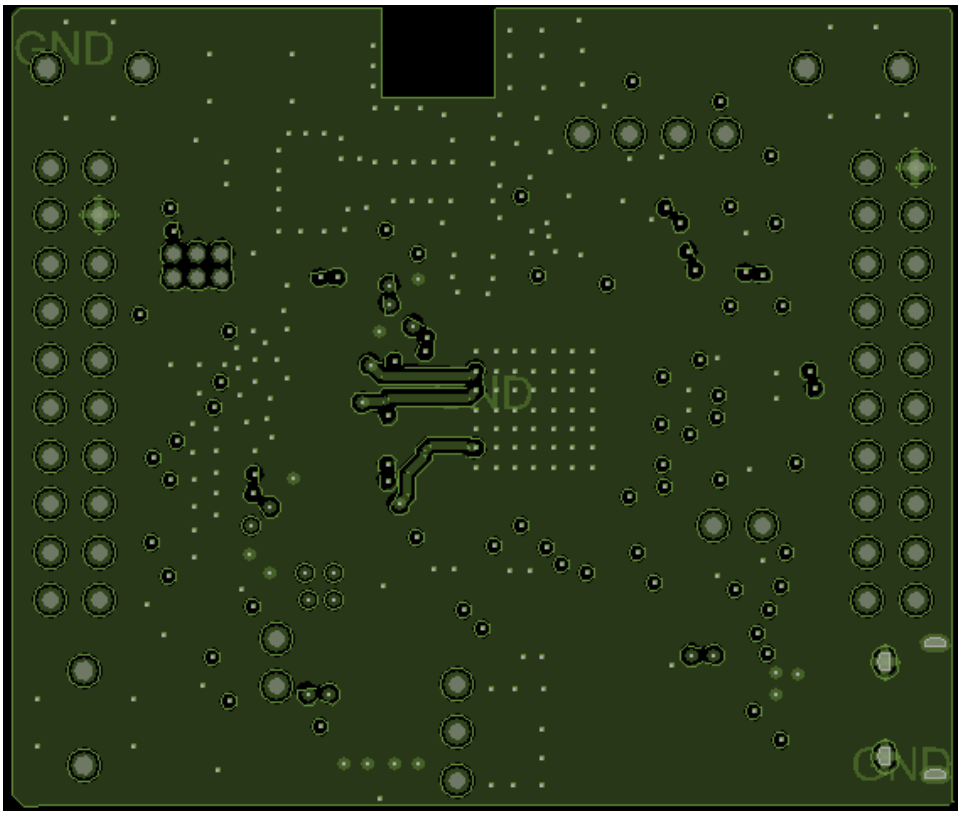


Figure 4. Layer-2

3.2.3 Layer-3

Layer-3 is used to route the power lines to the device (see Figure 5). Power planes are necessary for the power amplifier (PA) and the main supply input to the device. More details are available in subsequent sections.

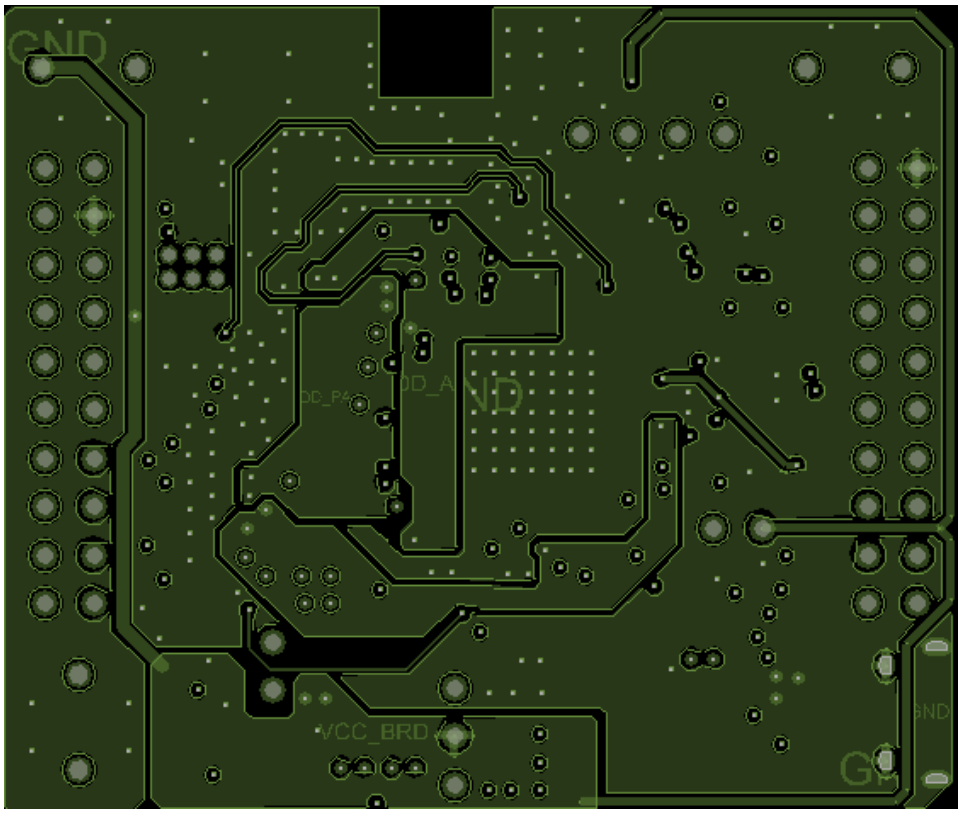


Figure 5. Layer-3

3.2.4 Layer-4

Layer-4 is used for routing the power and the signal lines on the board (see Figure 6). It is also the main power dissipation GND layer for the QFN package. The bottom GND plane has to be maximized for the best thermal performance. The solder mask has been kept open below the QFN device to improve heat dissipation and yield.

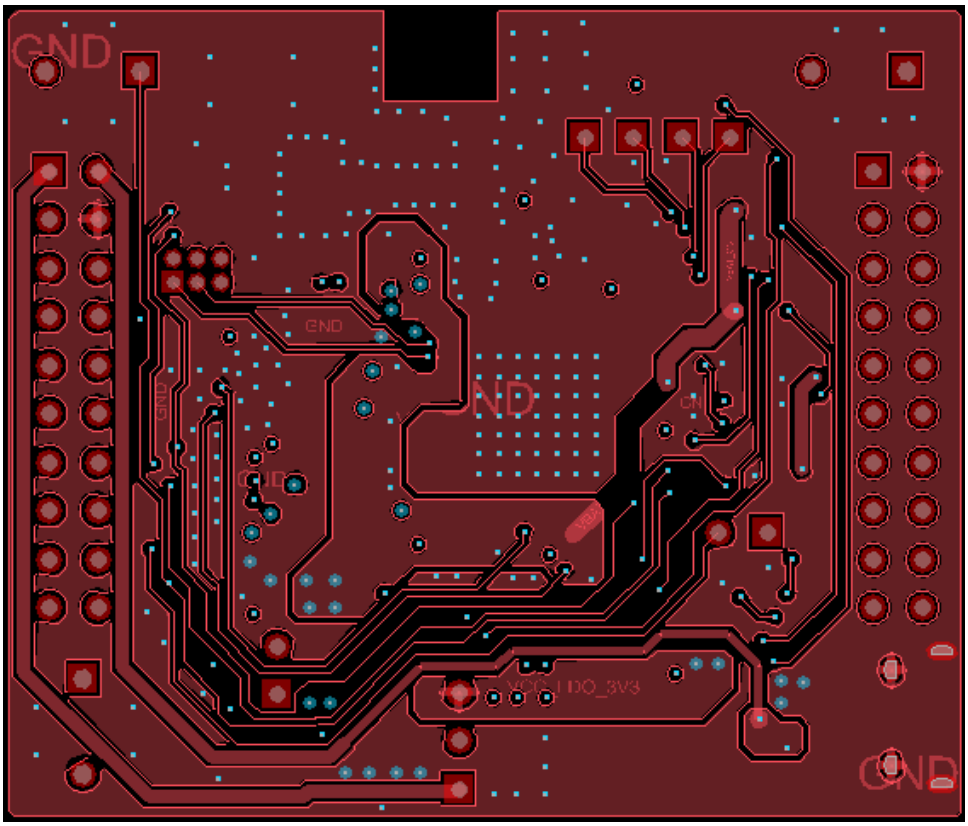


Figure 6. Layer-4

4 Layout Guidelines

4.1 RF Section

Being a wireless device, the RF section gets the top priority in terms of layout (see Figure 7). It is very important for the RF section to be laid out correctly in order to get the optimum performance from the device. A poor layout can cause performance degradation for the output power, the error vector magnitude (EVM), the sensitivity, and the spectral mask.

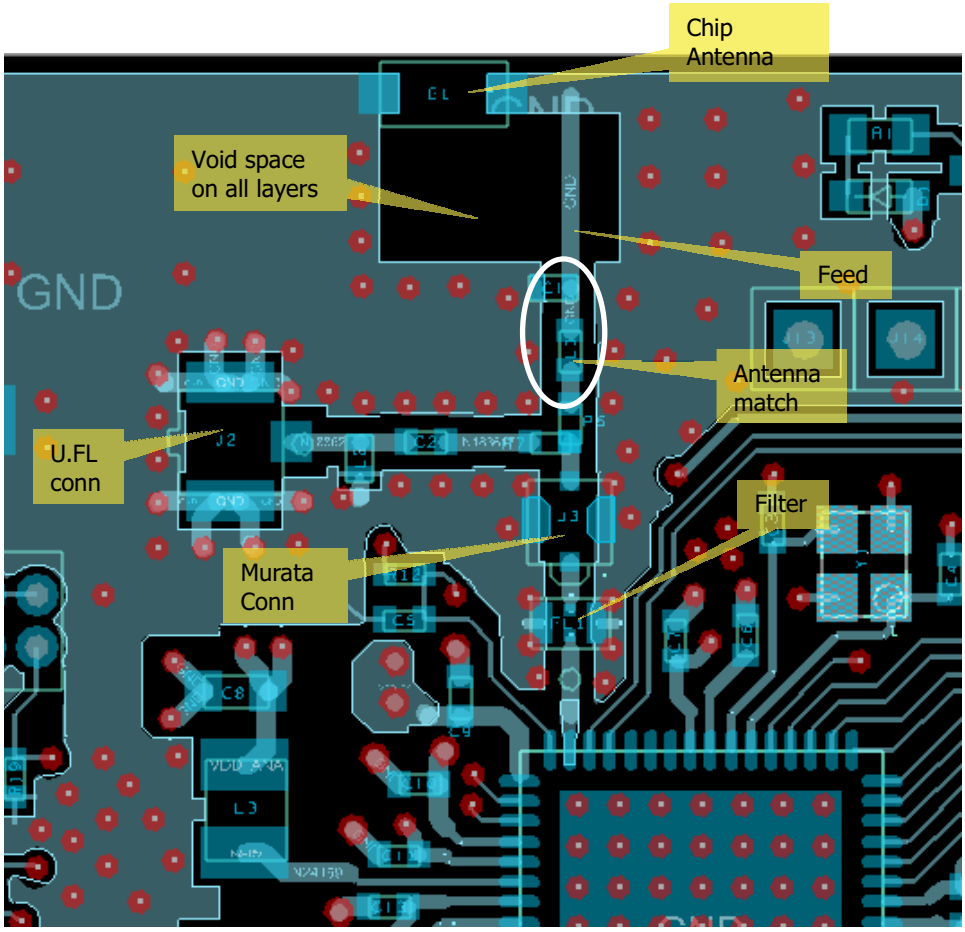


Figure 7. RF Section Layout

4.1.1 Antenna Placement and Routing

The antenna is the element used to convert the guided waves on the PCB traces to the free-space electromagnetic radiation. The placement and layout of the antenna is key to increased range and data rates.

The guidelines in Table 4 need to be observed for the antenna.

Table 4. Antenna Guidelines

Sr No	Guidelines
1	Place the antenna on an edge or corner of the PCB.
2	Make sure that no signals are routed across the antenna elements on all the layers of the PCB.
3	Most antennas, including the chip antenna used on the BoosterPack, require ground clearance on all the layers of the PCB. Ensure that the ground is cleared on inner layers as well.
4	Ensure that there is provision to place matching components for the antenna. These need to be tuned for best return loss once the complete board is assembled. Any plastics or casing should also be mounted while tuning the antenna as this can impact the impedance.
5	Ensure that the antenna impedance is 50 Ω as the device is rated to work only with a 50 Ω system.
6	In case of printed antenna, ensure that the simulation is performed with the solder mask in consideration.
7	Ensure that the antenna has a near omni-directional pattern.
8	The return loss measured at the filter out (looking into the device) should be better than -10dB. To ease the FCC, CE, and ETSI certification, the antenna used should be of the same gain or lesser.

Table 5. Recommended Components

Choice	Part Number	Manufacturer	Notes
1	AH316M245001-T	Taiyo Yuden	Can be placed on the edge of the PCB and uses less PCB space
2	RFANT5220110A2T	Walsim	Needs to be placed on the corner of the PCB

Table 6. Characteristic of Recommended Antenna

Parameter	Spec
Frequency Bandwidth	2.4G to 2.5G
Typical Peak Gain	+1.9dBi
Average Gain at OMNI plane	0dBi
Efficiency (Typical)	-1.3dB (73%)
VSWR	3

4.1.2 Filter Placement and Routing

The RF filter used on the board performs the important function of attenuating the out-of-band emissions from the device. The recommended filter is DEA202450BT-1294C1. The datasheet for the filter can be accessed at http://www.tdk.co.jp/tefe02/rf_bpf_dea202450bt-1294c1-h_en.pdf.

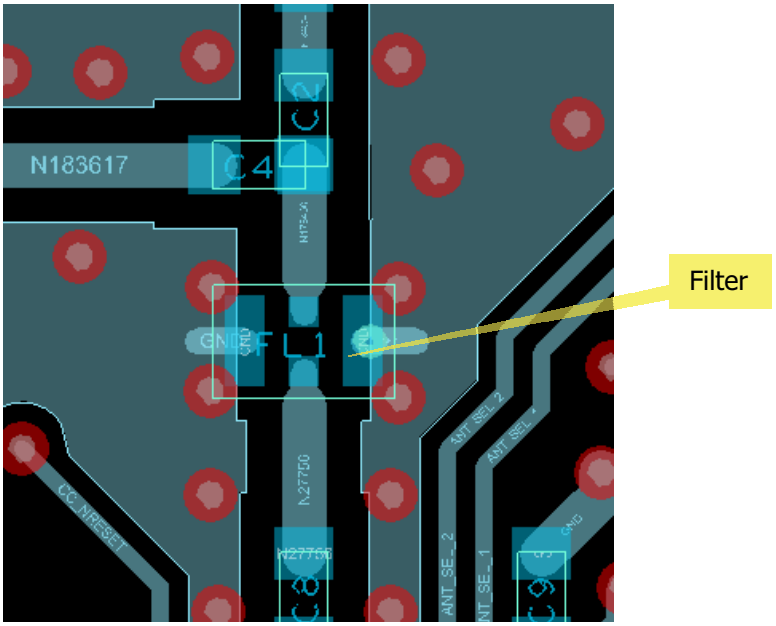


Figure 8. Filter Routing

Table 7. Filter Guidelines

Sr No	Guidelines	Notes
1	Route the RF lines at the input and output of the filter using a coplanar waveguide (CPW) with ground structure. This structure offers the best isolation between input and output due to reduced field fringing.	
2	Use via stitching along the RF trace to reduce emissions and keep the fields confined to the trace boundary.	CPW with GND and via stitching can be accurately simulated using 3D EM tools like EESOF.
3	Use a Zo of 50 Ω only with a tolerance of 10%. Use the stack-up and the trace width provided for reference in the PCB design rules.	
4	Add multiple ground vias for the filter ground pads as close as possible. Minimum of 2 per GND pad is recommended.	
5	To achieve the specifications of the filter attenuation, the minimum isolation between input and output ports of the filter has to be at least 60dB. (Measured without filter)	
6	In case conducted test is required on the PCB, it is recommended to add a U.FL connector or a Murata switch type connector (MM8030 series).	

Table 8. Characteristic of Recommended Filter

Parameter	Frequency (MHz)	Spec
Return loss	2412-2484	10dB (min)
Insertion loss	2412-2484	1.5 dB (Max)
Attenuation	800-830	30 dB (Min)
	1600-1670	20 dB (Min)
	3200-3300	30 dB (Min)
	4000-4150	45 dB (Min)
	4800-5000	20 dB (Min)
	5600- 5800	20 dB (Min)
	6400-6600	20 dB (Min)
	7200-7500	35 dB (Min)
	7500-10000	20 dB (Min)
Reference impedance	2412-2484	50 Ohms
Filter type		Band pass

4.1.3 Transmission Line

The RF signal from the device is routed to the antenna using a coplanar waveguide with ground (CPW-G) structure. This structure offers the maximum isolation across filter gap and the best possible shielding to the RF lines. In addition to the ground on the L1 layer, placing GND vias along the line also provides additional shielding.

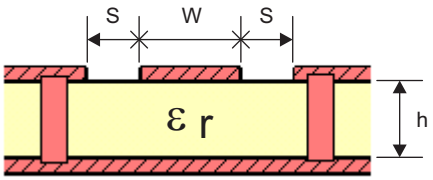


Figure 9. Coplanar Waveguide (cross section) With GND and via Stitching

Figure 10. CPW With GND (top view)

The recommended values for the PCB are provided in Table 9.

Table 9. Recommended Values for the PCB

Parameter	Value	Units
W	18	mils
S	15	mils
H	10	mils
Er (1)	3.9	

(1) Er is assumed to be of an FR-4 substrate.

4.2 Power Section

- All of the input de-coupling capacitors (C11, C13 and C18) should be routed on L2 using thick traces in order to isolate RF ground from noisy supply ground. This is also required to meet the IEEE spectral mask specifications.
- Maintain the thickness of power traces to be higher than 12 mils. Special care should be taken for power amplifier supply lines (pin 33, 40, 41 and 42) and all input supply pins (pin 37, 39 and 44).
- Ensure shortest grounding loop for PLL supply de-coupling capacitor (pin 24)
- Place all de-coupling capacitors as close to the respective pins as possible.
- Power budget: The CC3X00 device can consume up to 450 mA for 3.3 V, 670 mA for 2.1 V and 700 mA for 1.85 V for 24 msec during the calibration cycle. Ensure that the power supply is designed to source this current without any issues. The complete calibration (TX and RX) can take up to 17 mJ of energy from the battery over a time of 24 ms.
- There are many high current input pins on the CC3X00 device. Ensure the trace feeding these pins is capable of handling the below currents.
  - PA DCDC input : pin 39. Max 1A
  - ANA DCDC input : pin 37 : Max 600 mA
  - Dig DCDC input : pin 44: Max 500 mA
  - PA DCDC switching nodes : pin 40/41 , Max 1A
  - PA DCDC output node: pin 42, Max 1A
  - ANA DCDC switching node: pin 38: Max 600 mA
  - Dig DCDC switching node: pin 43 : Max 500 mA
  - PA supply : pin 33: Max 500mA

4.2.1 Inductors for Power Management

The components used in the power management section of the design are critical to achieve the required performance. These should be chosen based on the recommendations in Table 10.

Table 10. Power Management

Inductors	Value	ESR_{min} (mOhm)	Rated Current (A)	Saturation Current I_{sat}	Tolerance
PA DC-DC	1 uH	TBD	1.5	TBD	20%
ANA, DIG DC-DC	2.2 uH	TBD	1.3	TBD	20%

4.3 Clock Section

4.3.1 32K RTC

The 32.768K XTAL should be placed closer to the QFN package. Ensure the load capacitance is tuned based on board parasitic so that the frequency tolerance is within ± 150 ppm.

Table 11. Characteristic of Recommended 32K XTAL

Parameter	Spec
Nominal frequency	32.768KHz
Tolerance with temperature and aging	± 150 ppm

4.3.2 40M XTAL

The 40M XTAL should be placed closer to the QFN package. Ensure the load capacitance is tuned based on board parasitic so that the frequency tolerance is within ± 20 ppm. The frequency tolerance for the XTAL across temperature and with aging should be +/-25ppm. In addition, ensure no high frequency lines are routed closer to the XTAL routing to avoid any phase noise degradation.

Table 12. Characteristic of Recommended 40M XTAL

Parameter	Spec
Nominal frequency	40MHz
Tolerance	± 20 ppm
Load capacitance	8pF
Tolerance with temperature and aging	± 25 ppm

4.4 Digital IO Section

Route serial peripheral interface (SPI) and universal asynchronous receiver/transmitter (UART) lines away from any RF traces since these digital IO lines are high frequency lines and can cause interference to the RF signal.

Keep the length of the high speed lines as short as possible to avoid transmission line effects. Keep the line lower than 1/10th of the rise time of the signal to ignore transmission line effects. This is required only if the traces cannot be kept short. The resistor should be placed at the source end, closer to the device driving the signal.

Add series terminating resistors for each high-speed line (for example, SPI_CLK, SPI_DATA) to match the driver impedance to the line. Typical terminating resistor values range from 27 - 36 Ohms for a 50 Ohm Line impedance.

Route high-speed lines with a ground reference plane continuously below it to offer good impedance throughout, and help shield the trace against EMI interference.

Avoid stubs on high speed lines to minimize the reflections. If the line needs to be routed to multiple locations, use a separate line driver for each line.

If the lines are longer compared to the rise time, add series terminating resistors near the driver for each high speed line (for example, SPI_CLK, SPI_DATA) to match the driver impedance to the line. Typical terminating resistor values range from 27 - 36 Ohms for a 50 Ohm line impedance.

4.5 QFN Ground

1. Ensure 7x7 ground vias are placed on the ground pad for optimal thermal dissipation (see Figure 11). The via drill size can be between 8 mils to 12 mils.

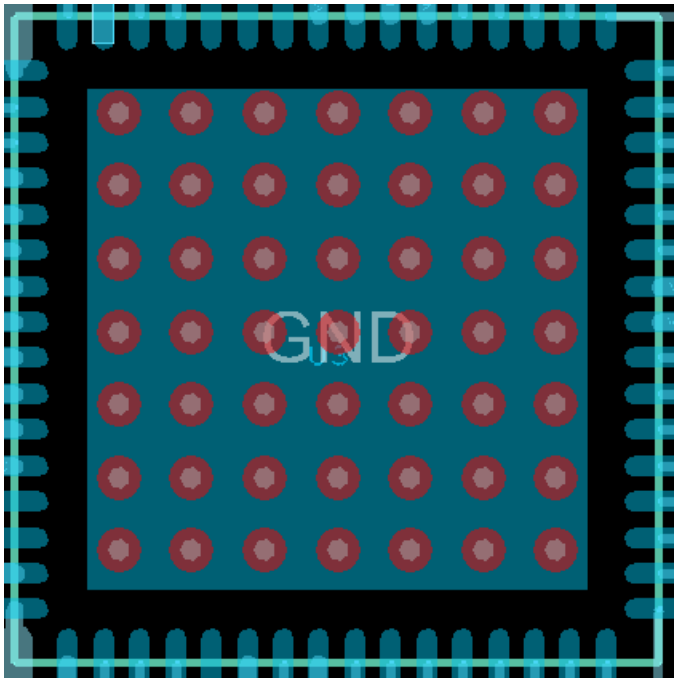


Figure 11. 7x7 Ground Vias on Ground Pad

2. Open the solder mask on L4 for better soldering yield.
3. Split solder paste into smaller blocks (see Figure 12) to avoid component lifting while soldering or re-flow.

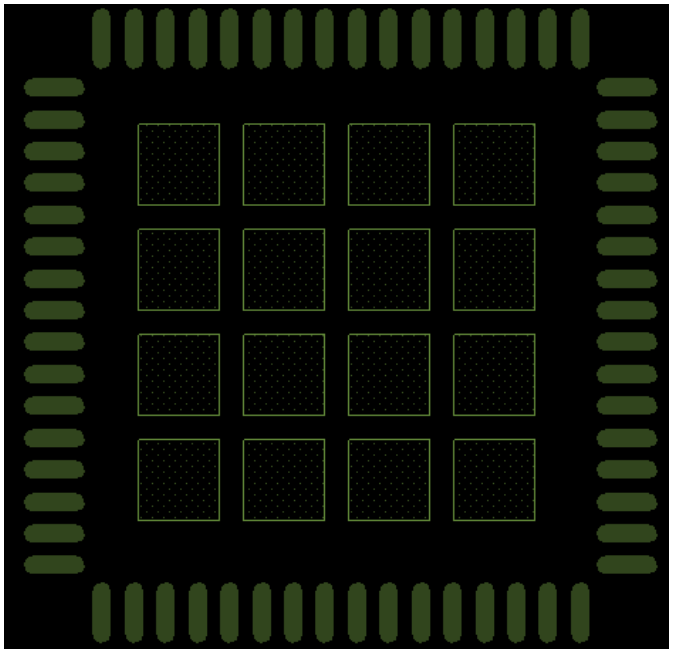
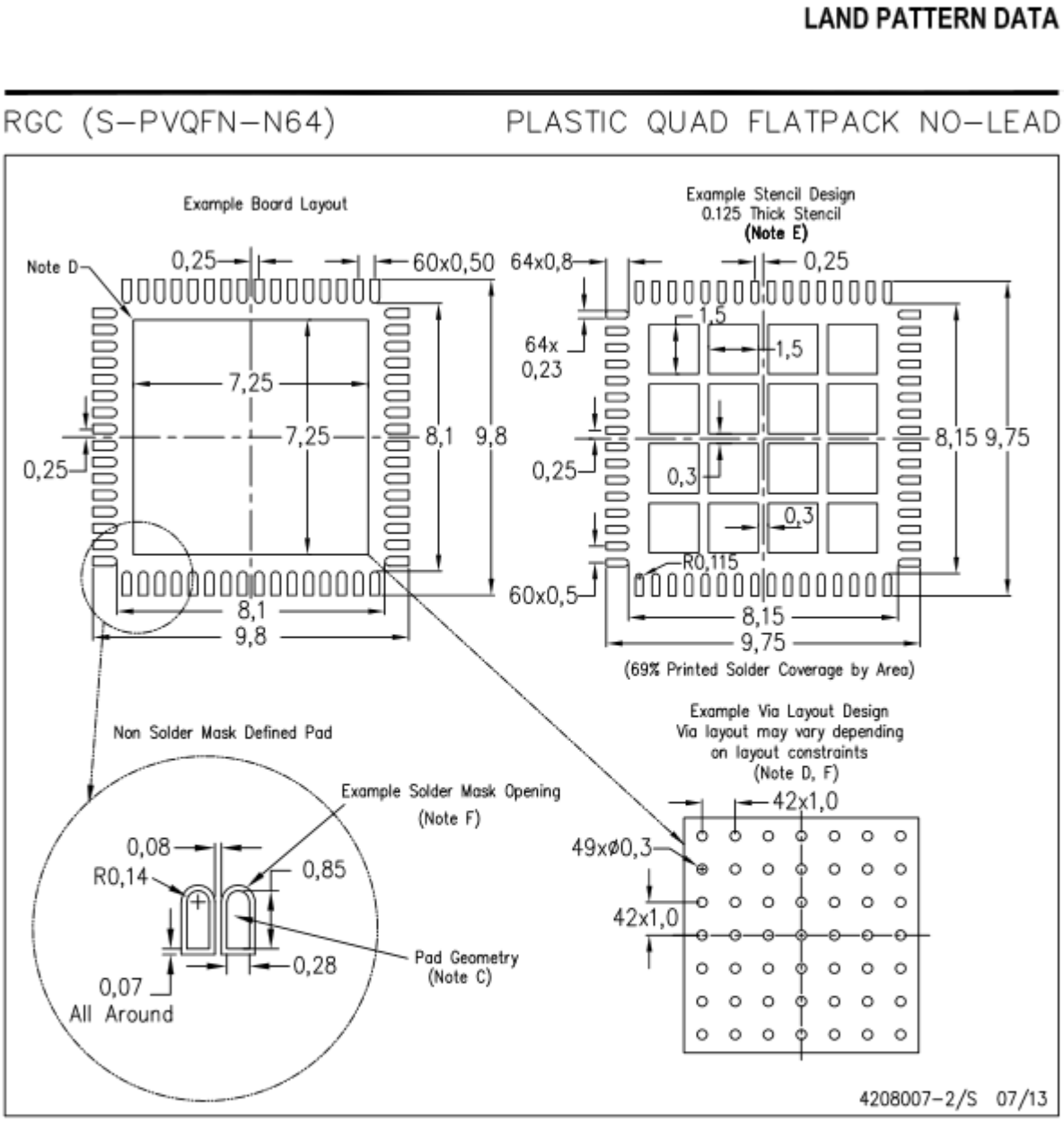


Figure 12. Split Solder Paste Into Smaller Blocks

4. Solder paste should cover at-least 75% of the ground tab of the QFN.

4.6 Recommended Footprint



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271 and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

Figure 13. Recommended Footprint

5 Summary

This document presented an introduction to designing a 4-layer PCB board for the CC3100/CC3200 SimpleLink Wi-Fi easy-to-layout QFN packaged family of devices. In addition to the recommendations presented here, see the CC3100 SimpleLink Wi-Fi and IoT Solution BoosterPack design files located at http://www.ti.com/lit/zip/swrc288 and the CC3200 SimpleLink Wi-Fi and IoT Solution With MCU LaunchPad board design files located at http://www.ti.com/lit/zip/swrc289.

6 Additional References

1. CC31xx and CC32xx main landing page: http://www.ti.com/product/simplelinkwifi
2. The datasheet of CC3100 SimpleLink™ Wi-Fi® and IoT Solution for MCU Applications (SWAS031)
3. The datasheet of CC3200 SimpleLink™ Wi-F®i and IoT Solution, a Single Chip Wireless MCU (SWAS032)

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