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There are three main aspects of performance in FPGA design that we will cover power, speed, and area.

The number one method for us to optimize our design on our end would be to ensure that our algorithm is optimized as possible, since the synthesizer already does its own optimization that is beyond our control such as routing, clock gating and so forth.

Power:

Using vectorless power estimation, the total thermal power estimate for the design is 135.29mW. Vectorless power estimation is using probability to determine switching rates on every gate.

Speed:

It takes around fifty-five thousand nanoseconds to transmit a message, and receive a message. The design is full duplex, so these occur at the same time.

$$\frac{55000ns}{20ns} = 2750\ cycles.$$

This is the number of internal clock cycles it takes for the UART module to what is state above, divide this by the 50MHz clock to get the fraction of a second it takes, and we obtain 0.000055 seconds.

Area:

The UART module takes less than one percent of the logic element that the FPGA provides, so it is lightweight as it should be. There are no multiplier elements being used, 91 Registers, and 228 Logic Elements.