

## Unit 3:

### Digital Electronics:

It is a branch of electronics that operate on digital signals (0, 1). A digital circuit is an electronic circuit which makes logical decisions based on the combinational digital input signal. These digital circuit is also called as digital logic gate. It is a basic building block for digital electronic circuit & processor or based system.

The basic logic gates AND, OR, NOT.

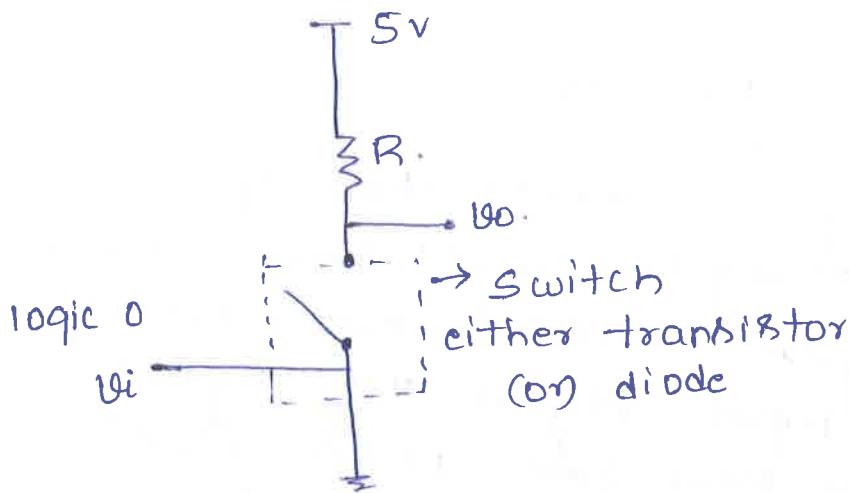
### Switching Circuit:

The digital logic circuit ~~gates~~ (<sup>(or)</sup>) operates at two logic levels i.e. at logic 0 (0V) & logic 1 (say 5V). These logic gates are available in two basic families TTL stands for (Transistor- Transistor logic) & CMOS stands for (Complementary Metal- Oxide-Silicon).

In TTL logic BJT combination (NPN or PNP) is used in manufacturing of logic gates. In CMOS technology MOSFET & JFET is used in the manufacturing of logic gates.

The basic principle of logic gate is it acts as a switch. A switching circuit is a basic composition of gates. Operates on binary values (0 & 1). The 0 level indicated as open - switch & level 1 indicated as closed - switch.

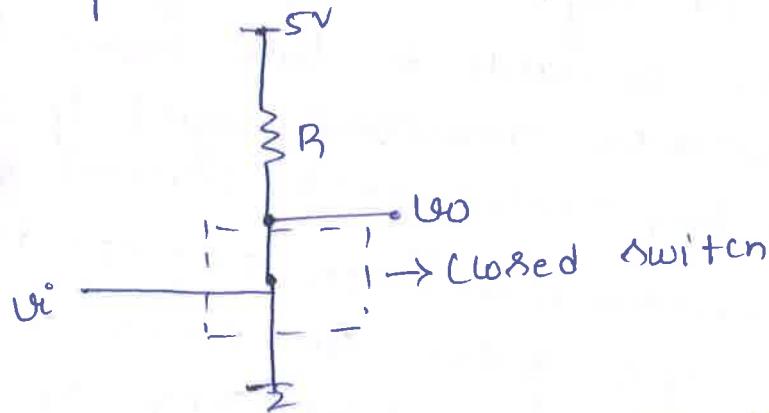
Let consider a simple switching circuit



Truth table

Input	switch status	Output
0	OPEN	1
-	-	-

In an electronic circuit switch is either transistor or diode. When input voltage is less than the threshold voltage (or) cut-in voltage, then the device will remain OFF state then it acts as a open switch. Thus the output of the circuit is high (say 5V).



Truth Table:

Input	switch status	Output
1	CLOSED	0
-	-	-

When the input voltage is greater than three hold voltage device get turn ON acts as a closed switch. Then the applied voltage is get grounded through the device. the output is approximately equal to 0.

### Basic logic gates:

Logic gates are the basic building block of any digital circuit, which has the ability to produce output level with the combination of input levels.

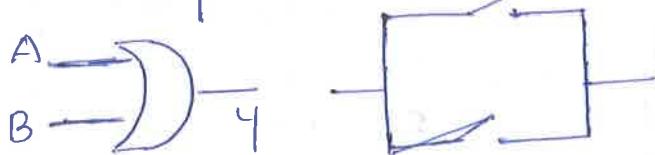
When  $V_1 = 0V < V_T$  &  $V_2 = 5V > V_T$ , then diode  $D_1$  is in OFF state &  $D_2$  is reverse biased. Then all current is get grounded through  $D_1$ , i.e. output is OV. Similarly when  $V_1 = 5V > V_T$  &  $V_2 = 0V < V_T$ , the  $D_1$  is reverse biased &  $D_2$  is in OFF state. The current is grounded through  $D_2$  which gives OV at the output.

But when both  $V_1 = V_2 = 5V$  then  $D_1$  &  $D_2$  is

get reverse biased acts as open switch which offers very resistance for the flow of base current through it. Then the all the voltage appears at output through resistance  $R$  & gives high value.

### OR Gates

It operations logical addition between two input variables. The output of this gate is high (say 5V) when any one of the input goes high. The symbolic representation & logic equation of this gate is given by:



$$Y = A + B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Symbolic Representation

Switching Action

Logic Equation

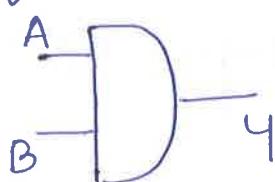
Truth Table

The discrete arrangement of OR gate is implemented by using diodes which is as shown below. The diodes  $D_1$  &  $D_2$  are connected to variable supply ( $V_1$  &  $V_2$ ).

There are seven basic types of logic gates:  
 AND ( $A \cdot B$ ), OR ( $A + B$ ), NOT ( $\bar{A}$ ), NAND ( $\bar{A} \cdot \bar{B}$ ), NOR ( $\bar{A} + \bar{B}$ ),  
 XOR ( $A \oplus B$ ), XNOR ( $\bar{A} \oplus \bar{B}$ ).

### AND gate:

It performs logical multiplication with two or more input variables. The output of this gate is high only when all the inputs applied is high. The symbolic representation & logical denotation of AND gate is given by:



$$Y = A \cdot B$$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

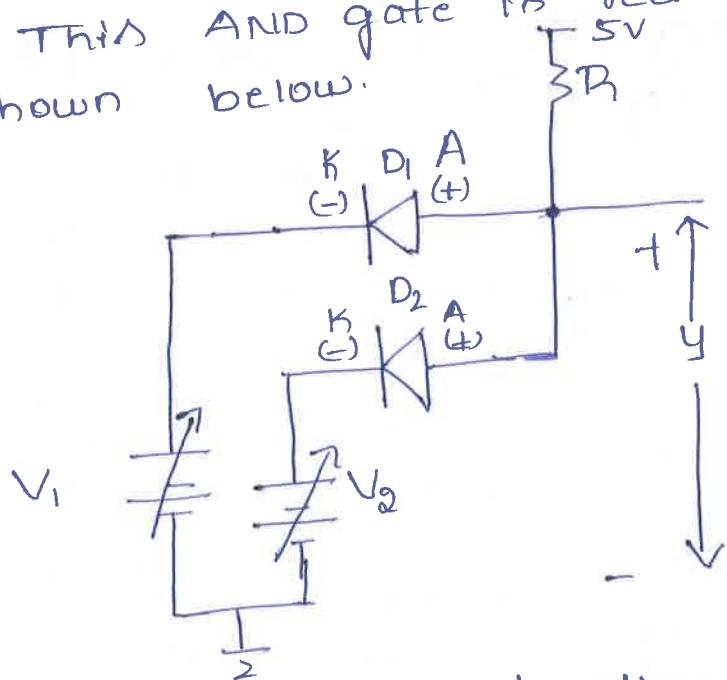
Symbollic Representation

logical equation

switching action

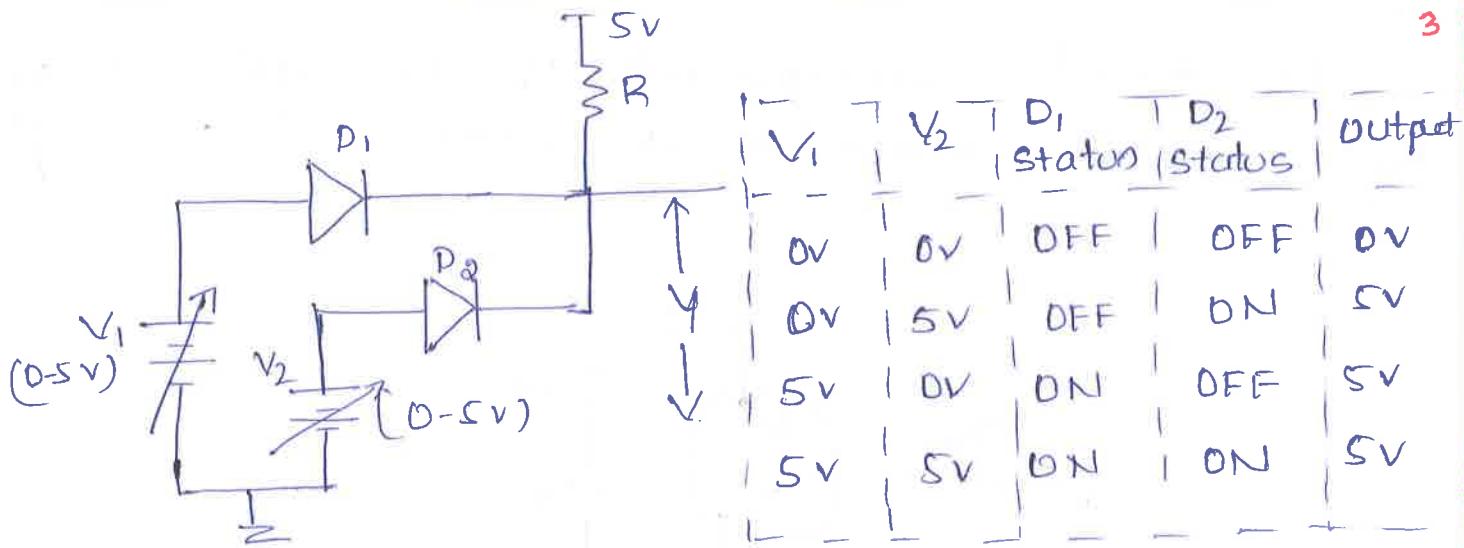
Truth table

This AND gate is realised by using diode as shown below.



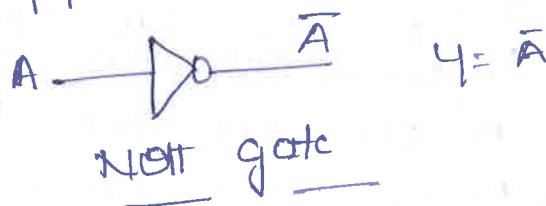
V <sub>1</sub>	V <sub>2</sub>	D <sub>1</sub> Status	D <sub>2</sub> Status	Output
0V	0V	OFF	OFF	0V
0V	5V	OFF	OFF	0V
5V	0V	OFF	OFF	0V
5V	5V	OFF	OFF	5V

In this arrangement the diodes D<sub>1</sub> & D<sub>2</sub> are connected to variable power supply (say 0-5V). When  $V_1 = 0V < V_T$  &  $V_2 = 0V < V_T$  both diodes are in cut-off region. So the output is 0V.



When both V<sub>1</sub>=V<sub>2</sub>=0V the diodes D<sub>1</sub> & D<sub>2</sub> are in OFF state because applied voltage is less than V<sub>F</sub>. Then output voltage is 0V. But when V<sub>1</sub>=5V diode D<sub>1</sub> acts as open switch for diode D<sub>2</sub> is forward biased acts as closed switch. Similarly V<sub>1</sub>=5V diode D<sub>1</sub> is forward biased & for V<sub>2</sub>=0V diode is in OFF state. It gives 5V output. For V<sub>1</sub>=V<sub>2</sub>=5V both D<sub>1</sub> & D<sub>2</sub> is forward biased & gives high output value.

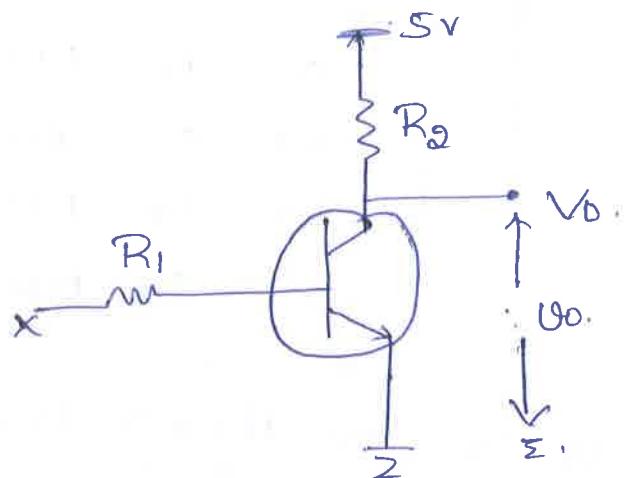
NOT gate:  
It performs logical inversion of the applied input voltage i.e. for 0 → 1 & 1 → 0. It also defines the output of this gate as inversion of input applied.



Truth table

A	Y
0	1
1	0

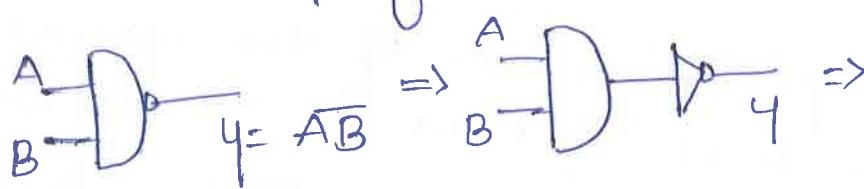
The discrete arrangement of NOT gate is realised by transistor, which is as shown in the figure.



When the input  $x = 0V$ , the transistor wont turn ON & it will remains in OFF state. As a result no current flows the resistor & there will no voltage drop across resistor. This results in high output value. Similarly when  $x = 5V$ , transistor get turns ON & the output voltage corresponds to 0V.

### NAND Gates

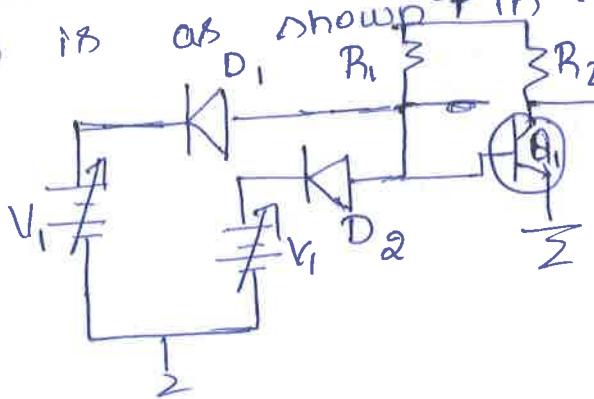
It performs inversion of the AND gate output.



A	B	Y
0	0	1
0	1	0
1	0	0

The combination AND

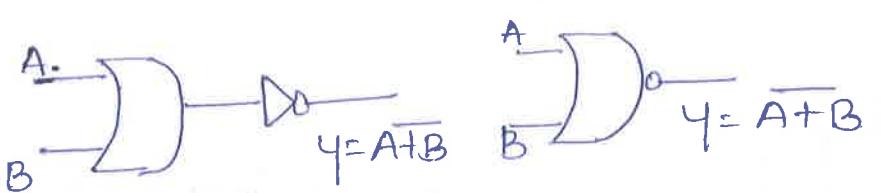
The discrete of NAND is followed by transistor NOT gate which is as shown in the figure.



D <sub>1</sub>	D <sub>2</sub>	T <sub>1</sub>	T <sub>2</sub>	V <sub>O</sub>	status
0V	0V	OFF	OFF	OFF	OFF
0V	5V	OFF	ON	5V	ON
5V	0V	ON	OFF	5V	ON
5V	5V	ON	ON	OFF	OFF

## NOR gate:

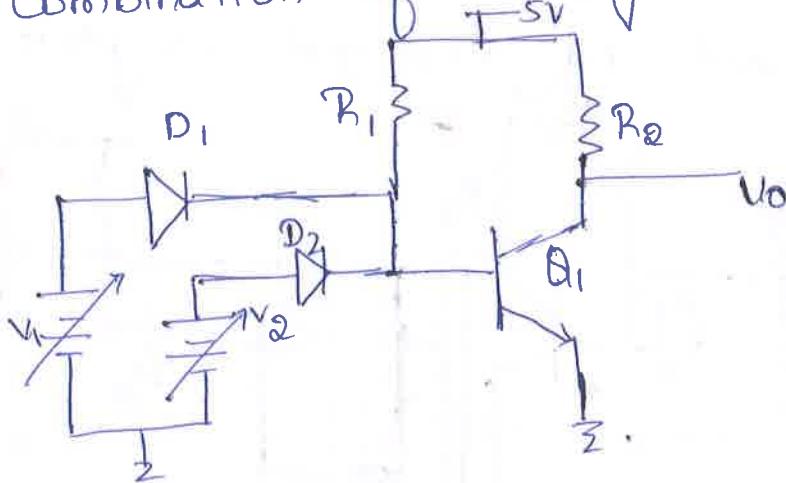
It is inverse of OR gate output.



A	B	Output (Y)
0	0	1
0	1	0
1	0	0
1	1	0

The discrete arrangement of NOR gate followed by NOT gate.

Combination of NOR gate



V <sub>A</sub>	V <sub>B</sub>	D <sub>1</sub> Status	D <sub>2</sub> Status	T <sub>O/P</sub> Status
0v	0v	OFF	OFF	OFF / 5v
0v	5v	OFF	ON	ON / 0v
5v	0v	ON	OFF	ON / 0v
5v	5v	ON	ON	ON / 0v

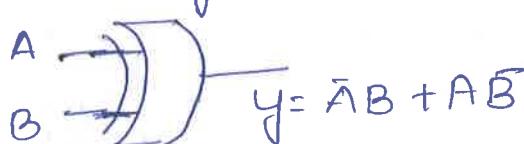
## XOR gates-

It is an exclusive OR gate circuit, which is a combination of all three basic gate (AND, OR, NOT) because it's logical expression is

$$Y = \overline{A} \cdot B + A \cdot \overline{B}$$

NOT      AND      OR.

So the logical representation of XOR gate & its truth table is given by

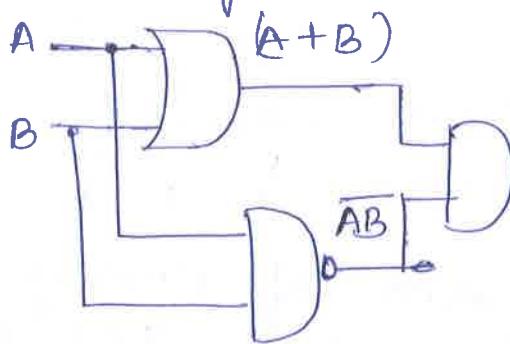


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Symbol representation

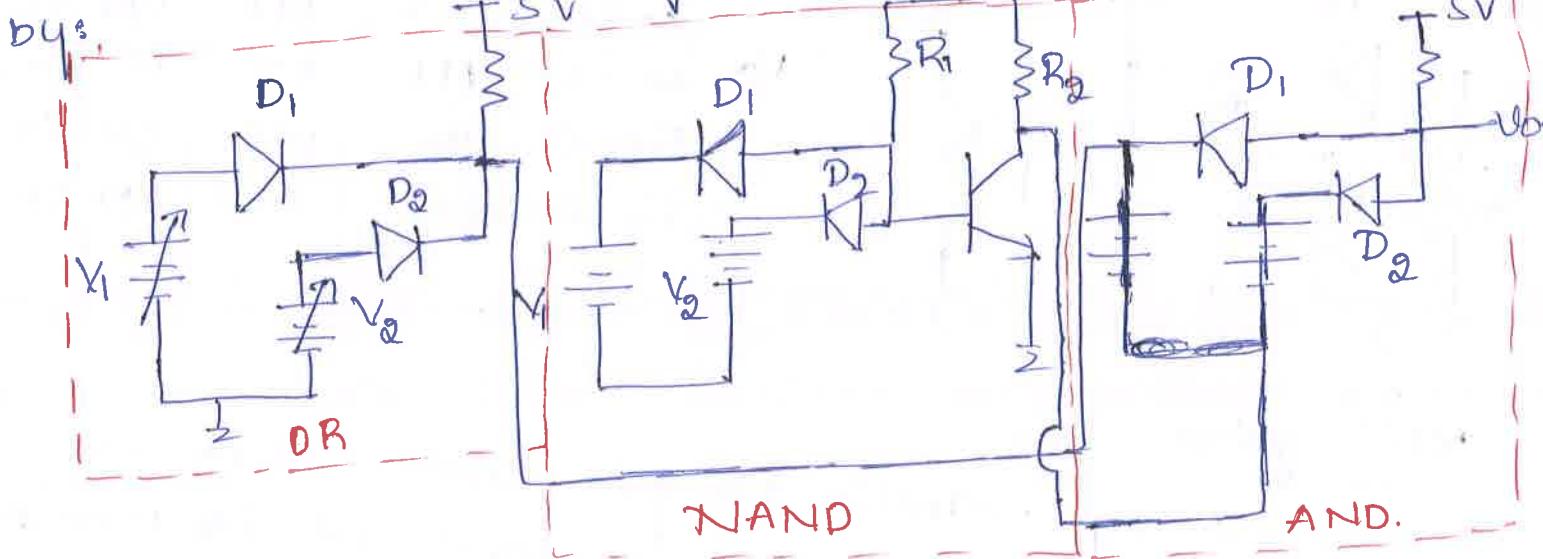
The output is high when any of the input is high

Q for other two combination of input (0 0 & 11) the output of this gate is '0'. The discrete equivalent logic circuit is given by:



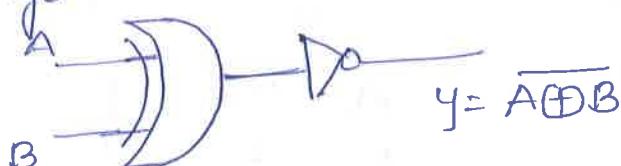
$$\begin{aligned} y &= (\bar{A}+B) \cdot (\bar{A}\bar{B}) = (\bar{A}+B) \cdot (\bar{A}+\bar{B}) \\ y &= A\bar{A} + A\bar{B} + \bar{A}B + B\bar{B} \\ &= A\bar{B} + \bar{A}B \end{aligned}$$

The discrete arrangement of XOR gate is given

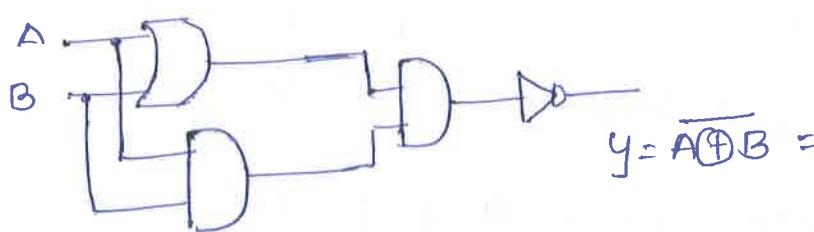


ExNOR:

It gives inverse value to the output of XOR gate.



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1



$$\begin{aligned} y &= \overline{\bar{A}\bar{B} + A\bar{B}} \\ &= (\bar{A} + \bar{B}) \cdot (\bar{A} + \bar{B}) \\ &= (A+B) \cdot (\bar{A} + B) \\ &= AB + \bar{A}\bar{B} \end{aligned}$$

## Number Systems:-

In digital electronics, the number system is used representing the information. The number system has different bases like decimal ( $x_{10}$ ), binary ( $x_2$ ), Octal ( $x_8$ ) & hexadecimal ( $x_{16}$ ).

### Decimal Number System:

The number system which is having a digit from 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, this number system is known as decimal number system. The base value of it is '10' i.e. ( $x_{10}$ ).

### Octal Number System:

The number system which is having a digit from 0, 1, 2, 3, 4, 5, 6, 7, this number system is known as octal number system. The base value of it is '8' i.e. ( $x_8$ ).

### Hexadecimal Number System:

The number system which is having a digit from 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F, this number system is known as hexadecimal number system. The base value of it is '16' i.e. ( $x_{16}$ ).

### Binary Number System:

The number system uses only two digits 0 & 1 known as binary number system. The binary equivalent for octal & hexadecimal number is derived as follows:  
 Octal :  $8 \rightarrow 2^3 = 8$  3 digit bits used to represent it binary  
 Hexadecimal :  $16 \rightarrow 2^4 = 4$  bits used to represent it binary.

Octal	$2^2$	$2^1$	$2^0$	Binary Value
0	0	0	0	0 0 0
1	-	-	$2^0$	0 0 1
2	-	$2^1$	-	0 1 0
3	-	$2^1$	$2^0$	0 1 1
4	$2^2$	-	-	1 0 0
5	$2^2$	$2^1$	$2^0$	1 0 1
6	$2^2$	$2^1$	-	1 1 0
7	$2^2$	$2^1$	$2^0$	1 1 1

Hexadecimal	$2^3$	$2^2$	$2^1$	$2^0$	Binary Value
0	0	-	-	-	0 0 0 0
1	-	-	-	$2^0$	0 0 0 1
2	-	-	$2^1$	-	0 0 1 0
3	-	-	$2^1$	$2^0$	0 0 1 1
4	-	$2^2$	-	-	0 1 0 0
5	-	$2^2$	$2^1$	$2^0$	0 1 0 1
6	-	$2^2$	$2^1$	-	0 1 1 0
7	-	$2^2$	$2^1$	$2^0$	0 1 1 1
8	$2^3$	-	-	-	1 0 0 0
9	$2^3$	-	$2^1$	$2^0$	1 0 0 1
A (10)	$2^3$	$2^2$	-	-	1 0 1 0
B (11)	$2^3$	$2^2$	$2^1$	$2^0$	1 0 1 1
C (12)	$2^3$	$2^2$	-	-	1 1 0 0
D (13)	$2^3$	$2^2$	-	$2^0$	1 1 0 1
E (14)	$2^3$	$2^2$	$2^1$	-	1 1 1 0
F (15)	$2^3$	$2^2$	$2^1$	$2^0$	1 1 1 1

## Number System Conversion:

(i) Decimal to binary:

a)  $(49)_{10} = \underline{\underline{1 \ 1 \ 0 \ 0 \ 0 \ 1}}_2$

$$\begin{array}{r}
 2 | 49 \\
 2 | 24 - 1 \\
 2 | 12 - 0 \\
 2 | 6 - 0 \\
 2 | 3 - 0 \\
 \text{---} \\
 0 | 1 - 1
 \end{array}$$

b)  $(891)_{10} = \underline{\underline{1 \ 1 \ 0 \ 1 \ 1 \ 1 \ 0 \ 1 \ 1}}_2$

$$\begin{array}{r}
 2 | 891 \\
 2 | 445 - 1 \\
 2 | 222 - 1 \\
 2 | 111 - 0 \\
 2 | 55 - 1 \\
 2 | 27 - 1 \\
 2 | 13 - 1 \\
 2 | 6 - 1 \\
 \text{---} \\
 2 | 3 - 1
 \end{array}$$

(iii) Decimal to Octal:

a)  $(77)_{10} = \begin{array}{r} 8 | 77 \\ 8 | 9-0 \end{array} - (905)_8$

b)  $(672)_{10} = \begin{array}{r} 8 | 672 \\ 8 | 84-0 \\ 8 | 10-4 \end{array} - (1040)_8$

c)  $(54.734)_{10} = \begin{array}{r} 8 | 54 \\ 8 | 48-6 \\ 8 | 6-0 \end{array} - (606)_8$

$\therefore (54.734)_{10} = (606.565)_8$

$$\begin{aligned} 0.734 \times 8 &= 0.872 \quad \text{carry } 5 \\ 0.872 \times 8 &= 0.976 \quad \text{carry } 6 \\ 0.976 \times 8 &= 0.856 \quad \text{carry } 5 \end{aligned}$$

(iv) Binary to decimal:

a)  $(10111)_2 = 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = 16 + 4 + 2 + 1 = (23)_{10}$

b)  $(01011.10111)_2 = 0 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4} + 1 \times 2^{-5}$

$$= 8 + 2 + 1 + 0.5 + 0.125 + 0.0625 + 0.03125$$

$$= (10.71875)_{10}$$

c)  $(1.01101)_2 = 1 \times 2^0 + 0 \times 2^1 + 1 \times 2^2 + 1 \times 2^3 + 0 \times 2^4 + 1 \times 2^5$

$$= 1 + 0.25 + 0.125 + 0.03125$$
$$= (1.40625)_{10}$$

3 bits from LSB to MSB  
 $2^3 = 8$  no group

(v) Binary to Octal:-

a)  $(01011101)_2 = 000 \begin{array}{r} 1 \\ | \\ 0 \\ | \\ 5 \end{array} \begin{array}{r} 1 \\ | \\ 0 \\ | \\ 5 \end{array} = (055)_8$

c)  $(72 - 42)_{10} =$

$$\begin{array}{r} 2 | 72 \\ 2 | 36 - 0 \\ 2 | 18 - 0 \\ 2 | 9 - 0 \\ 2 | 4 - 1 \\ 2 | 2 - 0 \\ \hline & 0 \end{array}$$

$$(72)_{10} = \underline{\underline{(1001000)}_2}$$

$$(-42)_{10} = 0.42 \times 2 = 0.84 \rightarrow \text{Carry } 0$$

$$0.84 \times 2 = 0.68 \rightarrow \text{Carry } 1$$

$$0.68 \times 2 = 0.36 \rightarrow \text{Carry } 1$$

$$\therefore (-42)_{10} = \underline{\underline{(1001000.011)}_2}$$

d)  $(0.843)_{10} =$

$$0.843 \times 2 = 0.686 \rightarrow \text{Carry } 1$$

$$0.686 \times 2 = 0.372 \rightarrow \text{Carry } 1$$

$$0.372 \times 2 = 0.744 \rightarrow \text{Carry } 0$$

$$(-843)_{10} = \underline{\underline{(-110)_2}}$$

(ii) Decimal  $\rightarrow$  Hexadecimal:-

$$\text{Quotient} \times \text{Divisor} = \text{Dividend} - \text{Remainder}$$

a)  $(99)_{10} = 16 \left| \begin{array}{r} 99 \\ 6-3 \uparrow \end{array} \right. - (63)_{16}$

b)  $(943)_{10} = 16 \left| \begin{array}{r} 943 \\ 58-15(F) \\ 3-10(A) \uparrow \end{array} \right. - (3AF)_{16}$

c)  $(85 \cdot 32)_{10} = 16 \left| \begin{array}{r} 85 \\ 80-5 \\ 5-0 \uparrow \end{array} \right. (505)_{16}$

$0.32 \times 16 = 0.12$   
 $0.12 \times 16 = 0.92$   
 $0.92 \times 16 = 0.72$

Carry 5  
 Carry 1  
 Carry 14(E)

$$\therefore (85 \cdot 32)_{10} = \underline{\underline{(505.51E)}_{16}}$$

$$\Leftrightarrow (101101101101101)_2$$

$$001|011|011\cdot1101111|0102$$

1 3 3 . 6 #

(133- 6#2) 8

$$\Leftrightarrow (1 \cdot 1101100)_2 = \begin{array}{r} 001 \\ | \\ 001 \end{array} \cdot \begin{array}{r} \overline{110} \\ | \\ 6 \end{array} + \begin{array}{r} 10 \\ | \\ 6 \end{array} \cdot 0 = (1 \cdot \underline{\underline{660}})_8$$

(vi) Binary to Hexadecimal:  $2^4 = 16 \rightarrow$  Group 4 digits from LSB to MSB

$$a) (1101101\overset{1}{\overleftarrow{101}})_2 \text{ is } \begin{matrix} 1 & 0 & 1 & 1 & 0 & 1 \\ (3) & 6 & & & & D \end{matrix}_{16}$$

$$b) (0110\overset{\leftarrow}{1}10\cdot 01\overset{\rightarrow}{1}010) =$$

$$00011 \Big| 0110.0110 \Big| 1000 \\ (3) \qquad \qquad \qquad 6 \cdot \qquad \qquad 6 \qquad \qquad 8)_{16}$$

$$\Leftrightarrow (11 \cdot 110100)_2 = \underbrace{001}_{(3)} \cdot \underbrace{\overline{1101}}_{D} \mid \begin{matrix} 0000 \\ 0 \end{matrix} _{16}$$

(vii) Octal to decimal

$$0) (-43)_8 = -1 \times 8^2 + 4 \times 8^1 + 3 \times 8^0 = -1 + 4 + 3 = 6$$

$$0) (743)_8 = 7 \times 8^2 + 4 \times 8^1 + 3 \times 8^0$$

$$b) (851 \cdot 340)_8 = 8^4 + 5 \cdot 8^3 + 1 \cdot 8^2 + 3 \cdot 8^1 + 4 \cdot 8^0$$

$$= (553 \cdot 4375)_{10}$$

(VIII) Octal to binary:

a)  $(35)_8 = (011101)_2$

b)  $(756)_8 = (111101110)_2$

c)  $(434)_8 = (111\cdot100011100)_2$

(IX) Octal to hexadecimal:

a)  $(41)_8 = \begin{array}{r} 001 \\ 2 | 0 \\ 0 \end{array} = (21)_{16}$

b)  $(356)_8 = \begin{array}{r} 000 \\ 0 | 1110 \\ 0 E E \end{array} = (0EE)_{16}$

c)  $(6.542)_8 = \begin{array}{r} 0110 \\ 6 . B \\ 1 \end{array} \cdot \begin{array}{r} 101100010000 \\ 1 \end{array} = (6.B10)_{16}$

(X) Hexadecimal to decimal:

a)  $(A13)_{16} = A \times 16^2 + 1 \times 16^1 + 3 \times 16^0 = (2579)_{10}$

b)  $(84.45)_{16} = 8 \times 16^1 + 4 \times 16^0 + 4 \times 16^{-1} + 5 \times 16^{-2} = (132.2695)_{10}$

b)  $(84.45)_{16} = 8 \times 16^1 + 4 \times 16^0 + 4 \times 16^{-1} + 5 \times 16^{-2} + 1 \times 16^{-3} + 1 \times 16^{-4}$

c)  $(F.BCD)_{16} = F \times 16^0 + B \times 16^{-1} + C \times 16^{-2} + D \times 16^{-3} + 1 \times 16^{-4}$   
 $= (15.7375)_{10}$

(XI) Hexadecimal to binary:

a)  $(C03)_{16} = (110011000011)_2$

b)  $(45.1AB)_{16} = (000000101.000110101011)_2$

c)  $(8.CDE)_{16} = (1000.110011001110)_2$

(xii) Hexadecimal to Octal:

a)  $(8ACF)_{16} = 001 \begin{array}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|} \hline & 0 & 0 & 0 & | & 0 & 1 & 0 & | & 0 & 0 & | & 1 & 1 & \\ \hline \end{array} \begin{array}{l} 1 \\ 0 \\ 5 \\ 6 \\ 7 \end{array} \begin{array}{l} 8 \end{array}$

b)  $(F \cdot 2A)_{16} = 001 \begin{array}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|} \hline & 1 & 1 & . & 0 & 0 & | & 0 & 1 & 0 & | & 0 & 0 \\ \hline \end{array} \begin{array}{l} 1 \\ 1 \\ - \\ 2 \\ 4 \end{array} \begin{array}{l} 8 \end{array}$

c)  $(33 \cdot 4A1)_{16} = 000 \begin{array}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|} \hline & 1 & 1 & 0 & | & 0 & 1 & 0 & | & 0 & 1 & 0 & | & 0 & 0 & 1 & 0 \\ \hline \end{array} \begin{array}{l} 0 \\ 6 \\ 3 \\ 2 \\ 2 \\ 4 \\ 2 \end{array} \begin{array}{l} 8 \end{array}$

Binary addition:

a)  $\begin{array}{r} 11010 \\ + 1010 \\ \hline 10011 \end{array}$

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

b)  $\begin{array}{r} 11110 \\ + 1010 \\ \hline 10100 \end{array}$

c)  $\begin{array}{r} 1.1001 \\ + 1.1101 \\ \hline 10.00101 \end{array}$

## Binary addition using 1's Compliment:

a)  $(22)_{10} \oplus (-8)_{10}$  \* 1's Compliment is taken  
 $\begin{array}{r} 22 - 10110 \\ 8 - 1000 \\ \hline \end{array}$  to negative numbers by changing  
 $i \rightarrow 0 \quad 8^0 \rightarrow 1$

$$\begin{array}{r} 1000 \\ 0111 \\ \hline 10110 \\ 00111 \\ \hline \underline{\underline{11100}} \end{array} \quad * \text{If any carry exists, add carry to LSB.}$$

b)  $-(1101)_{10} \oplus (0110)_{10}$

$$\begin{array}{r} 1101 \\ 0010 \\ \hline \underline{\underline{1000}} \end{array} \quad \begin{array}{r} 0110 \\ 0110 \\ \hline \underline{\underline{1000}} \end{array}$$

## Binary addition using 2's Compliment:

a)  $(102)_{10} \oplus -(88)_{10}$

$$102 - (110010)_2 \quad \begin{array}{r} 88 - 1011000 \\ 10 \text{ comp} - 0100111 \\ + 1 \\ \hline \underline{\underline{0101000}} \end{array}$$

$$\begin{array}{r} 110010 \\ 010000 \\ \hline \underline{\underline{1010}} \end{array}$$

b)  $-(10010)_{10} \oplus -(74)_{10}$

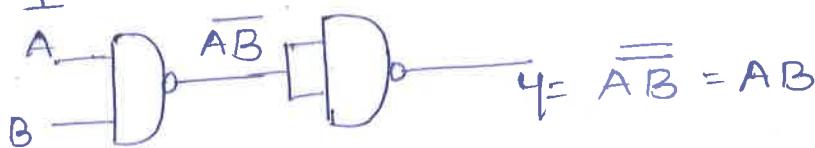
$$\begin{array}{r} 10010 \\ 01101 \\ + 1 \\ \hline \underline{\underline{01100}} \end{array}$$

$$\begin{array}{r} 74 - 1001010 \\ 10 \text{ comp} - 0110101 \\ + 1 \\ \hline \underline{\underline{0110110}} \end{array}$$

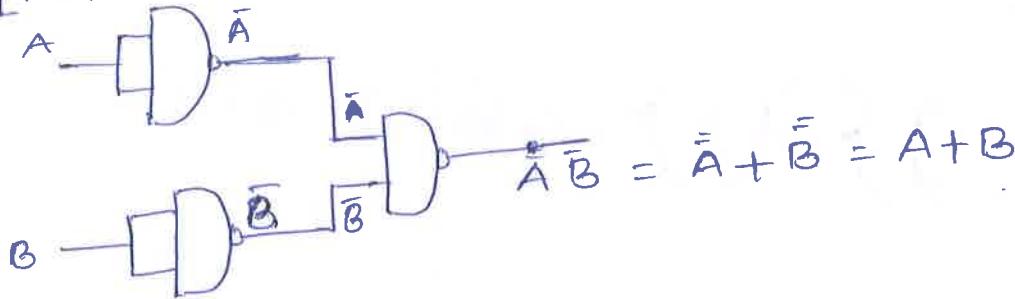
$$\begin{array}{r} 11110 \\ 0110110 \\ + 1 \\ \hline \underline{\underline{1000010}} \end{array}$$

NAND is a universal gate:

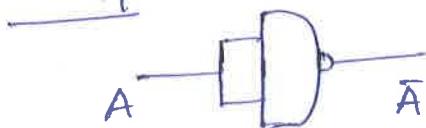
AND gate:



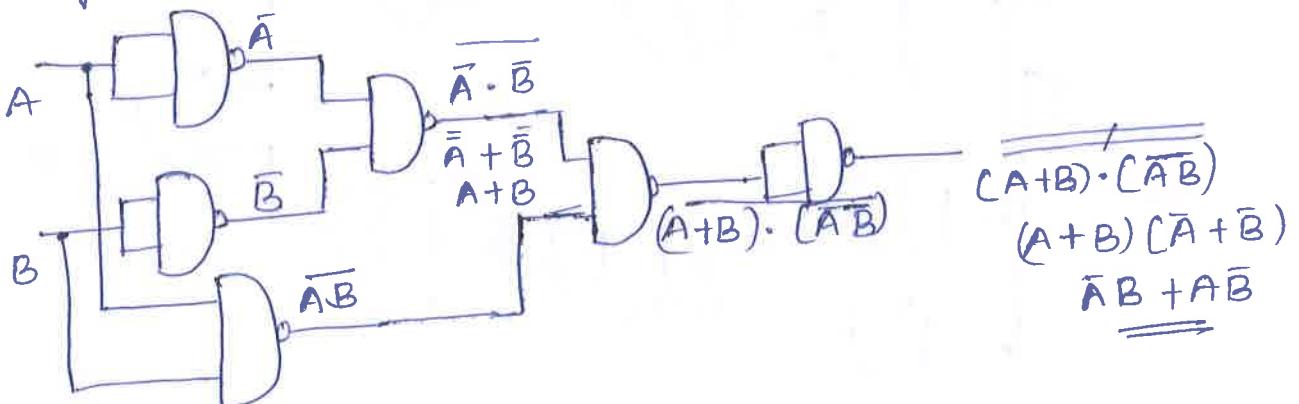
OR gate:



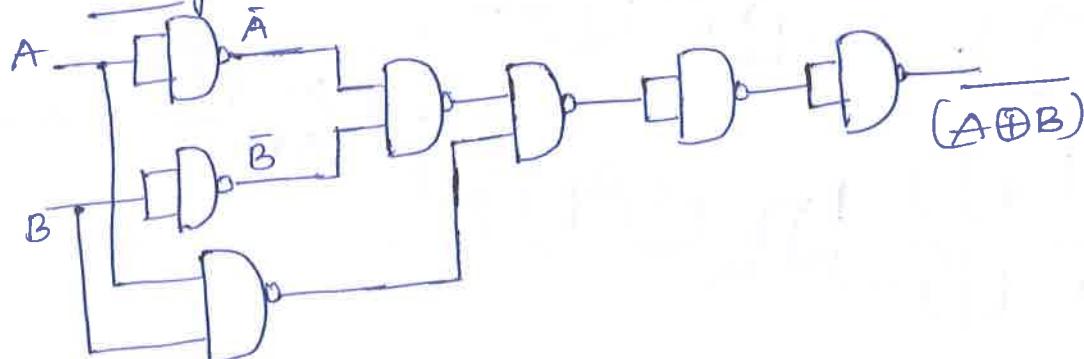
NOT gate:



XOR gate:

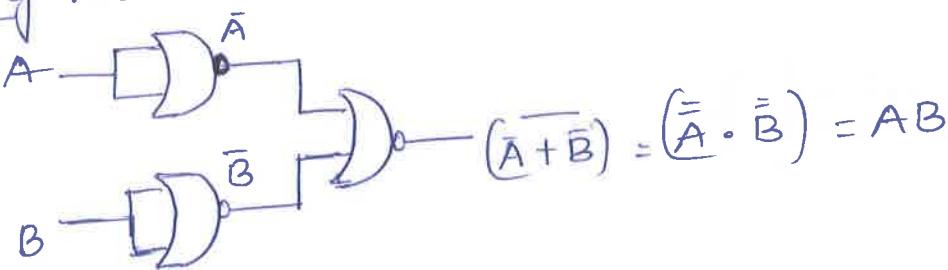


XNOR gate:

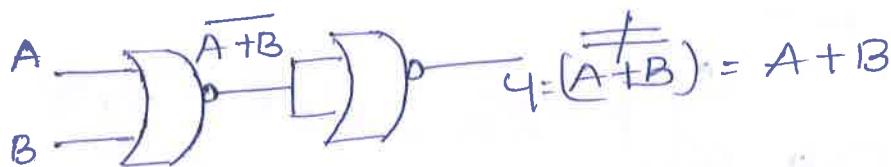


NOR is a universal gate:

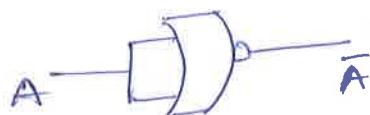
AND gate:



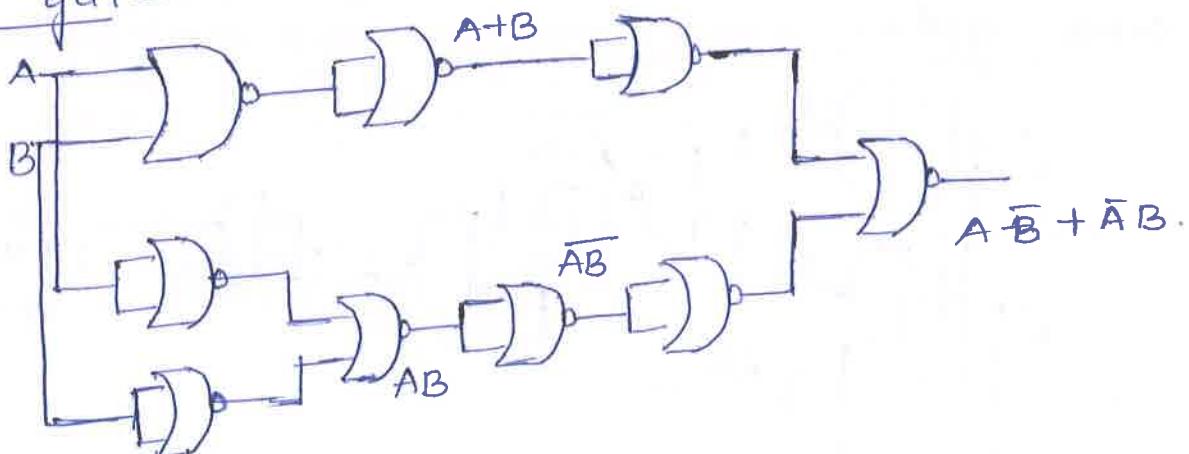
OR gate:-



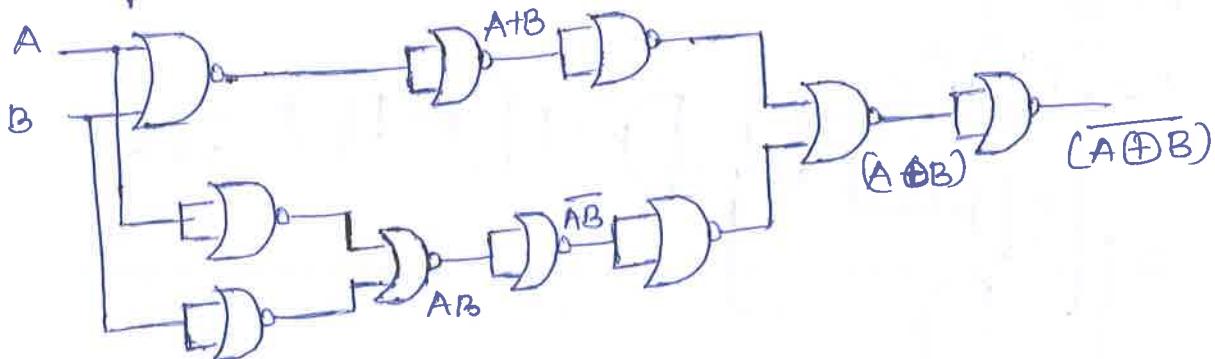
NOT gates:-



XOR gate:



XNOR gate:



De Morgan's Theorem :-

Statement 1: The complement of the product of two or more variables is equal to the sum of the complements of the variables.

Complements of the variables  
i.e.  $\overline{AB} = \bar{A} + \bar{B}$  - ①

Statement 2: The complement of the sum of two or more variables is equal to the product of the variables.

Complements of the  
i.e.  $\overline{A+B} = \bar{A} \cdot \bar{B}$  - ②

prod

## Boolean laws:

## Boolean law

## Annullment

## Identity

Idempotent

## Complement

## Commutative

Business

Absorptive  
Associative

## Boolean Expression

$$A+I=I \quad \bar{q} \quad A \cdot 0=0$$

$$A + 0 = A \quad \& \quad A - 1 = A$$

$$A+A=A \quad \& \quad A \cdot A=A$$

$$A + \bar{A} = I \quad \epsilon_A A \cdot \bar{A} = 0$$

$$\{ A \cdot B = B \cdot A, A + B = B + A \}$$

$$AB + C = ABC + AC$$

$$\begin{cases} A + BC = C \\ A + AB = A \end{cases}$$

$$| A + (B+C) = A+B+C \& A$$

Involution  $\bar{\bar{A}} = A$

$$\text{Absorption } AB + A\bar{B} = A$$

$$A + \bar{A}B = A + B$$

$$A \cdot (\bar{A} + B) = A \cdot B$$

## Simplification of boolean expression:

→ Simplify the following boolean expression & Implement using NAND gate.

$$(i) Q = C + \overline{B} \overline{C}$$

But  $\overline{BC} = \overline{B} + \overline{C}$  - DeMorgan's law

$$\therefore Q = C + (\overline{B} + \overline{C})$$

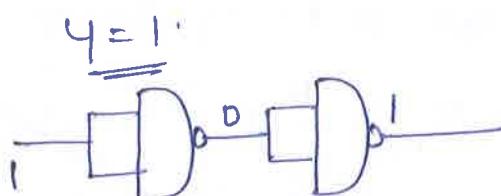
Let if  $\overline{B} + \overline{C} = X$ ,  $C + X = X + C$

$$\therefore Q = C + X$$
  
$$= (\overline{B} + \overline{C}) + \overline{B}$$

But  $C + \overline{C} = 1$

$$Q = 1 + \overline{B}$$

But  $1 + \overline{B} = 1$



$$(ii) Q = \overline{AB}(\overline{A} + B)(\overline{B} + B)$$

$$= \overline{AB}(\overline{A}\overline{B} + AB + B\overline{B} + BB)$$

But  $B\overline{B} = 0$  &  $BB = B$

$$\therefore Q = \overline{AB}(\overline{A}\overline{B} + AB + B)$$

$$= \overline{AB}(\overline{A}\overline{B} + B(A + 1))$$

But  $A + 1 = 1$

$$\therefore Q = \overline{AB}(\overline{A}\overline{B} + B) \quad \text{DeMorgan's law } \overline{AB} = \overline{A} + \overline{B}$$

$$= \overline{A}\overline{B}(\overline{A} + \overline{B})(\overline{A}\overline{B} + B)$$

$$Q = \overline{A}\overline{A}\overline{B} + \overline{A}\overline{B} + \overline{B}\overline{A}\overline{B} + \overline{B}\overline{B}$$

$$\text{But } \bar{B}B = 0, \bar{A}\bar{A} = \bar{A}$$

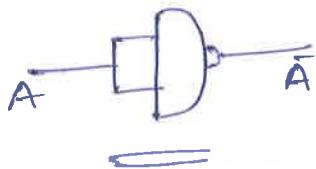
$$\therefore y = \bar{A}\bar{B} + \bar{A}B + A\bar{B} \quad \text{But } \bar{A}\bar{B} + \bar{A}B = \bar{A}\bar{B}$$

$$= \bar{A}B + \bar{A}\bar{B}$$

$$= \bar{A}(B + \bar{B})$$

$$\text{But } A + \bar{A} = 1, \text{ thus } B + \bar{B} = 1$$

$$\underline{\underline{y = \bar{A}}}$$



$$(III) y = (A+C)(AD + A\bar{D}) + AC + C$$

$$y = (A+C)A(D + \bar{D}) + C(A+1)$$

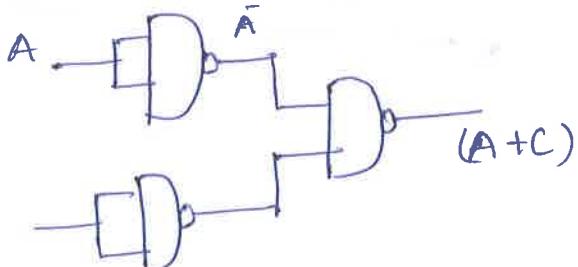
$$\text{But } D + \bar{D} = 1 \quad A+1 = 1.$$

$$\therefore y = (A+C) \cdot (A+C)$$

$$\text{But let } (\bar{A}+C) = x$$

$$\text{Thus } y = x \cdot x = x.$$

$$y = (A+C)$$



$$(IV) \text{ Show that } \bar{A}(A+B) + (B+AA)(A+\bar{B}) = A + \cancel{B}$$

$$y = \bar{A}(A+B) + (B+AA)(A+\bar{B})$$

$$\text{But } AA = A$$

$$= \bar{A}(A+B) + (B+A)(A+\bar{B})$$

$$\text{But } \cancel{B+A} = A + \bar{B}$$

$$\text{But } (B+A) = A + B$$

$$= \bar{A}(A+B) + (A+B)(A+\bar{B})$$

$$\text{But } (\bar{A}+B)(\bar{A}+B) = A$$

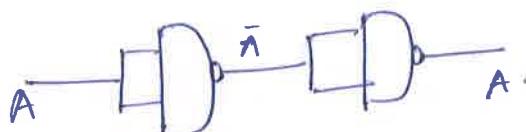
$$\therefore Y = \bar{A}(\bar{A}+B) + A$$

$$= \bar{A}\bar{A} + AB + A$$

$$= 0 + B(B+1)$$

$$\text{But } B+1=1$$

$$\therefore Y = \underline{\underline{A}} \cdot 1 = \underline{\underline{A}}$$



Q) Simplify the following boolean expression & implement by using NOR gate only.

$$(1) Y = \bar{A}B + B\bar{C} + BC + A\bar{B}\bar{C}$$

$$= \bar{A}B + B(\bar{C} + C) + A\bar{B}\bar{C}$$

$$\bullet \text{ But } \bar{C} + C = 1$$

$$Y = \bar{A}B + B + A\bar{B}\bar{C}$$

$$= B(\bar{A} + 1) + A\bar{B}\bar{C}$$

$$\text{But } \bar{A} + 1 = 1$$

$$Y = B + A\bar{B}\bar{C}$$

$$= B + \bar{B}\bar{A}\bar{C}$$

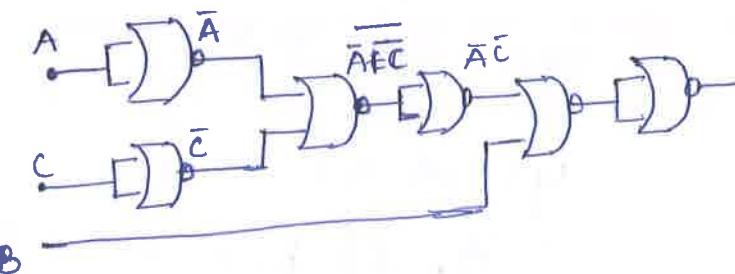
$$\text{let } X = \bar{A}\bar{C}$$

$$Y = B + \bar{B}X$$

$$\text{But } A + \bar{A}B = A + B$$

$$\therefore Y = X + B$$

$$Y = \underline{\underline{\bar{A}\bar{C} + B}}$$



(ii) Show that  $(A+B)(A+C) = A+BC$

$$\text{SOL: let } y = (A+B)(A+C)$$

$$= A \cdot A + A \cdot C + AB + BC \quad \text{But } A \cdot A = A$$

$$= A + AC + AB + BC$$

$$= A(1+C) + AB + BC$$

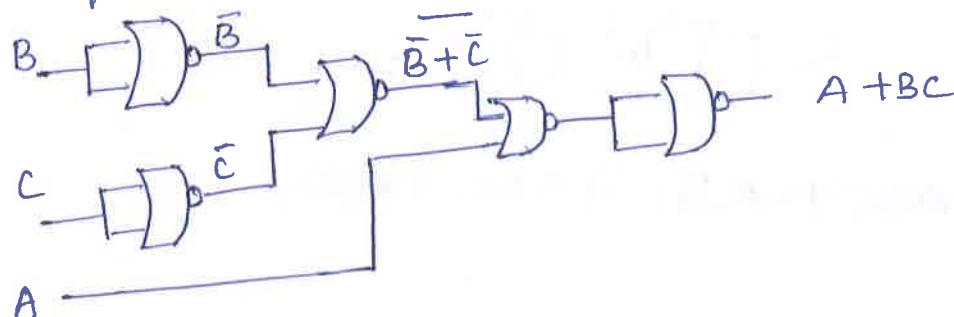
$$\text{But } 1+C=1$$

$$= A + AB + BC$$

$$= A(1+B) + BC$$

$$\text{But } 1+B=1$$

$$y = A + BC$$



$$(iii) y = ABC + \bar{A} + A\bar{B}C$$

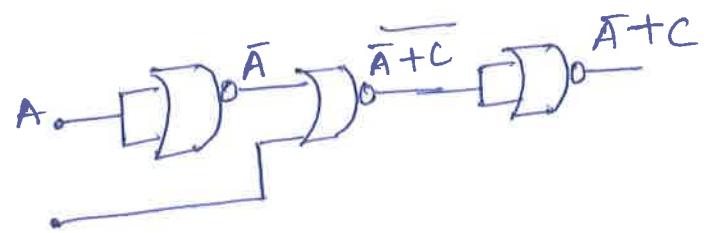
$$= A(BC + A(\bar{B} + \bar{C})) + \bar{A}$$

$$\text{But } B + \bar{B} = 1$$

$$y = AC + \bar{A}$$

$$\bar{A} + AB = A + C$$

$$y = \underline{\bar{A} + C}$$



$$(iv) y = (\bar{A}\bar{B}C) + (\bar{A}BC) + (\bar{ABC}) + (ABC)$$

$$\text{But } \bar{A}\bar{B}C + \bar{A}BC = \bar{ABC}$$

$$y = (\bar{ABC}) + \bar{ABC} + ABC$$

$$= \bar{ABC} + BC(\bar{A} + A) \quad \text{But } A + \bar{A} = 1$$

$$Y = \overline{ABC} + BC$$

DeMorgan's law  $\overline{AB} = \overline{A} + \overline{B}$

$$Y = (\overline{A} + B)C + BC$$

$$= \overline{AC} + \overline{BC} + BC$$

$$= \overline{AC} + C(\overline{B} + B)$$

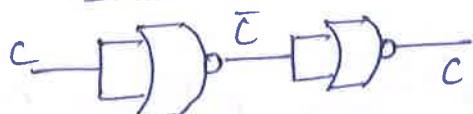
$$\overline{B} + B = 1$$

$$Y = \overline{AC} + C$$

$$Y = C(\overline{A} + 1)$$

$$\text{But } \overline{A} + 1 = 1$$

$$Y = \underline{\underline{C}}$$



$$(v) \cancel{Y = ABC + \overline{A}\overline{B}C + \overline{A}BC + \overline{A}\overline{B}C}$$

### Half adder

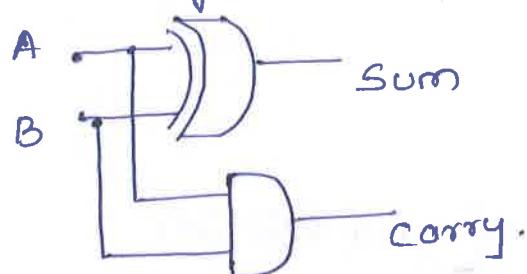


A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

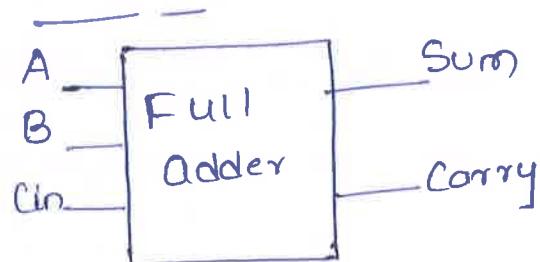
$$\text{Sum} = \bar{A}B + A\bar{B} = A \oplus B$$

$$\text{Carry} = AB$$

The complete logical diagram is



### Full adder:



A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$\text{Sum} = \bar{A}\bar{B}\text{Cin} + \bar{A}B\bar{\text{Cin}} + A\bar{B}\bar{\text{Cin}} + AB\text{Cin}$$

$$= (\bar{A}\bar{B} + AB)\text{Cin} + \bar{\text{Cin}}(\bar{A}B + A\bar{B})$$

$$\text{let } \bar{A}B + A\bar{B} = X \quad \text{ & } \bar{A}\bar{B} + AB = \bar{X}$$

$$= \bar{X}\text{Cin} + X\bar{\text{Cin}}$$

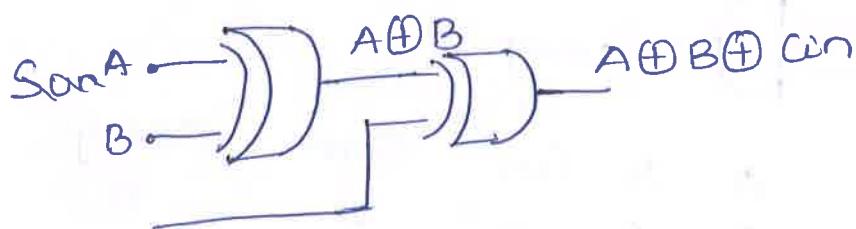
$$= X \oplus \text{Cin}$$

$$= (\bar{A}\bar{B} + A\bar{B}) \oplus \text{Cin}$$

$$\underline{\text{Sum}} = A \oplus B \oplus \text{Cin}$$

$$\begin{aligned}
 \text{Carry} &= \bar{A}B\bar{C}\bar{n} + \bar{A}\bar{B}C\bar{n} + A\bar{B}\bar{C}\bar{n} + AB\bar{C}\bar{n} \\
 &= \bar{A}B\bar{C}\bar{n} + A\bar{B}C\bar{n} + AB(\bar{C}\bar{n} + \bar{C}\bar{n}) \\
 &= \bar{A}B\bar{C}\bar{n} + A\bar{B}C\bar{n} + AB\cdot
 \end{aligned}$$

=



## Unit 4:

## SEMICONDUCTOR DEVICES:

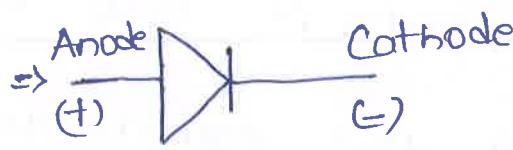
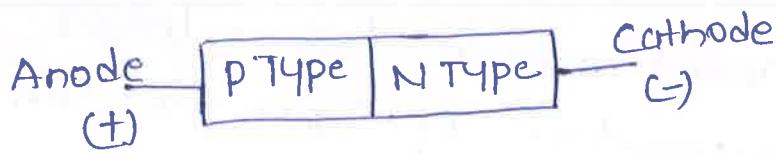
### 1. DIODE:

Diode is a two terminal devices, which is made up of p-type & n-type semiconductors. So it is also called as PN-junction diode. This non-linear conductors only in one direction that is in forward bias condition i.e. Connecting p-type to positive terminal & n-type to negative terminal. So it is also known as unidirectional device.

In forward bias condition, the diode will conduct only when the applied (biasing) voltage becomes greater than the threshold voltage i.e. for silicon type diode the threshold voltage is  $V_{th} \geq V_T$ . For germanium type diode  $0.1 - 0.3V$ .

The term threshold voltage means, it is the minimum required voltage for the device to get turn-on. If the applied voltage is less than the threshold voltage, then the diode will remain's in OFF (or) it is reverse biased.

The symbolic representation of this two terminal device (DIODE) is as shown below.

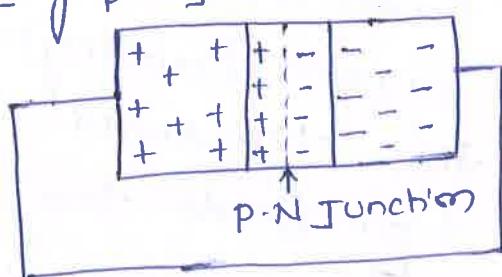


## V-I Characteristics:

The voltage - current characteristic of a diode is obtained when the diode is get biased properly. There are three possible biasing conditions for the diode, they are : (i) zero bias.  
(ii) Forward biasing  
(iii) Reverse biasing.

The term biasing, it is external voltage which decreases potential barrier & makes the device to work in suitable region.

i) Zero biasing: p-region N-region



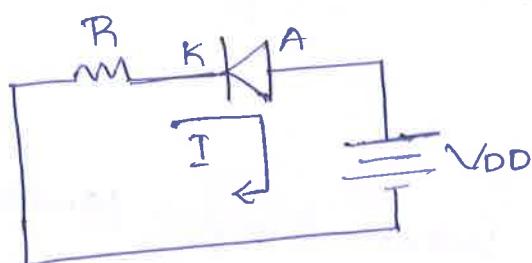
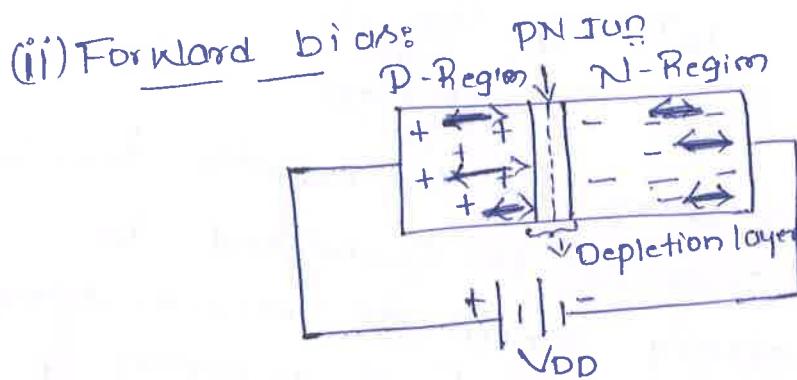
When no external voltage applied to a diode, then terminal are shorted together. results in diffusion of holes from p-type & crosses the barrier potential similarly the majority charge carriers of (electrons) diffused from n-type & crosses the barrier potential. This barrier potential helps few free electrons in p-region & holes in n-region to drift across the junction.

When equal number of majority charge carriers are equal in both n-type & p-type, an equilibrium is established, so that the net current in the circuit is 0.

But this equilibrium won't remain for a longer time, because as the temperature of PN junction is increased, the generation of minority charge carriers

2

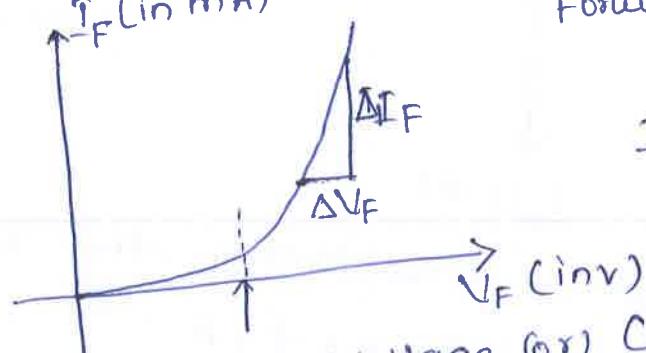
also get increases which raises the thermal energy, which broke the equilibrium between the junction. It results in increase of leakage current but an electric current cannot flow since no circuit has been connected to the PN junction.



When the p-region (Anode) connected to positive terminal & n-region (cathode) connected to negative terminal of the battery, is known as forward bias condition. When the value of external voltage greater than the cut-in voltage (or) threshold voltage the majority charge carriers from p-type & n-type are get repelled from the positive & negative terminal of the battery & comes the barrier junction, results in the flow of current from p-type to n-type.

The generated is called as forward current ( $I_F$ ) from a forward voltage ( $V_F$ ) mentioned as  $V_{DD}$ . The V-I charac of a forward biased diode is given by.

$$\text{Forward resistance } R_F = \frac{\Delta V_F}{\Delta I_F}$$

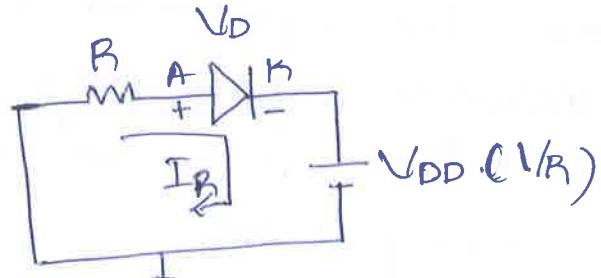
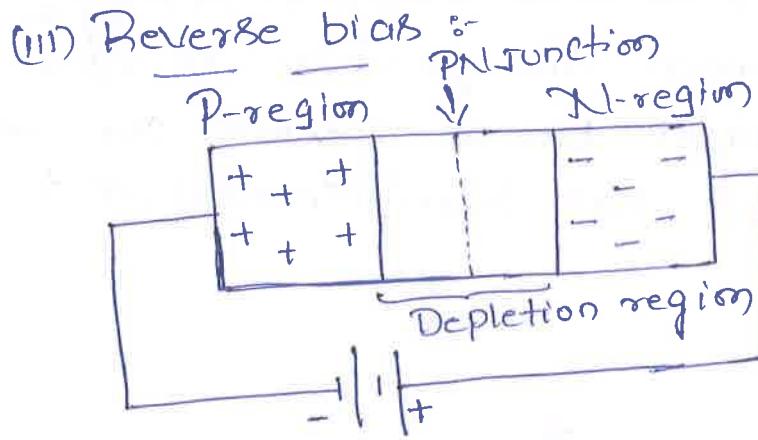


$$I_F R - V_D - V_F = 0$$

$$I_F = \frac{V_D + V_F}{R}$$

Knee voltage (or) Cut-in voltage.

In forward bias the width of depletion region is less.



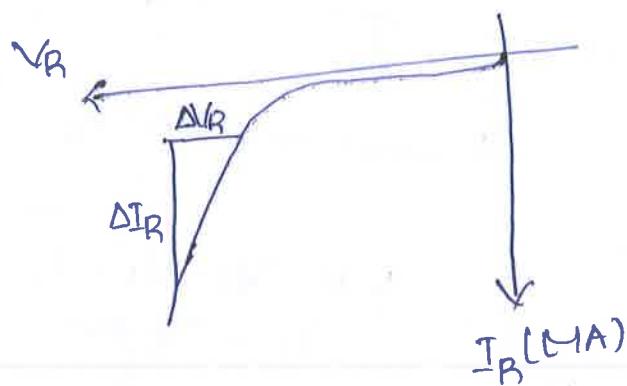
$$I_B R - V_D - V_{DD} = 0$$

$$I_B = \frac{V_R + V_{DD}}{R}$$

When P-region (Anode) is connected to negative terminal of the battery & n-region (cathode) is connected to positive terminal of the battery known as reverse biasing. That negative voltage attracts holes from P region & positive voltage attracts electrons from n region. This attraction of charge carriers widens the width of depletion region. & it presents high resistance. results in high barrier potential. Thus a very small leakage current (I<sub>A</sub>) flows in semiconductor.

This leakage current is known as reverse current & voltage which generates this reverse current known as reverse voltage.

The V-I characteristics of this biasing is shown



$$\text{Reverse resistance } R_R = \frac{\Delta V_R}{\Delta I_R}$$

For silicon type semiconductor, the reverse current is  $\sim 0.02 \text{ A}$  & for germanium  $- 0.05 \text{ A}$ .

## Diode Parameters:-

Knee voltage: The forward voltage at which the current through the diode starts increasing rapidly is knee voltage. It is also called as cut-in voltage (or) threshold voltage.

Forward voltage ( $V_F$ ): It is the voltage drop across the diode, which breaks the barrier potential & makes the diode to conduct.

Reverse voltage ( $V_R$ ): It is the voltage drop across the diode which increases the barrier potential & makes the diode to operate as a conductor at very small leakage current.

Peak inverse voltage (PIV): It is the maximum voltage at which diode can withstand in reverse direction without breaking down.

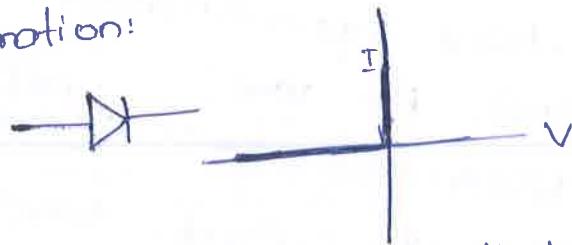
Forward Current ( $I_F$ ): It is the maximum current generated by a forward voltage ( $V_F$ ).

Reverse Current ( $I_R$ ): It is the minimum current generated by a reverse voltage ( $V_R$ ).

## Diode Approximations:-

The diode approximations are way to analyse the diode in circuit. There are three approximations, in all the cases diode acts as a switch.

### (1) First approximation:

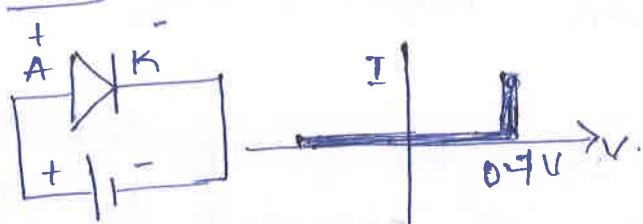


\* In this approximation, the diode is an ideal diode. Ideal diode means it acts like a perfect conductor under

forward bias & insulator under reverse bias.

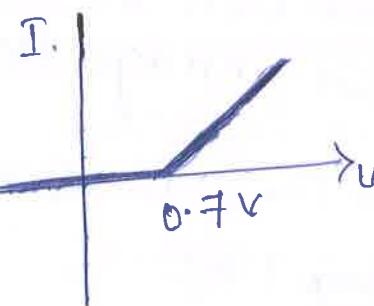
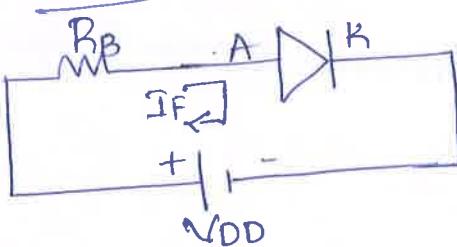
- \* In ideal situation diode doesn't consume any voltage & doesn't have any resistance.
- \* It is not used for real-time situations but just as general approximations when precision isn't needed.

### (ii) Second approximation:-



In this approximation, the diode is get biased through a external supply voltage to get turn ON after knee point. For Silicon knee point is b/w 0.5 - 0.7V & for Germanium knee point is between 0.1 - 0.3V.

### (iii) Third approximation:



$$V_{DD} - I_F R_B - V_D = 0$$

$$V_{DD} = V_D + I_F R_B$$

$$I_F = \frac{V_{DD} - V_D}{R_B}$$

In this approximation, a bulk resistance (Resistance of p-type & n-type material) connected in series with a diode across a voltage  $V_F$ . It is most commonly used circuit in many real-time applications.

The second approximation is used when load resistance is high whereas third approximation circuit is used when load resistance is low. not fixed but it changes according

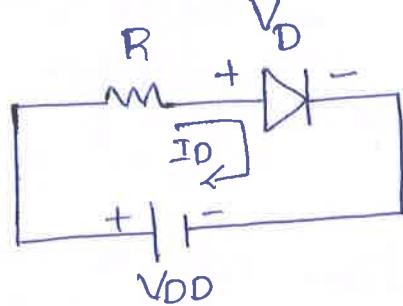
The value of bulk resistance is not fixed but it is to the forward voltage & current through diode. It's value is in b/w  $1\Omega$  to  $10\Omega$ .

## DC load line Analysis

A DC load line analysis is the graphical analysis of non-linear electronic devices like diode or transistor which determines the DC operating point (or) Q point of it.

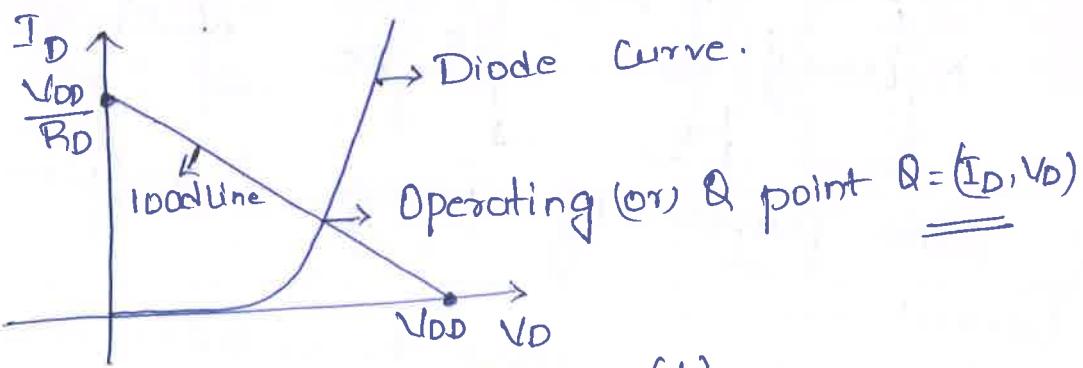
It usually draw on a characteristic curve of a diode & load line is a straight line. The intersection point of load line & curve gives the Q point of a diode.

Let consider a circuit as per third approximation.



$$V_{DD} - I_D R - V_D = 0 \quad \text{--- (1)}$$

By applying KVL  $V_{DD} - I_D R - V_D = 0$  give by  
The V-I characteristic of diode is given by



To obtain load line equation, from (1)  
when  $V_D = 0$  then

$$I_D = \frac{V_{DD} - V_D}{R_D} \quad \text{--- (2)}$$

$$I_D = \frac{V_{DD}}{R_D} \quad \text{--- (2)}$$

$$\text{When } I_D = 0, \Rightarrow 0 = \frac{V_{DD} - V_D}{R_D}$$

$$V_{DD} = V_D \quad \text{--- (3)}$$

Mark (2) & (3) on the Characteristic Curve

## Half - Wave Rectifier:

A rectifier is an electrical device which converts alternating current into pulsating direct current.

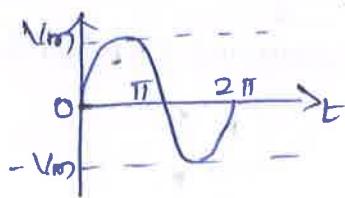
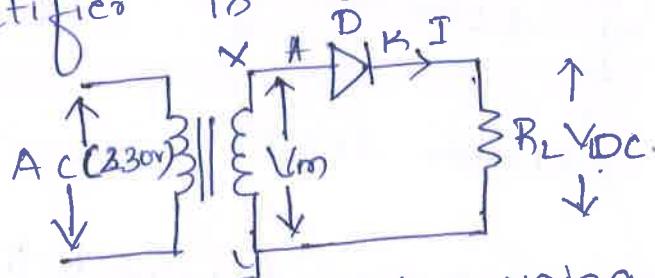
A rectifier circuit may be single phase or three phase (multi phase). The domestic equipment phase rectifier single-phase rectifier is used & multi phase rectifier is used in industries.

Based on the applications rectifiers are broadly classified into:

- a) Half wave rectifier
- b) Full wave rectifier
- c) Bridge type rectifier

## Half wave rectifiers:

The circuit configuration of a half wave rectifier is shown in the figure.



The purpose of using transformer in a rectifier circuit is:

(i) It can be used to obtain desired DC voltage value

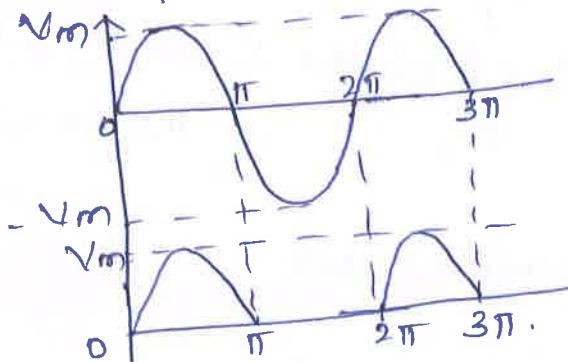
(ii) It provides isolation from the power line.

The primary winding of a transformer is connected to AC supply & this induces an AC voltage across the secondary winding of the transformer.

During positive half cycle:

In positive half cycle, the point X is positive wrt point Y in secondary which forward biases the diode. As a result current flows through the resistor  $R_L$ .

The forward biased diode offers very low resistance & hence voltage drop across the diode is small. Thus voltage across the load is almost equal to input voltage at every instant.



During negative half cycles:

In negative half cycle, X is negative wrt Y reverse biases the diode. As a result no current flows through the load resistor.

Since the rectification is done only for positive half cycle, it is named as HALF WAVE rectifier.

Advantages:-

- \* Easy to construct, since it is having only one diode.

## Disadvantage:

- \* The output is low.
- \* The output contains more ripples.
- \* Efficiency is quite low.

## Rectifier parameters:

### (i) Average DC Current ( $I_{DC}$ ):

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} I_L \cdot dt$$

Area of one cycle.

$$\text{load current } I_L = \begin{cases} I_m \sin(\omega t) & ; 0 \leq \omega t \leq \pi \\ 0 & ; \pi \leq \omega t \leq 2\pi \end{cases}$$

$$\begin{aligned} \therefore I_{DC} &= \frac{1}{2\pi} \int_0^{\pi} I_m \sin(\omega t) \cdot dt \\ &= \frac{-I_m}{\omega\pi} [-\cos(\omega t)]_0^\pi \\ &= \frac{-I_m}{\omega\pi} [\cos(\pi) - \cos(0)] \\ &= \frac{-I_m}{\omega\pi} [-1 - 1] = \frac{2I_m}{\omega\pi} \end{aligned}$$

$$\underline{I_{DC}} = \frac{I_m}{\cancel{\omega\pi}} \rightarrow I_m - \text{maximum current} = \frac{V_m}{R_s + R_f + R_L}$$

$R_s$  - Secondary resistance  
 $R_f$  - forward resistance

### (ii) Average DC voltage

$$\begin{aligned} V_{DC} &= I_{DC} \times R_L \\ &= \frac{I_m}{\pi} \times R_L \\ &= \frac{V_m}{(R_s + R_f + R_L)\pi} \times R_L \end{aligned}$$

$$= \frac{V_m}{\left( \frac{R_s + R_f}{R_L} + 1 \right) \pi}$$

If  $R_s + R_f \ll R_L$ , then  
 $\frac{R_s + R_f}{R_L} \ll 1$ .

$$\therefore V_{DC} = \frac{V_m}{\pi}$$

(iii) Rms value of load current ( $I_{rms}$ )

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} (I_L)^2 \cdot dwt}$$

Note's Root mean square is used to measure both alternating & direct current (or) voltage value. Since AC signals are varying consecutively from positive to negative. Hence to find mean value of AC signal square root is taken to sum of their squares.

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{\pi} (I_m \sin wt)^2 \cdot dwt} \quad \sin^2 \theta = \frac{1 - \cos 2\theta}{2}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \int_0^{\pi} \left[ 1 - \frac{\cos 2wt}{2} \right] dwt}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \int_0^{\pi} \frac{dwt}{2} - \int_0^{\pi} \frac{\cos 2wt}{2} \cdot dwt}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \left[ \frac{wt}{2} \right]_0^{\pi} - \left[ \frac{\sin 2wt}{4} \right]_0^{\pi}}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \left[ \frac{\pi}{2} - 0 \right]}$$

$$= I_m \sqrt{\frac{1}{2\pi} \times \frac{\pi}{2}} = I_m \cdot \sqrt{\frac{1}{4}}$$

$$\underline{I_{rms} = \frac{I_m}{\sqrt{2}}}$$

Rms value of voltage ( $V_{rms}$ ):

$$V_{rms} = I_{rms} \times R_L$$

$$= \frac{I_m}{2} \times R_L$$

$$= \frac{V_m}{(R_s + R_f + R_L) \times 2} \times R_L$$

If  $R_s + R_f \ll R_L$

$$\frac{V_m}{R_L \times 2} \times R_L$$

$$= \frac{V_m}{\left( \frac{R_s + R_f + 1}{R_L} \right) \times 2} \times 2$$

If  $R_s + R_L \ll 1$ , then

$$\frac{V_m}{2}$$

$$V_{rms} = \underline{\underline{\frac{V_m}{2}}}$$

(iv) Efficiency ( $\eta$ ):

$$\eta = \frac{\text{DC output power}}{\text{RMS AC output power}} = \frac{P_{DC}}{P_{AC}}$$

$$P_{DC} = V_{DC} \times I_{DC}$$

$$= I_{DC} \times R_L \times I_{DC}^2$$

$$= I_{DC}^2 \times R_L$$

$$= \left( \frac{I_m}{2} \right)^2 \times R_L$$

$$P_{AC} = (I_{rms})^2 \times (R_s + R_f + R_L)$$

$$= \left( \frac{I_m}{2} \right)^2 \times (R_s + R_f + R_L)$$

$$= \frac{I_m^2}{4} (R_s + R_f + R_L)$$

$$\eta = \frac{I_m^2 / 4 \times R_L}{I_m^2 / 4 \times (R_s + R_f + R_L)}$$

$$= \frac{4}{\pi^2} \times \left( \frac{R_s + R_f + 1}{R_L} \right)$$

If  $R_s + R_f \ll R_L$ , then

$$\eta = \frac{4}{\pi^2} = \underline{\underline{40.6\%}}$$

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### (v) Ripple factor ( $\delta$ ):

The output of a half wave rectifier is not a pure DC component, but it is a pulsating DC component. A pulsating DC component contains both DC & AC, that will change in every short interval of time. These pulsating components called as ripples ( $\delta$ ).

$\delta = \frac{\text{RMS value of AC component of op}}{\text{DC component of output}}$

$$= \frac{I_{\text{rms}}}{I_{\text{DC}}} \quad \text{or} \quad \frac{V_{\text{rms}}}{V_{\text{DC}}}$$

$$= \sqrt{\frac{I_{\text{rms}}^2 - I_{\text{DC}}^2}{I_{\text{DC}}^2}}$$

$$= \sqrt{\left(\frac{I_{\text{rms}}}{I_{\text{DC}}}\right)^2 - 1} : \sqrt{\left(\frac{I_m}{\frac{I_m}{2}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2}\right)^2 - 1}$$

$$\underline{\underline{\delta = 1.21\%}}$$

### (vi) Voltage regulation:

$$VR = \frac{V_{\text{DC(NL)}} - V_{\text{DC(FL)}}}{V_{\text{DC(FL)}}}$$

$$V_{\text{DC(NL)}} = \frac{V_m}{\pi}$$

$$V_{\text{DC(FL)}} = I_{\text{DC}} \times R_L$$

$$= \frac{\frac{V_m}{\pi} - \frac{V_m}{\pi(R_s + R_f + R_L)} \times R_L}{\frac{V_m}{\pi(R_s + R_f + R_L)} \times R_L}$$

$$VR = \frac{\frac{V_{op}}{\pi} \left[ 1 - \frac{1}{R_s + R_f + R_L} \right] \times R_L}{\frac{V_{op}}{\pi} \cdot \frac{1}{(R_s + R_f + R_L)} \times R_L}$$

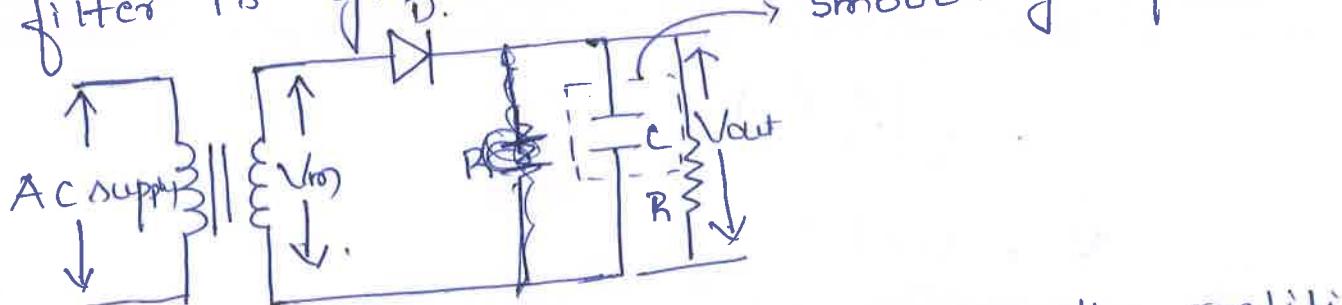
$$= \frac{1 - \frac{R_L}{R_s + R_f + R_L}}{\frac{R_L}{R_s + R_f + R_L}}$$

$$\therefore \frac{R_s + R_f - R_L}{R_s + R_f + R_L} = \frac{\frac{R_s + R_f - R_L}{R_s + R_f + R_L}}{\frac{R_L}{R_s + R_f + R_L}}$$

$$VR = \frac{R_s + R_f}{R_L} \times 100.$$

Half wave rectifier with capacitor filters  
 The pulsating component in rectified output charges regularly at each interval of time. These pulsating components are smoothed by using large value capacitors in parallel with the rectified source.

The circuit arrangement for half wave rectifier with filter is given below:



When the capacitor placed across the rectifier gets charged & store the charge during the conduction period & it will discharge through R during non-conduction period of rectifier.

Through this charging & discharging time process during the current flows through the load resistor  $R_L$  get increased & ripples gets decreased by a greater extent.

Thus for the ripple component with a frequency of MHz, the capacitor 'C' will offer lower impedance.

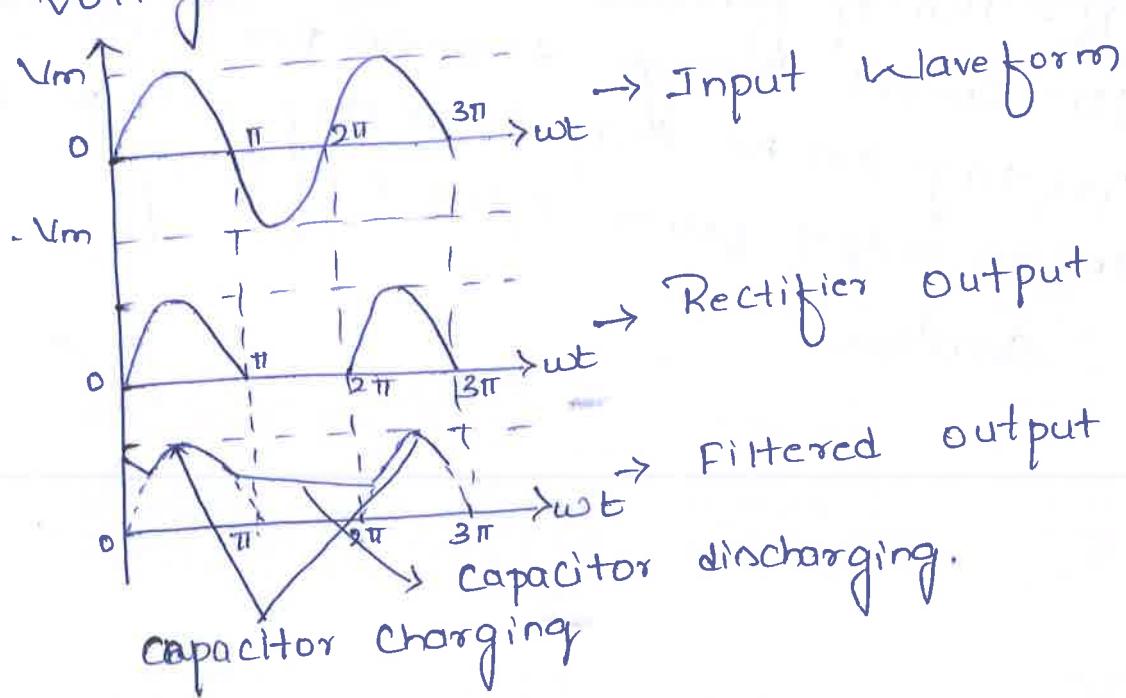
### Working:

During the positive half cycle, the diode is get forward biased & starts conducting. During this period, the capacitor 'C' charged to maximum input voltage ( $V_m$ ). It holds the charge until the ac supply reaches negative half cycle.

In negative half cycle the diode get reverse biased, then the capacitor 'C' discharge through  $R_L$  till the value of  $V_C$  become equal to  $V_L$ .

$$\text{Time constant } T_C = \frac{1}{R_C}$$

As soon as when  $V_C = V_L$  in next positive cycle the capacitor get charge to maximum value of the input voltage.



If the value of load resistance is high, then the discharge time constant ( $\tau_L$ ) will be high & thus capacitor get less time to discharge soon. This will reduces the amount of ripple in output & increases the output voltage.

Since the value of capacitor plays import role in determining the output ripples & dc output voltage, if the capacitor value is high, then amount of charge stored will be high & amount of discharge is less. Thus the ripples will be less & average dc level will be high.

The ripple factor of filtered rectified circuit is

$$\delta = \frac{1}{2\sqrt{3}fcR_L}$$

where  $f$  - operating frequency

$C$  - capacitor value

$R_L$  - load resistance

### Problems

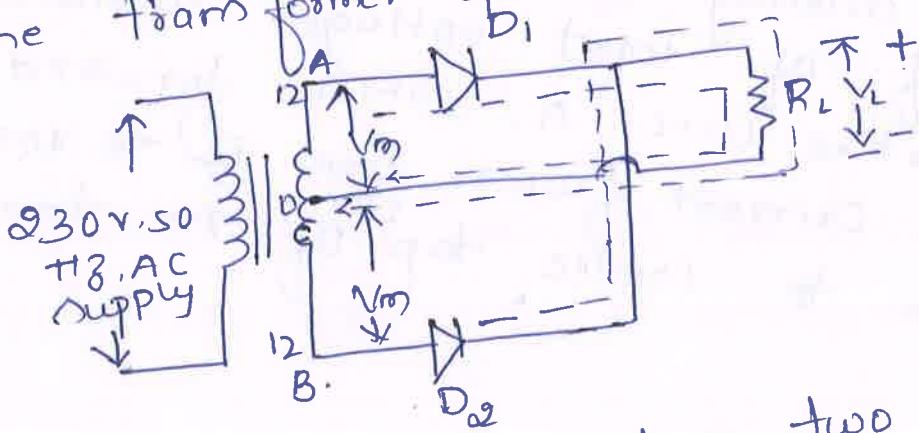
1. The input of a half wave rectifier is  $V_i = 500 \sin \omega t$ . If  $R_L = 1k\Omega$  & forward resistance of diode is  $500\Omega$ . Find  
 (i) DC Current through diode (ii) RMS value of current  
 & voltage (iii) DC output voltage (iv) AC output power  
 (v) DC output power & (vi) Efficiency.

### Solution:

## Full Wave rectifiers:

In half wave rectifier, the ripples are reduced by connecting a capacitor across rectifier. But this method is suitable for low power applications, but it won't give smooth & steady DC output voltage.

So to get smooth & steady DC voltage, diode should conduct for both positive & negative half cycle. This can be achieved by connecting the transformer & diode as shown in the figure.

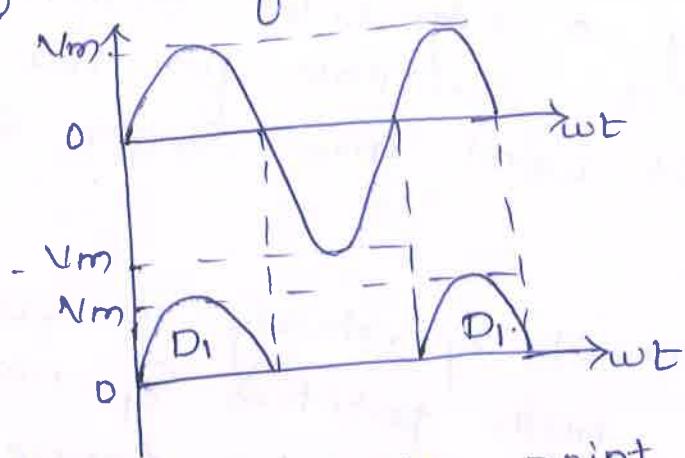


In this configuration, two diodes are connected to secondary windings for A & B terminals respectively. The cathode terminal of D1 & D2 are short circuited, & load resistance across D1 & D2 through centre tap.

### Working:

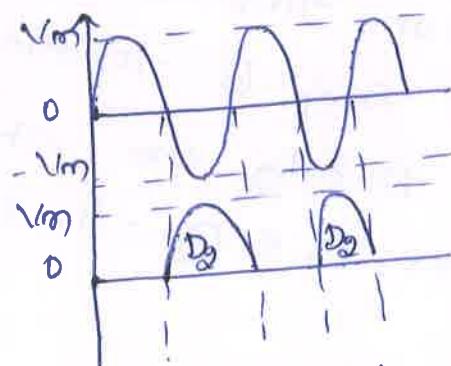
In positive half cycle, point A is positive wrt B & forward biased since a negative signal is applied to D2. The diode D1 & D2

then diode  $D_1$  allows current to pass through it, & it grounded through load resistance  $R_L$  at '0' of transformer.



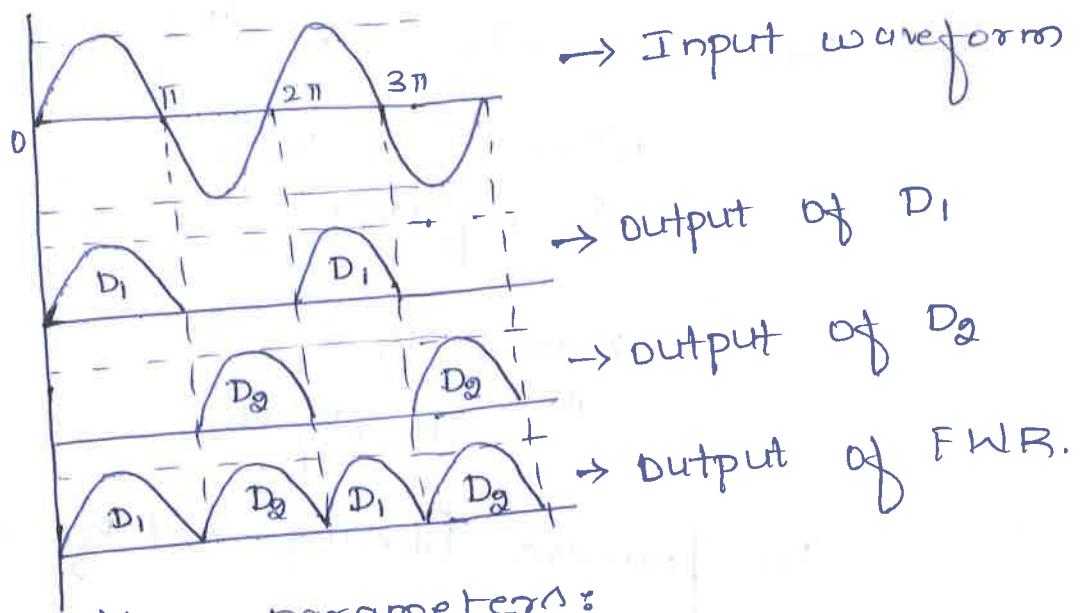
In negative half cycle point A point is negative wrt B, thus it reverse biases the diode  $D_1$ . The terminal B is already at  $-12v$  of input voltage then negative half of input voltage & make 'B' as positive wrt A, which biases the  $D_2$ . Then current flows from resistance  $R_L$ , then to centre tap of transformer, combined, forward  $D_2$  to load the transformer.

- mer.



From the output of  $D_1$  &  $D_2$ , it clearly shows that the diode  $D_1$  &  $D_2$  is conducted for both negative & positive cycle. Thus the circuit will conduct for complete cycle of input voltage. Thus it is named as Full wave rectifier.

The output of the full wave rectifier is as shown below: 10



### Full wave rectifier parameters:

#### (i) D.C output current

Area under each diode is  $\frac{\pi}{2}$

$$I_{dc} = \frac{1}{2\pi} \int_0^{\pi} I_L \cdot d\omega t$$

$$I_L = \begin{cases} I_m \sin(\omega t) & : 0 \leq \omega t \leq \pi \\ 0 & : \text{else} \end{cases}$$

$$I_{dc} = \frac{1}{\pi} \int_0^{\pi} I_m \sin(\omega t) \cdot d\omega t$$

$$= \frac{I_m}{\pi} \left[ -\cos(\omega t) \right]_0^\pi = \frac{I_m}{\pi} \left[ -\cos(\pi) - (-\cos(0)) \right]$$

$$= \frac{I_m}{\pi} \left[ -(-1) + 1 \right] = \frac{2I_m}{\pi}$$

Peak Current  $I_m = \frac{V_m}{R_s + R_f + R_L}$

## ii) DC Voltage: ( $V_{DC}$ )

$$V_{DC} = I_{DC} \times R_L = \frac{2I_m}{\pi} \times R_L$$

$$= \frac{2 \times V_m}{\pi (R_s + R_f + R_L)} \times R_L$$

$$= \frac{2V_m}{\pi} \times \frac{R_L}{R_s + R_f + R_L}$$

In forward biasing  $R_s + R_f \ll R_L$

$$V_{DC} = \frac{2V_m}{\pi} \times \frac{R_L}{R_s + R_f + R_L}$$

$$V_{DC} = \frac{2V_m}{\pi}$$

## (iii) RMS value of Current ( $I_{rms}$ )

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_L^2 \cdot dwt} = \sqrt{\frac{1}{2\pi} \int_0^{\pi} (I_m \sin \omega t)^2 dwt}$$

$$= \sqrt{\frac{I_m^2}{\pi} \int_0^{\pi} \sin^2 \omega t \cdot dwt} = \sqrt{I_m^2 \int_0^{\pi} \left(\frac{1 - \cos 2\omega t}{2}\right) \cdot dwt}$$

$$= I_m \sqrt{\frac{1}{\pi} \int_0^{\pi} \left(\frac{1 - \cos 2\omega t}{2}\right) \cdot dwt}$$

$$= I_m \sqrt{\frac{1}{\pi} \int_0^{\pi} \frac{dwt}{2} - \int_0^{\pi} \frac{\cos 2\omega t}{2} dwt}$$

$$= I_m \sqrt{\frac{1}{\pi} \left[ \frac{\pi}{2} - \frac{\sin 2\omega t}{4} \right]_0^{\pi}}$$

$$I_{rms} = I_m \sqrt{\frac{1}{\pi} \left[ \frac{\pi}{2} - D \right]} = I_m \sqrt{\frac{V_m}{2R}}$$

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$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

(v) RMS value of voltage ( $V_{rms}$ ) :

$$V_{rms} = I_{rms} \times R_L = \frac{I_m}{\sqrt{2}} \times R_L$$

$$= \frac{V_m}{\sqrt{2} (R_f + R_s + R_L)} \times R_L$$

$$= \frac{V_m}{\sqrt{2}} \frac{R_L}{R_f + R_s + R_L}$$

In forward biasing  $R_f + R_s \ll R_L$

$$V_{rms} = \frac{V_m}{\sqrt{2}} \times \frac{R_L}{R_f + R_s + R_L}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

(vi) Efficiency ( $\eta$ ):

$$\eta = \frac{P_{DC}}{P_{AC}}$$

$$\begin{aligned} P_{DC} &= V_{DC} \times I_{DC} \\ &= I_{DC} \times R_L \times I_{DC} \\ &= I_{DC}^2 \times R_L \\ &= \left( \frac{2I_m}{\pi} \right)^2 \times R_L = \underline{\underline{0.5I_m^2}} \end{aligned}$$

$$P_{AC} = I_{rms} \times I_{AC} = I_{rms} \times R_L \times I_{rms}$$

$$= I_{rms}^2 \times R_L$$

$$= \left( \frac{I_m}{\sqrt{2}} \right)^2 \times R_L$$

$$\eta = \frac{\frac{4}{\pi^2} \times I_{m0}^2 \cdot R_L}{\frac{I_{m0}^2}{2} \times R_L} = \frac{8}{\pi^2} \frac{I_{m0}^2}{I_{m0}^2} \times 100$$

$$\underline{\underline{\eta}} = 81.2\%$$

Ripple factor: (8):

$$8 = \frac{I_{AC}}{I_{DC}} = \sqrt{\frac{I_{rms}^2 - I_{DC}^2}{I_{DC}^2}} = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1}$$

$$8 = \sqrt{\frac{\left(\frac{I_m}{\sqrt{2}}\right)^2}{\frac{2I_m}{\pi}}} - 1 = \sqrt{\frac{\pi^2}{8} - 1}$$

$$\underline{\underline{8}} = 0.48$$

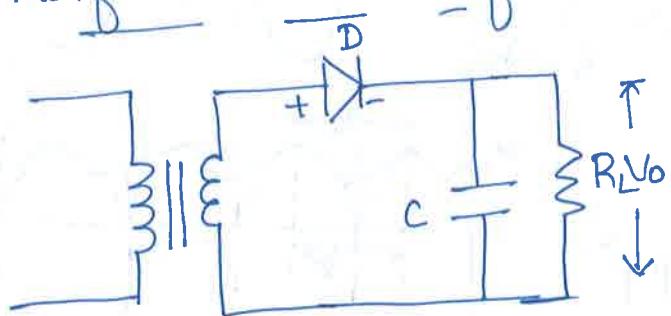
Voltage Regulation:

$$VR = \frac{(V_{DC})_{NL} - (V_{DC})_{FL}}{(V_{DC})_{FL}}$$

$$VR = \frac{R_s + R_B}{R_L} \times 100$$

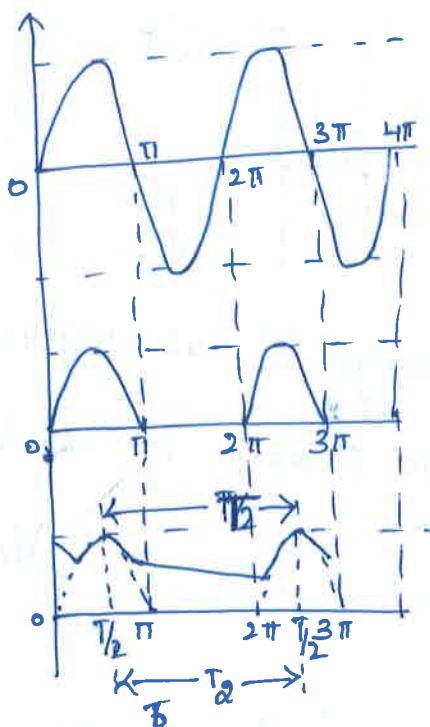
# Derivation of Ripple factor ( $\delta$ ) for a filtered circuit.

## 1. Half Wave Rectifier:



The charge it has acquired =  $V_{o-p-p} \times C$

The charge it has lost =  $I_{dc} \times T_2$



$$V_{o-p-p} \times C = I_{dc} \times T_2$$

The periodic time of waveform  $T_2 = T = \frac{1}{f}$ .

$$V_{o-p-p} = I_{dc} \times \frac{T_2}{C}$$

$$= \frac{I_{dc}}{fC}$$

The rms value of ripple waveform is :  $V_{rms} = \frac{V_{o-p-p}}{2\sqrt{3}}$

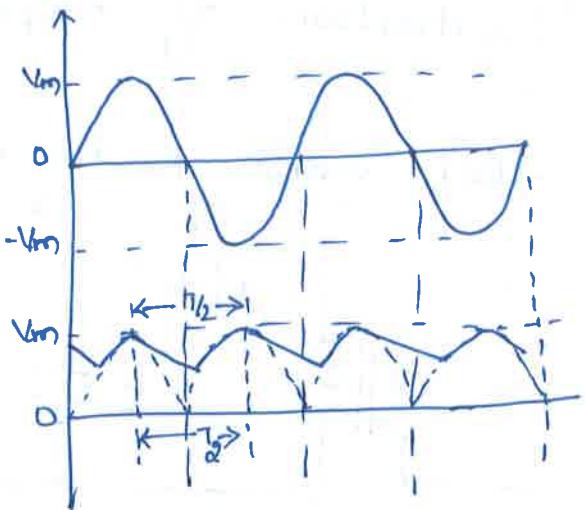
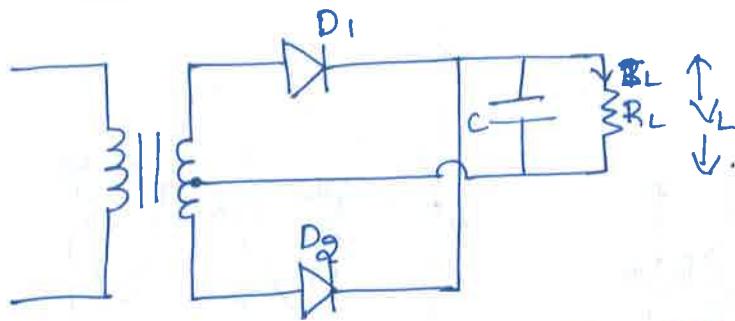
$$= \frac{I_{dc}}{2\sqrt{3}fC}$$

$$\text{But } I_{dc} = \frac{V_{dc}}{R_L} \quad \delta = \frac{V_{rms}}{V_{dc}}$$

$$\therefore V_{rms} = \frac{V_{dc}}{2\sqrt{3}fC R_L}$$

$$\frac{V_{rms}}{V_{dc}} = \delta = \frac{1}{2\sqrt{3}fC R_L}$$

## 2) Full wave rectifier:



The charge it has acquired =  $V_{op-p} \times C$

The charge it has lost =  $I_{dc} \times T_0$

$$V_{op-p} \times C = I_{dc} \times T_0$$

$$T_0 = \frac{T}{2} = \frac{1}{2f} \quad \therefore V_{op-p} = \frac{I_{dc}}{2fC}$$

The rms value of the ripple waveform is

$$V_{rms} = \frac{V_{op-p}}{\sqrt{3}} = \frac{I_{dc}}{4\sqrt{3}fC}$$

$$\text{But } I_{dc} = \frac{V_{rms}}{\sqrt{3}fC} = \frac{V_{dc}}{R_L} \quad \text{Efficiency } \eta = \frac{V_{rms}}{V_{dc}}$$

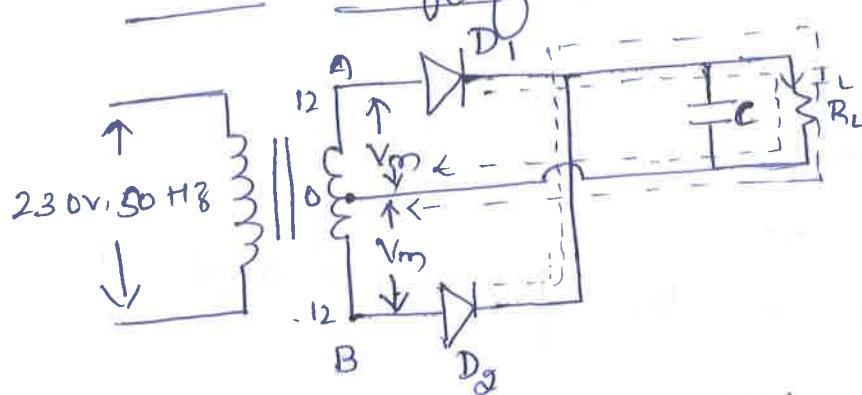
$$V_{rms} = \frac{V_{dc}}{\sqrt{3}fC R_L}$$

$$\underline{\underline{\frac{V_{rms}}{V_{dc}} = \gamma = \frac{1}{4\sqrt{3}fC R_L}}}$$

Note: The above derivation is also holds for Bridge-type full wave rectifier.

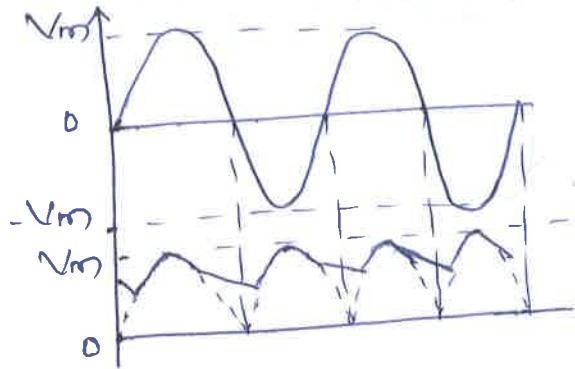
## Full wave rectifier with capacitor filter

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The circuit arrangement for full wave rectifier with filter is as shown in the figure. The working of full wave rectifier is almost same half wave rectifier but the only difference is in full wave rectifier both the output  $D_1$  &  $D_2$  in capacitive filter has filter out positive & negative half cycle.

In positive half cycle  $D_1$  is forward biased. & the capacitor charges to maximum value of the input only when the applied input voltage greater than the capacitor voltage. During the conduction period of diode  $D_1$  capacitor stores the charge & starts the AC voltage. When the AC voltage is less than the capacitor voltage, the capacitor starts discharging. The discharging of the capacitor is very slow, so the capacitor does not get enough time to discharge completely. Before the complete discharge, it again charges to maximum value three times from the output of full wave rectifier with filter as shown:

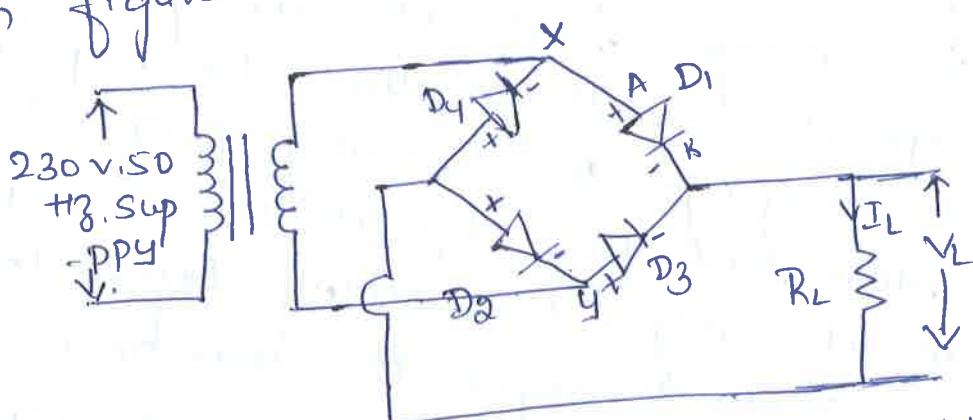


The ripple present in the filtered output is measured by  $\delta = \frac{1}{4\sqrt{3} + CR_L}$

### Bridge type full wave rectifier:

Even though full wave rectifiers convert both positive & negative half cycle of AC signal to its equivalent smooth output voltage, it is difficult to provide centre tap on secondary winding. Also for small applications full wave rectifier is not suitable.

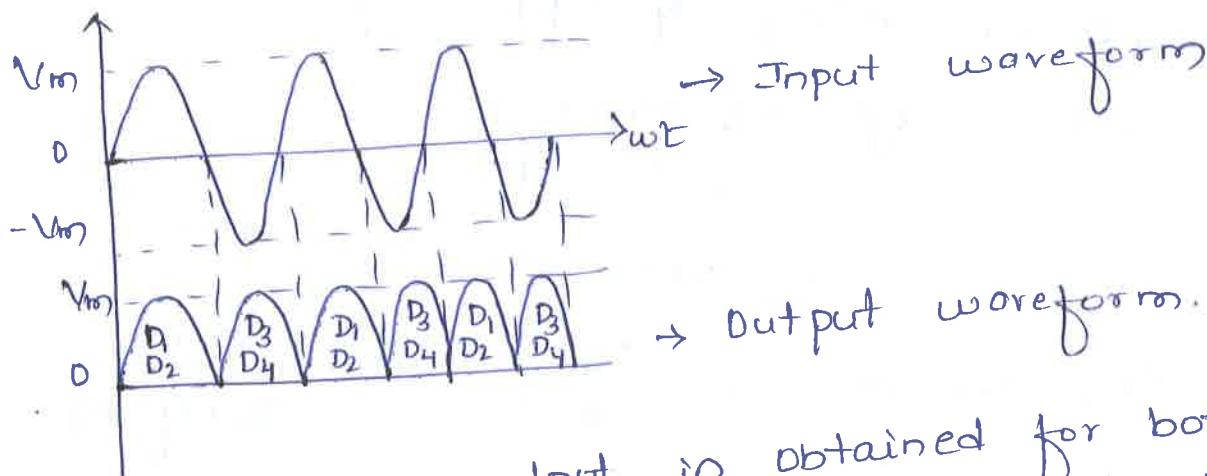
To overcome the problem of connected Centre tapping as shown in figure.



In positive half cycle, X is positive wrt to Y. This positive voltage forward biases the diode D1. Then the current flows through load resistance  $R_L$  & forward biases the diode  $D_2$ . Thus in positive cycle  $D_1$  &  $D_2$  are conducted.

In negative half cycle, point X is negative wrt y. This negative half voltage forward biases the diode  $D_3$  & current flows through  $R_L$ . Then it forward biases the diode  $D_4$ . Thus in negative cycle,  $D_4$  &  $D_3$  are 13 conducted.

Conducted.



Since the rectified output is obtained for both positive & negative half cycles by an alternate diodes, it is called an Bridge-Type Full Wave rectifier.

Rectifier parameters:-

$$I_{DC} = DC \text{ current } I_{DC} = \frac{2I_m}{\pi} \quad I_m = \frac{V_m}{R_s + R_f + R_L}$$

$$DC \text{ voltage } V_{DC} = \frac{2V_m}{\pi}$$

$$Rms \text{ value of Current } I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$Rms \text{ value of Voltage } V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$\eta = \frac{P_{DC}}{P_{AC}} = 81\%$$

$$\epsilon_f = 40.8\%$$

## Problems on rectifiers

1. The input of a half wave rectifier is  $200 \sin \omega t$ . If  $R_L = 1k\Omega$  & forward resistance of the diode is  $50\Omega$ . Find DC current, DC voltage, rms value of current & voltage & Efficiency.

Soln:  $V_i = V_m \sin \omega t$   
 $= 200 \sin \omega t$

$$V_m = 200V \quad \omega = 50 \text{ rad/sec}$$

$$\text{DC Current } I_{DC} = \frac{I_m}{\pi} \quad I_m = \frac{V_m}{R_s + R_f + R_L} = \frac{V_m}{R_f + R_L}$$

$$I_{DC} = \frac{0.19}{\pi} = \frac{20}{50 + 1k\Omega} = \underline{\underline{0.19A}}$$

$$= \underline{\underline{60mA}}$$

$$\text{DC voltage } V_{DC} = \frac{V_m}{\pi} = \frac{200}{\pi} = \underline{\underline{60V}}$$

$$I_{rms} = \frac{I_m}{\alpha} = \frac{0.19}{2} = \underline{\underline{0.095mA}}$$

$$V_{rms} = \frac{V_m}{2} = \frac{200}{2} = \underline{\underline{100V}}$$

$$\eta = \frac{P_{DC}}{P_{AC}}$$

# Clippers & Clampers

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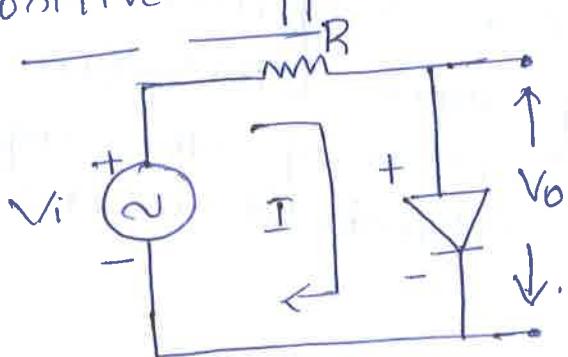
## Clipper:

A circuit which cut-off the voltage above or below at specific level is called an clipper circuit.

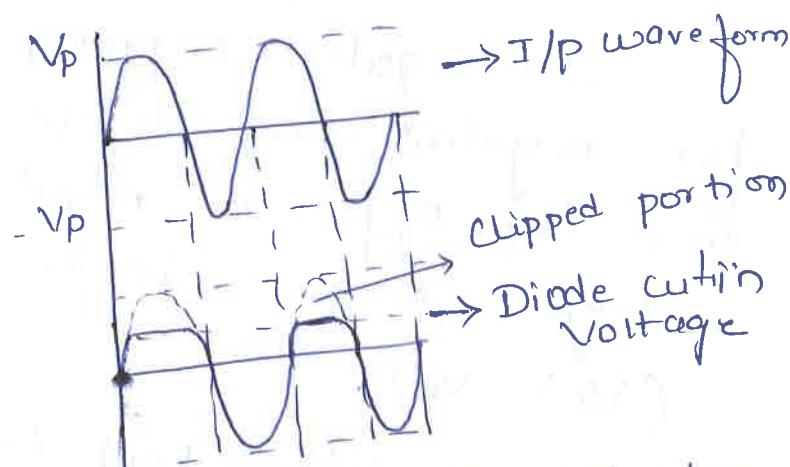
A clipper circuit which removes a portion of positive cycle of the input signal is called as an positive clipper.

A clipper circuit which removes a portion of negative half cycle of the input signal is called as negative clipper.

## positive Clipper:-



$$V_o \approx V_f$$



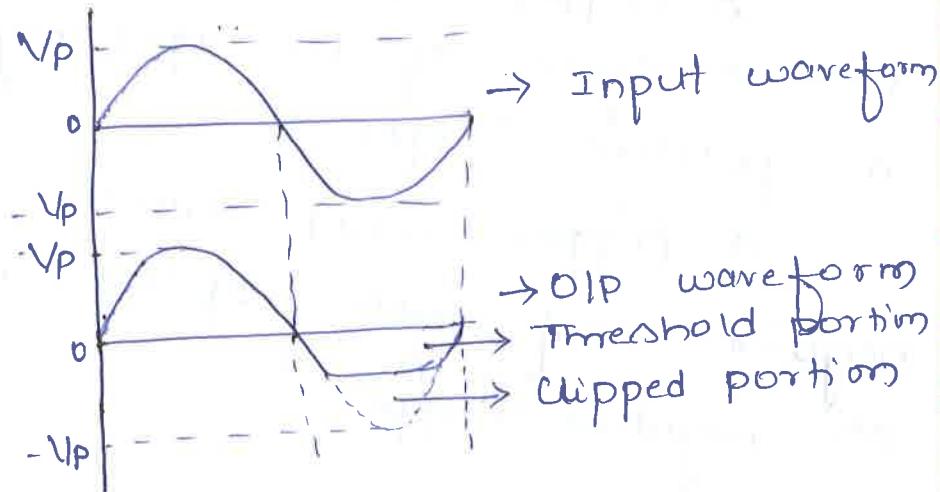
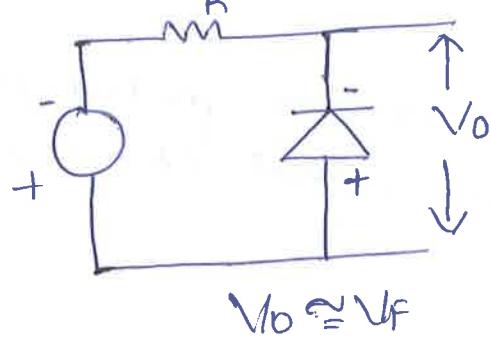
In positive clipper, diode is forward biased for positive half cycle signal. In forward biased condition diode starts its conduction when  $V_i \geq V_t$ .  $V_t$  is threshold voltage.

When  $V_i \geq V_t$  ( $0.7\text{-Si}, 0.3\text{-Ge}$ ) diode holds the constant voltage across it until the sinusoidal waveform falls below the threshold point. Thus above threshold voltage diode will cut-off the signal.

Thus output voltage won't exceed the threshold point.

In negative half cycle, diode is reverse biased & hence no effect on negative half cycle. The OLP is as it is.

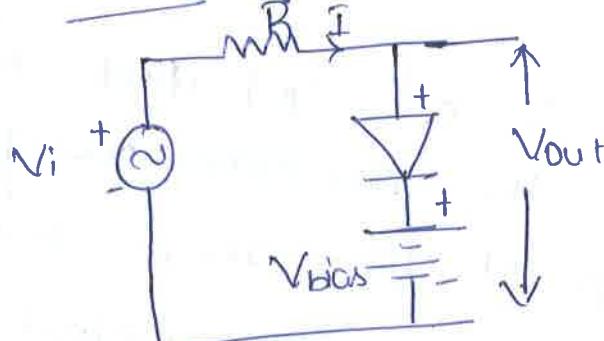
### Negative Clipping:



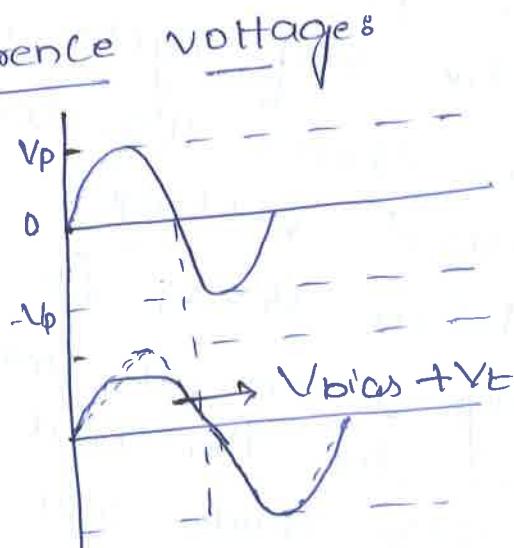
In negative clipping, diode is forward biased for negative half cycle of input. This circuit will clip off the negative portion of the input voltage which is below the threshold voltage ( $V_i > -V_t$ ).

For positive half cycle diode is reverse biased. & hence no effect of positive voltage in the circuit.

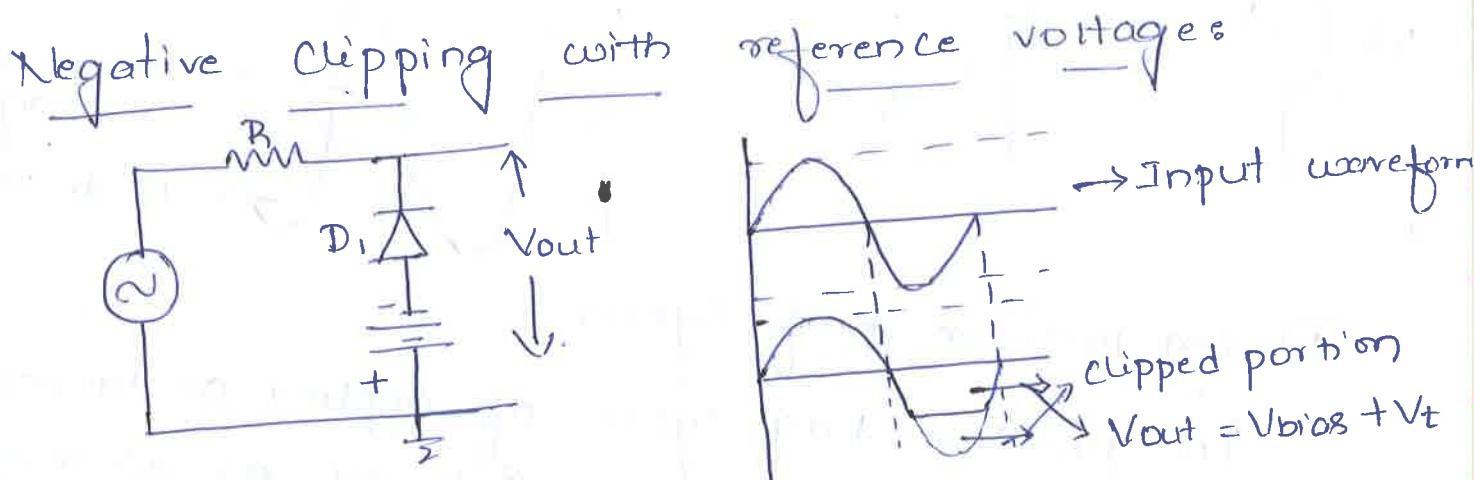
### positive clipping with reference voltage:



$$V_{out} = V_{bias} + V_t$$



To produce diode Clipping Circuit for applied input voltage ( $V_i$ ), a biasing voltage added in series with a diode to produce a combination clipper output.



$$V_{out} = -V_{bias} - V_t = -(V_{bias} + V_t)$$

In this clipping circuit, diode is forward biased by a negative half cycle. Now negative half cycle of the input signal is clipped off when  $V_i > V_{bias} + V_t$ .

### Clammer Circuits:-

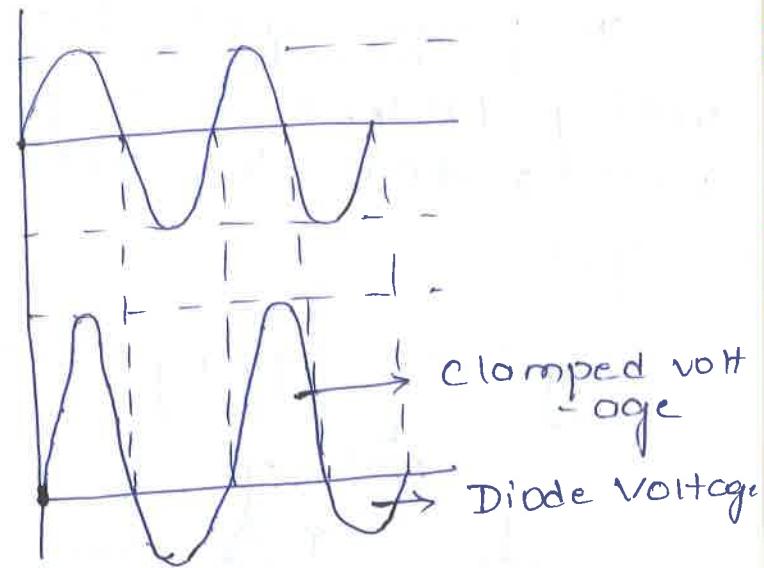
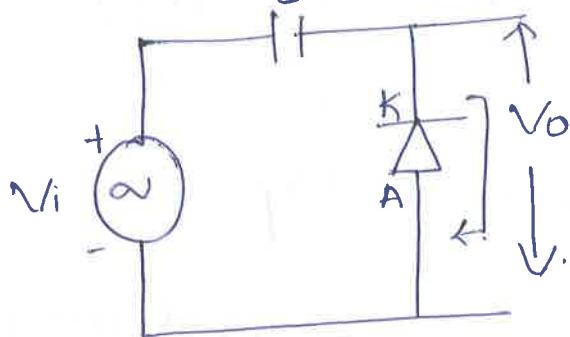
It is an electronic circuit that changes the DC level to the desired level without changing the shape of the applied signal.

The construction of clammer circuit is similar to clipper circuit, the only difference is a capacitor is connected in series with a diode instead of resistance. This capacitor provide a dc offset from the stored charge.

The clamping circuit's are of three types:

1. positive clammer & negative clammer
2. Biased clammer.

positive clumper:



During positive half cycles-

In positive half cycle of applied ac i/p voltage, the diode is reverse biased & it act as an open switch, hence no current flow through it. So the signal appears at the output with the doubled value of the i/p applied. ie. When diode is non-conducting state of the capacitor is get charged to peak value initially, later it is get discharged.

Therefore, the output voltage is equal to sum of voltage stored in capacitor ( $V_C$ ) & the input voltage ( $V_i$ ).

$$V_o = V_C + V_i \quad \text{--- (1)}$$

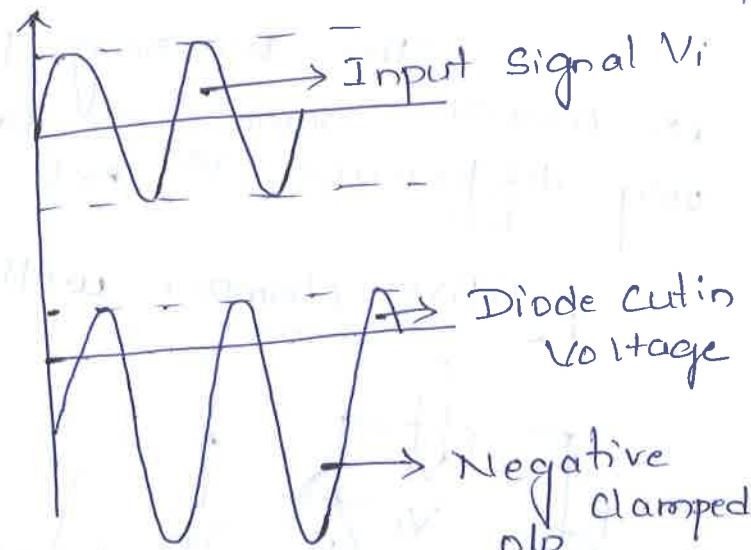
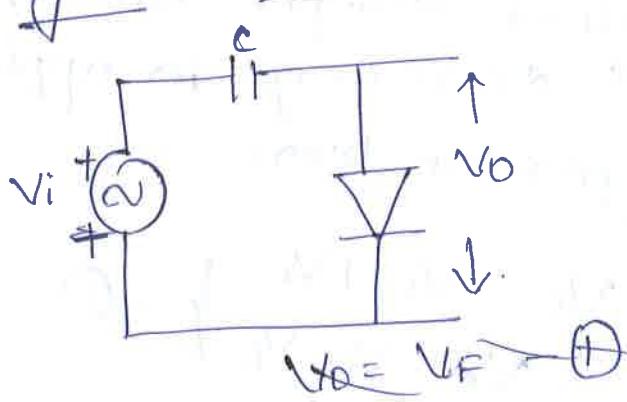
In positive half cycle, the capacitor get charged to peak value of input ( $V_i$ ). At maximum value of  $V_i$ :  $V_o = V_m + V_m = 2V_m$ . --- (2)

For example if input applied is  $\frac{1}{2}V_{p-p}$ , in positive half cycle it is 6v & negative half cycle it is -6v

During negative half cycles

During negative half cycle of the i/p. diode is forward biased & it allows current to pass through it. This negative half cycle charges the capacitor to  $-V_m$ .  $V_o = V_F - \textcircled{3}$

(ii) Negative clamps:-



During positive half cycles

In positive half cycle, the diode is forward biased & hence current flows through it. This charges the capacitor to peak value of  $V_i$  in reverse polarity ( $-V_m$ ). As the  $V_i$  decreasing after reaching maxi. value of  $V_i$ , the capacitor holds the charge until the diode remains forward biased.  $V_o = V_F - \textcircled{1}$

During negative half cycles

In negative half cycle, the diode is reverse biased & it won't allow current to pass through it. In non conducting state diode in acts as an open switch, as a result capacitor starts its discharge.

Then output voltage is equal to :

$$V_o = V_c + V_i$$

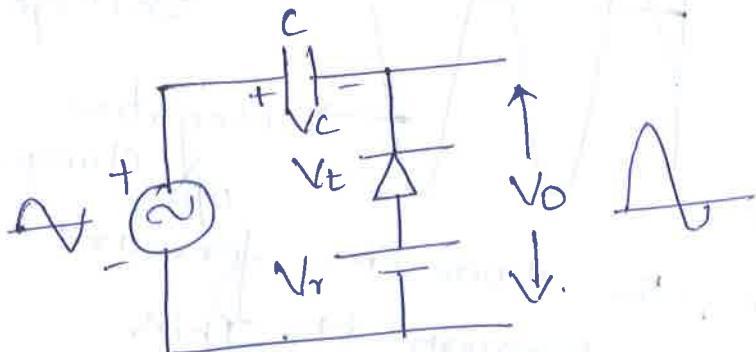
$$= -V_m - V_m$$

$$\underline{V_o = -2V_m}$$

### (III) Biased Clamper:-

The working principle of biased clamper is almost same as unbiased clamper but the only difference is external dc voltage is applied.

positive clamper with positive bias:



$$V_o = V_r + V_i \quad \text{---} \quad ①$$

$$V_r = V_o - V_i$$

In positive half cycles, the positive reference forward biases the diode, when:

$$V_i < V_r \quad ②$$

allows the current to pass through it.

Then diode allows the current to pass through it. When the input voltage ( $V_i$ ) exceeds the reference voltage, diode get reverse bias & it stops allowing current to pass through it.

In negative half cycle, the reference voltage reverse biases the diode when.

$$V_i < V_r$$

As a result, the output voltage is almost

as input voltage

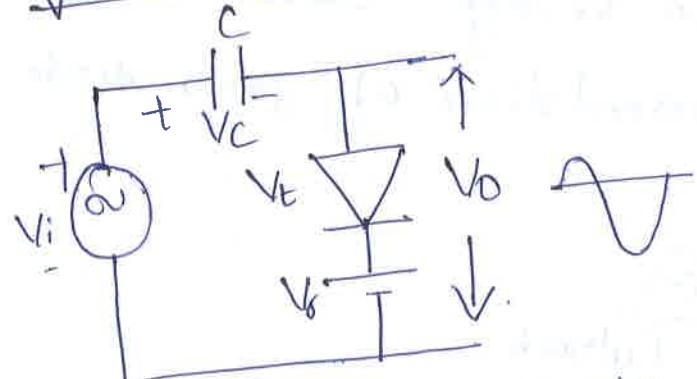
$$V_o \approx V_i$$

~~When the supply ( $V_o$ ) reference voltage exceed input voltage ( $V_i > V_r$ ) then diode is forward biased.~~

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In positive half cycle, the diode is forward biased by both reference voltage ( $V_r$ ) & input voltage ( $V_i$ ). As a result capacitor get charge to maximum peak value.

Negative Clamper with positive bias



$$\begin{aligned} V_o + V_r + V_t &= 0 \\ V_r &= -(V_o + V_t) \end{aligned} \quad \text{①}$$

In positive half cycle, the reference voltage ( $V_r$ ) reverse biases the diode when reference voltage ( $V_r$ ) is less than reference voltage ( $V_i$ ).

When input voltage ( $V_i$ ) exceeds the reference voltage ( $V_r$ ) then diode is forward biased & hence current flows through it, as a result it charges the capacitor to maximum peak value.

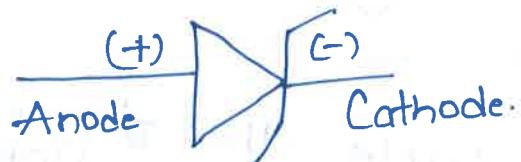
In negative half cycle, the diode is reverse biased & capacitor is get discharge.

## Zener diode:

A Zener diode is a special kind of diode, the working of Zener diode in a forward biasing condition is same as normal diode, but in reverse regular PN junction diode acts as an open switch i.e. it is reverse biased. ~~where~~ <sup>but</sup> Zener diode also work in reverse bias condition.

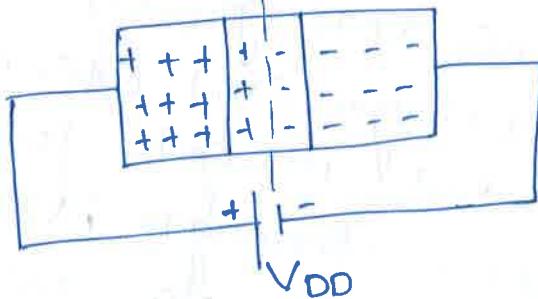
In reverse bias, Zener current allows the current to pass through it when the value of reverse voltage is above the breakdown voltage called as Zener voltage.

The symbolic representation of Zener diode is as shown in figure:



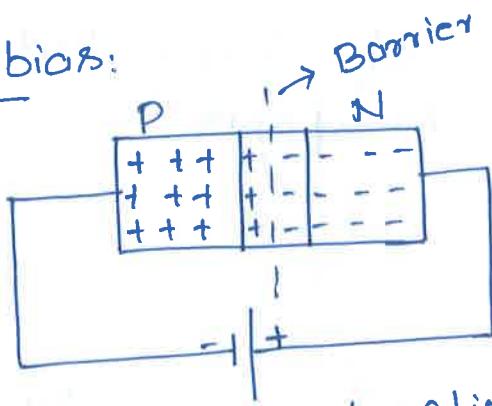
## Working principle:

### i) Forward bias:



As in normal pn junction diode, if Zener diode is forward biased, if external voltage becomes greater than the barrier ( $\approx 0.7$  or  $\approx 0.3$ ) current will start to flow. Because when the positive voltage repels the holes towards the junction & combines with the electrons being repelled in opposite direction towards the junction.

### ii) Reverse bias:



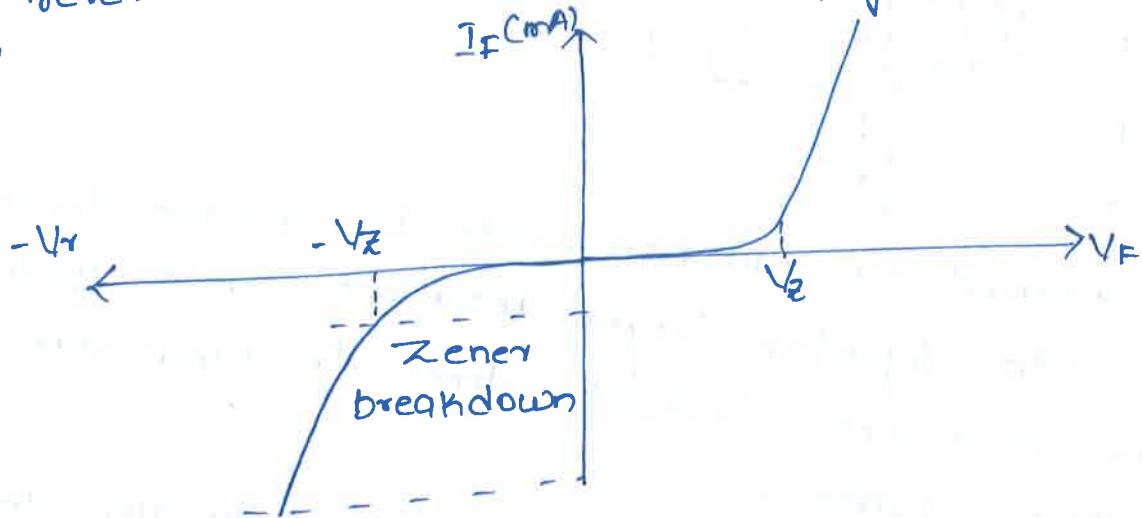
When a normal pn junction diode is reverse biased, the width of the depletion layer becomes more wider. At same time, a reverse current starts to flow due to minority charge carriers.

After certain reverse voltage across the junction, the minority charge carriers get sufficient energy to cross the barrier. As a result it combines with stationary carrier in depletion layer. This recombination knock out more free electrons, these free electrons causes breakdown, which damages the diode called as Avalanche breakdown.

In Zener diode, the pn junction is highly doped by higher concentrated impurity ions. Due to this for a applied reverse voltage, the width of the depletion regions becomes more thinner than the width of the normal diode.

As the width of the depletion layer becomes more thin then the voltage across it quite high. If the reverse voltage is increased continuously, then the electrons come out of the impurity ions & make the depletion layer to conduct. Then breakdown is known as Zener breakdown. Thus Zener diode will conduct in reverse voltage also.

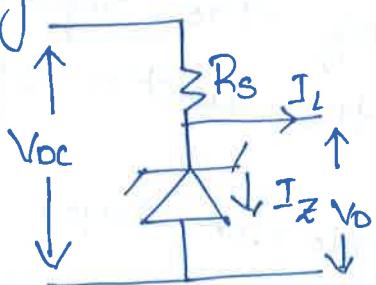
The V-I characteristic of Zener diode in forward & reverse bias is shown in figure



### Zener diode Regulator:

When a Zener diode is connected across a voltage source, the voltage across a Zener diode remains constant & current through Zener diode will keep on increasing with respect to voltage source. Thus Zener diode is mainly used a voltage regulator to regulate the variation of voltage.

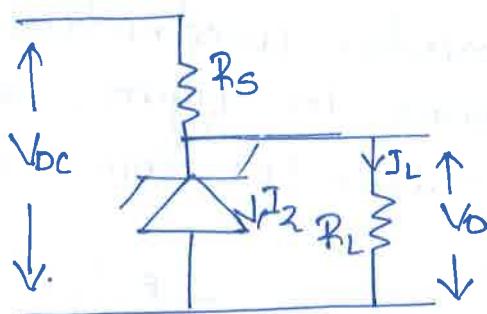
### Line Regulation:



The resistor  $R_s$  which is connected in series with Zener limits the flow of current through the diode. The stabilised output voltage  $V_o$  is measured across the diode.

When all the current flows through the diode which in turn dissipates the maximum power in it. As the value of  $R_s$  increases the dissipation of power in the diode also gets increases.

case 2: load Regulation:

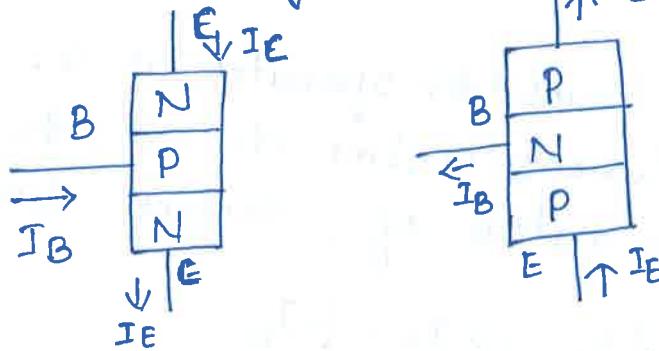


When a load ( $R_L$ ) is connected in parallel across zener, so that voltage across zener is same as voltage across  $R_L$  i.e.  $V_L = V_z$ . This load effectively stabilizes the voltage across zener ( $V_z$ ).

### BIPOLAR JUNCTION TRANSISTOR:

A bipolar junction is a terminal device consisting of two pn junctions to amplify the signal. The three terminals are: Emitter (E), Base (B) & Collector (C). These terminals are formed by sandwiching of either p-type (or) n-type semiconductor between a two p+ (or) n+ substrate. Based on this BJT is of two types: NPN & PNP.

The schematic representation of NPN & PNP BJT is as shown in the figure:

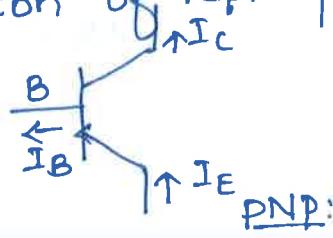
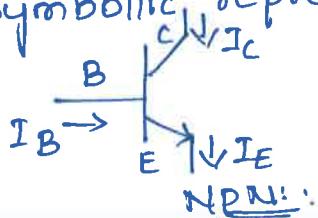


$I_E$  - Emitter Current

$I_C$  - Collector Current

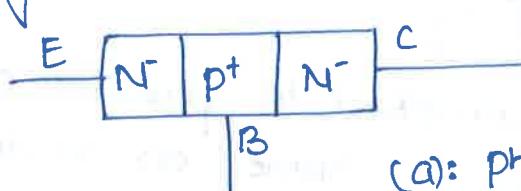
$I_B$  - Base Current

The symbolic representation of NPN & PNP BJT is as:

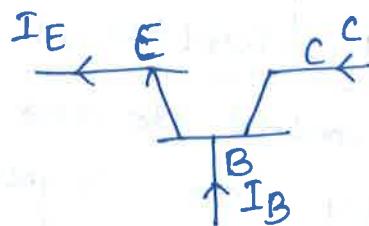
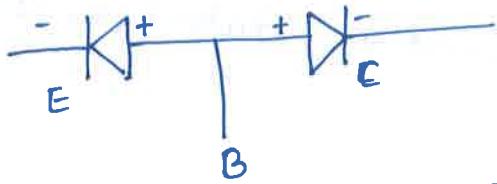


## Construction & working principle of BJT:

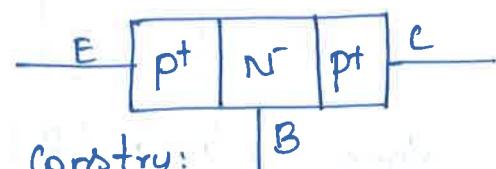
The bipolar transistor construction consists of two PN junction diodes as shown in figure, which gives three connecting terminals: Emitter (E), Collector (C) & Base (B).



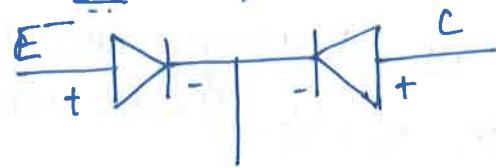
(a): physical



(b): Two-diode Analogy



Constru:



B

(c): Circuit Symbols:

Transistor is also semiconductor device, it can act as insulator (or) conductor. The change of state between these two states insulator (or) conductor enables transistor to perform two basic functions: switch (or) Amplifier.

Then BJT have the ability to operate within three different regions:

1. Active region : the transistor operates as an amplifier. Since BJT is a Current Control device, the amplification factor ( $\beta$ ) is the ratio of output current & input current i.e.  $\beta = \frac{I_C}{I_B} \Rightarrow I_C = \underline{\underline{\beta I_B}}$

g. Saturating region - <sup>transistor</sup> the transistor operates as an switch.

Thus  $I_C = \underline{I}_{\text{saturation}}$ .

3. Cutt-off: the transistor is fully OFF & operating as a switch i.e.  $\underline{I}_C = 0$ .

Relationship b/w  $\alpha$  &  $\beta$ :

$$\beta = \frac{I_C}{I_B} \quad \alpha = \frac{I_C}{I_E} \quad - \textcircled{2}$$

$$I_E = I_B + I_C$$

$$I_E = \frac{\beta}{\alpha} I_B + I_B$$

$$I_B = I_E - I_C \quad \text{from (2)} \quad I_C = \alpha I_E$$

$$I_B = I_E - \alpha I_E$$

$$I_B = I_E (1 - \alpha) \quad \text{from (1)} \quad \beta = \frac{I_C}{I_B}$$

$$\therefore \beta = \frac{\alpha I_E}{I_E (1 - \alpha)}$$

$$\beta = \frac{\alpha}{1 - \alpha} \rightarrow \text{Quality Efficiency factor.}$$

$$I_E = I_B + I_C$$

$$\frac{I_C}{\alpha} = \frac{I_C}{\beta} + I_C$$

$$\frac{I_C}{\alpha} = I_C \left( \frac{1}{\beta} + 1 \right)$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\frac{1}{\alpha} = \frac{1 + \beta}{\beta}$$

$$\alpha = \frac{\beta}{1 + \beta}$$

## BJT Voltages:

$$V_{BE} > 0.7V \text{ & } V_{CB} > V_{BE}$$

## DC bias Conditions:

$$V_{BE} = V_B - V_E$$

$$V_E = I_E R_E$$

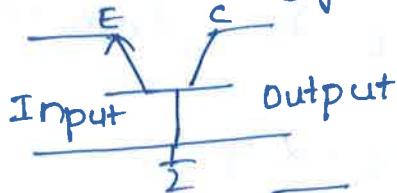
$$V_{CE} = V_C - V_E$$

$$V_C = I_C R_C$$

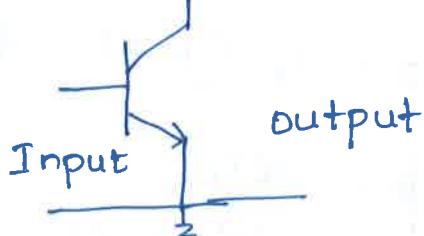
## BJT Configuration:

As the bipolar ~~transistor~~ configuration is a three terminal device, hence there are three possible ways to connect within an electronic circuit with one terminal being common to both input and output. The three possible configurations are:

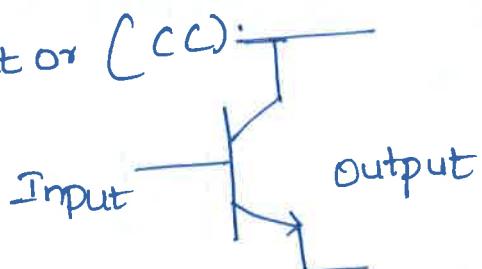
### 1. Common Base (CB):



### 2. Common Emitter (CE):



### 3. Common Collector (CC):



## Common base Characteristics:

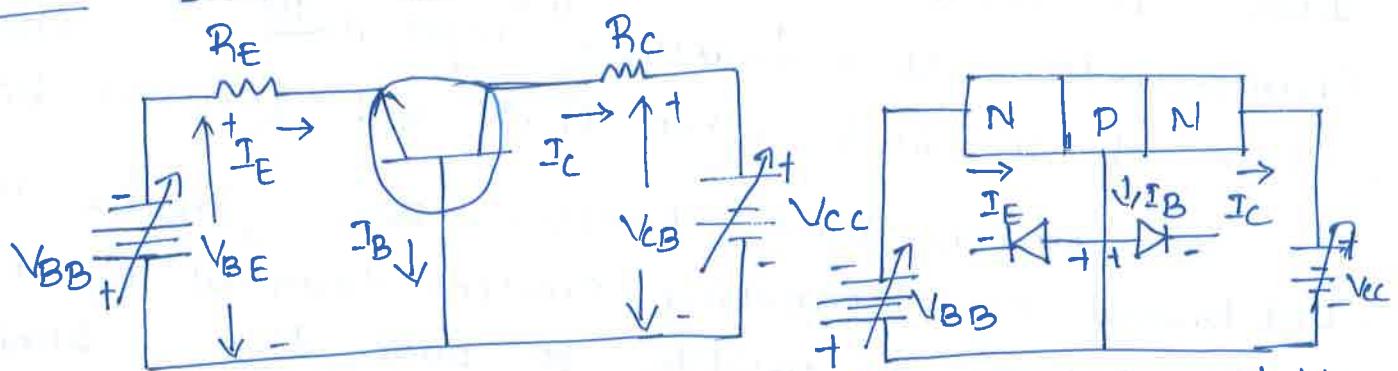


figure: a) Circuit Configuration: b) Symbolic representation:

The Common base terminology derived from the fact that the base terminal is common for both input & output in the circuit. Thus base terminal is connected to ground potential.

In this configuration <sup>input</sup> is applied b/n emitter & base junction, which is named as ( $V_{BE}$ ) & output is measured collector & base junction, which is named as ( $V_{CB}$ ).

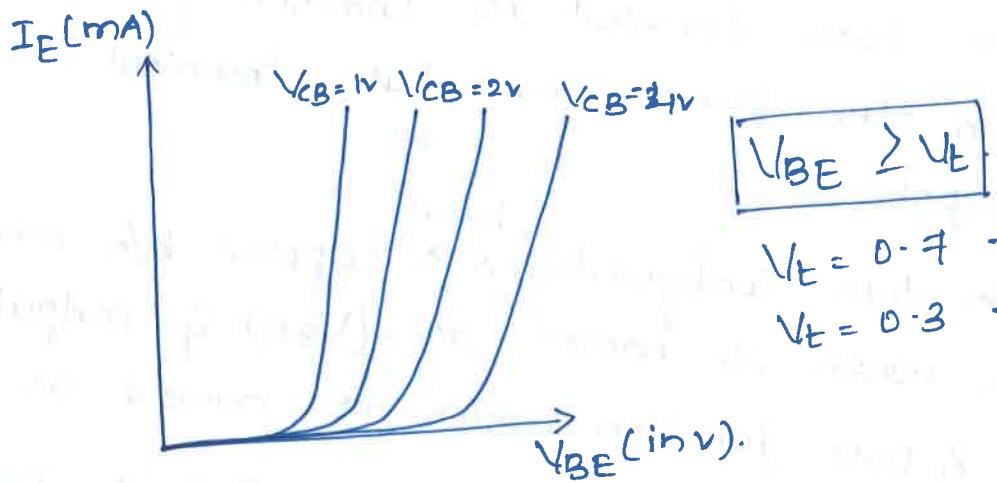
After biasing the currents in BJT ( $I_E$ ,  $I_B$  &  $I_C$ ) are due to the flow of holes, called as conventional current.

To understand the complete electrical characteristics of common-base, it is necessary to know the interrelations between b/n currents ( $I_E$ ,  $I_B$  &  $I_C$ ) & voltages ( $V_{BE}$  &  $V_{CB}$ ). Thus the input characteristics of a transistor classified into: input characteristics & output characteristics.

The input characteristics of a transistor is obtained by plotting V-I characteristics curve for input current ( $I_E$ ) & voltage  $V_{BE}$ . by keeping output voltage ( $V_{CB}$ ) constant at different levels.

Since a BJT is obtained by connecting two PN junction diodes as shown in the figure (b), thus the Input characteristics of a transistor <sup>replicates</sup> the V-I Characteristics of a diode when it is get forward biased.

In Common-base, Emitter - Base junction is forward biased by connecting emitter terminal to negative of the battery & positive to base terminal. Similarly Collector - base junction is reverse biased by connecting Collector to positive of battery & base to negative of supply.



$$V_{BE} \geq V_T$$

$$V_T = 0.7 \text{ for Si}$$

$$V_T = 0.3 \text{ for Ge.}$$

Analysis: Since base is connected at ground potential  $V_B = 0$ . The D.C biasing conditions of CB Configurations are:

$$V_{BE} = V_{EB} = V_E - V_B = V_E - 0 \quad \text{--- (1)}$$

$$V_{EB} = V_E$$

According to Ohm's Law  $\Rightarrow V_E = I_E R_E$

$$\therefore V_{EB} = V_E = I_E R_E \quad \text{--- (2) (or)} \quad I_E = \frac{V_E}{R_E}$$

According to equation (2), if  $V_{EB}$  is kept constant at certain values it increases the value of  $I_E$ .

$$\text{Similarly } V_{CB} = V_C - V_B = V_C - 0 \quad \text{--- (3)}$$

$$V_{CB} = V_C$$

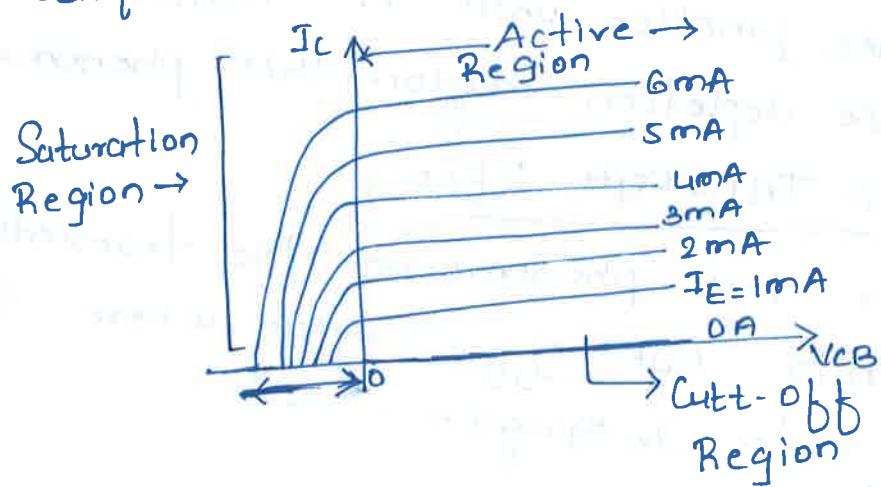
$$\text{But } V_C = I_C R_C \Rightarrow I_C = \frac{V_C}{R_C} \\ \therefore I_C = \frac{V_{CB}}{R_C}$$

$$\text{Also } d = \frac{I_C}{I_E} \text{ & } I_E = I_B + I_C - (5)$$

$$\text{If } I_B = 0, \text{ then } I_E = I_C - (6)$$

According to equation (2), (4) & (6), if  $V_{CB}$  is kept constant at certain values the value of  $I_E$  is also get effected.

The output characteristics of a CB is obtained by plotting Output Current ( $I_C$ ) & output voltage ( $V_{CB}$ ).



The output characteristics of CB defines three region of operation: Active, Saturation & Cut-off.

Active region: In this region Emitter-Base junction is forward biased & Collector-Base junction is reverse biased. & in this region Collector current is approximately equal to emitter current as given in equation (6).

$$I_C \approx I_E$$

Thus transistor operates like an amplifier.

Saturation region: In this region, the collector current ( $I_c$ ) increases exponentially as  $V_{CB}$  increases towards '0'. Further increase in  $V_{CB}$  makes transistor to enter active region. Where  $I_c$  is almost independent of  $V_{CB}$  & transistor can be set to work as Constant Current Source.

The increase of reverse bias voltage increases the depletion region width between collector & base region. As a result the electrical width of the base region is reduced. This effect is known as Early effect (or)

### Base width modulation:

If  $V_{CB}$  is increased even after early effect, the width of the depletion region touches (or) it penetrates into Emitter-base junction until it makes contact with Emitter-base depletion region. This phenomenon is known as Punch-through Effect:

After this phenomenon the transistor will enter again into Cut-off region where transistor will be in OFF - State. In this region :

$$V_{BE} < V_t$$

### Summary:

\* From input characteristics, it is cleared that the input  $I_E$  increases rapidly with a small increases in input voltage  $V_{EB}$  by keeping  $V_{CB}$  constant. This indicates that input resistance of common base configuration is very small & it is given by :  $r_i = \frac{\Delta V_{EB}}{\Delta I_E} \mid V_{CB} = \text{const.}$

This resistance is known as dynamic input resistance of transistor in CB Configuration.

\* From output characteristics, it is cleared that after generation of collector ( $I_C$ ) from reverse bias voltage ( $V_{CB}$ ),  $I_C$  will become independent of  $V_{CB}$  in active region. Thus it gives high output dynamic resistance.

It is given by:

$$R_D = \frac{\Delta V_{CB}}{\Delta I_C} \quad |_{I_E = \text{Constant}}$$

\* Current gain  $\alpha = \frac{I_C}{I_E}$  Since  $I_C = I_E$

$$\underline{\underline{\alpha = 1}}$$

\* Voltage gain  $A_v = \frac{V_o}{V_i} = \frac{V_{CB}}{V_{EB}} = \frac{V_C}{V_E} = \frac{I_C R_C}{I_E R_E}$

$$\text{When } I_C = I_E \Rightarrow A_v = \frac{R_C}{R_E}$$

Thus it is used as

### CURRENT AMPLIFIER:

#### Common Emitter Configuration:

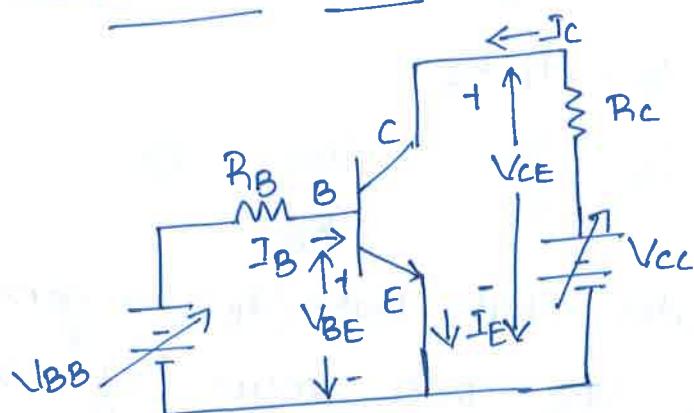
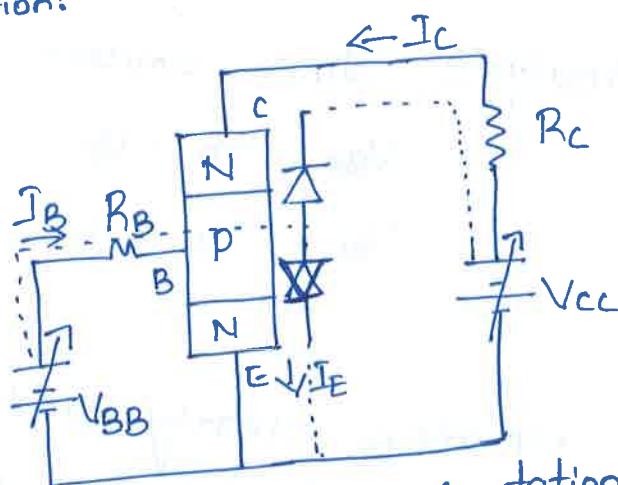


fig a): Circuit diagram

The terminology Common - emitter is derived from the fact that the input emitter terminal is common for input & output in the circuit. Thus emitter terminal is



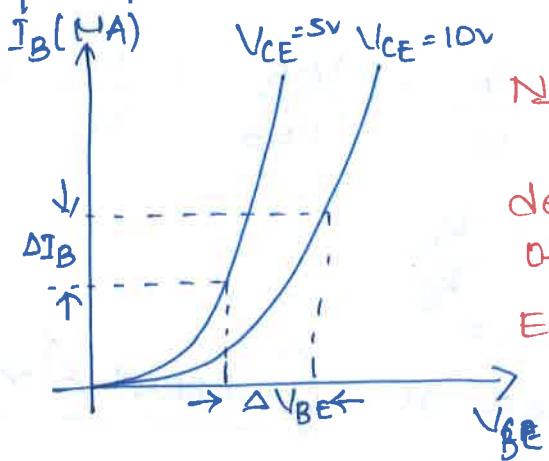
b): Symbolic representation:

Common - emitter is derived from

Connected to ground potential.

In Common-Emitter Configuration, Base-Emitter junction is forward biased by connecting base terminal to the positive of the supply which gives base current  $I_B$  and Collector-Emitter is reverse biased by connecting Collector terminal to positive of the supply & Emitter to negative terminals.

In Common-emitter Configuration, the input characteristics is obtained by plotting V-I characteristics of input voltage ( $V_{BE}$ ) & input current ( $I_B$ ) by keeping  $V_{CE}$  const.



Note:- As reverse bias  $V_{CE}$  increases voltage decreases the recombination of charge carriers in Emitter-base junction. Thus  $I_B$  is taken in mA.

Input Characteristics:

Analysis: Since emitter terminal is grounded  $V_E \approx 0$  &  $I_E \approx 0$ .

$$V_{BE} = V_B - V_E \quad I_B = I_B R_B$$

$$V_{BE} = V_B - ① \quad I_B = \frac{V_B}{R_B} = \frac{V_{BE}}{R_B} - ②$$

Equation clearly indicates that base ( $I_B$ ) is generated by increasing the value of  $V_{BE}$ . This value of  $V_{BE}$  is increased upto cutin-voltage of a transistor i.e.

$$V_{BE} \geq V_T \quad -③$$

$$\left. \begin{array}{l} V_T = 0.7V \text{ for Si} \\ V_T = 0.3V \text{ for Ge} \end{array} \right\}$$

$$V_{CE} = V_C - V_E$$

$$V_C = I_C R_C$$

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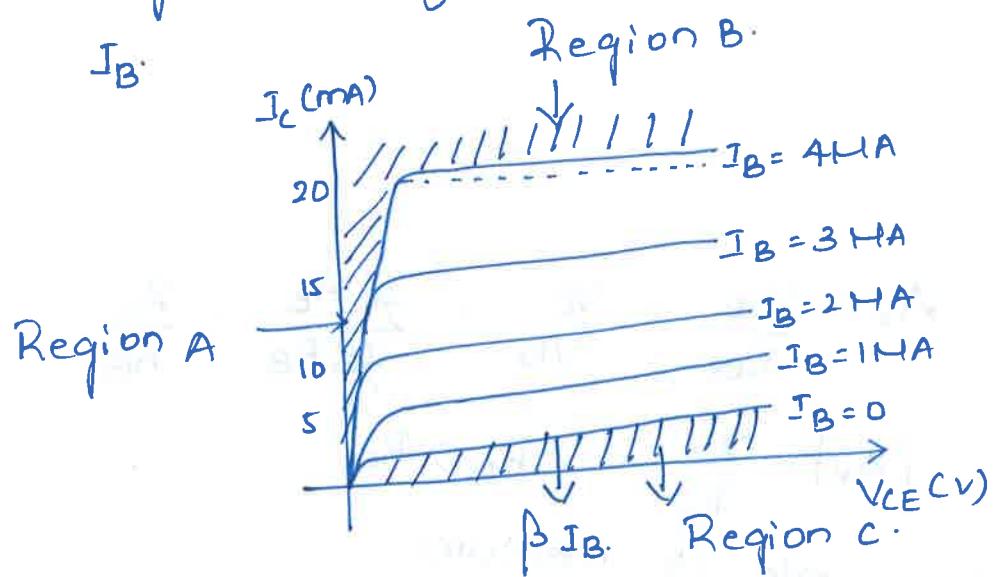
$$V_{CE} = V_C - \textcircled{4}$$

$$I_C = \frac{V_{CE}}{R_C} = \frac{V_C}{R_C} - \textcircled{5}$$

$$\text{Emitter Current } I_E = I_B + I_C$$

$$I_B = -I_C - \textcircled{6} \quad I_B \propto \frac{1}{I_C}$$

The output characteristics of CE is obtained by plotting collector current ( $I_C$ ) vs collector-emitter voltage ( $V_{CE}$ ) for different level of base current ( $I_B$ ).

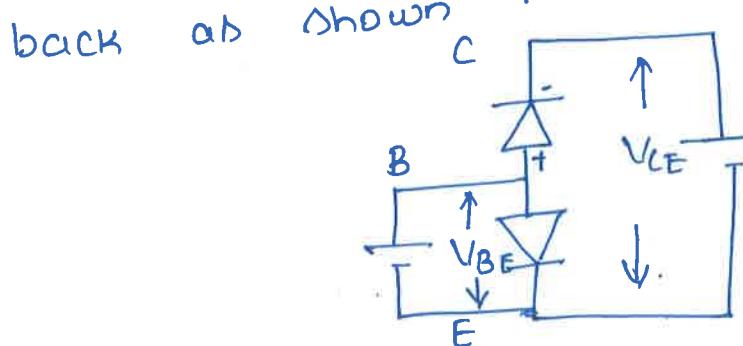


$$\beta = \frac{I_C}{I_B}$$

$$I_C = \beta I_B - \textcircled{7}$$

From eqn it shown that as  $I_C$  increases  $I_B$  decreases & collector current ( $I_C$ ) is increased by  $\beta$  times the value of fixed base current ( $I_B$ ). Thus output charac. is exactly straight (or) parallel to  $x$ -axis.

Region A: let consider a diode connected back to back as shown in the figure:



As  $V_{CE}$  increases both diodes are forward biased & makes the transistor works in cut saturation.

Region B: From the output characteristics of Common emitter, let take  $I_B = I_{MA}$  which  $I_C = 5mA$ . This indicates that output current  $I_C$  is amplified, thus transistor working as an amplifier. It indicates that transistor is in Active region.

Region c: In this  $V_{BE}$  is not increased upto cut-in voltage of transistor thus  $I_B \neq 0$ . If  $I_B \neq 0$  then  $I_C$  is also  $0$ . Hence transistor is in Cut-off region.

### Summary:

- \* Voltage gain  $A_v = \frac{V_{CE}}{V_{BE}} = \frac{V_C}{V_B} = \frac{I_C R_E}{I_B R_B} = -\frac{R_C}{R_B}$
- $|A_v| = \frac{R_C}{R_B} \quad R_B > R_C$
- Thus voltage gain is medium
- \* Since  $I_B = -I_C$  output is outp' of phase wrt input Current  $I_B$ .
- \* Current gain  $\beta = \frac{I_C}{I_B} = -1 \Rightarrow |\beta| = 11$ .

\*

# Common Collector Characteristics:

In Common Collector Configuration, Collector terminal is common for input & output. The circuit arrangement of CC configuration is shown.

Arrangement of CC Configuration

$R_E$

$V_{BB}$

$V_{BC}$

$I_B$

$V_{EC}$

$I_C$

$R_E$

$V_{EE}$

$I_E$

$V_{BC}$

$I_B$

$V_{EC}$

$I_C$

$R_E$

$V_{EE}$

$I_E$

$V_{BC}$

$I_B$

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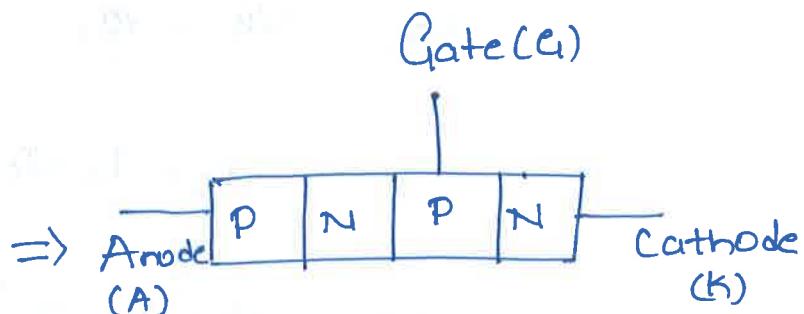
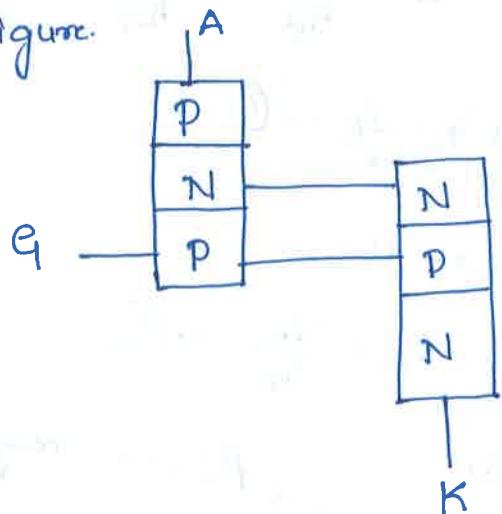
## Silicon Controlled Rectifier (SCR):

The Silicon Controlled Rectifier (SCR) is a three terminal Semiconductor switching device, which is used as a controlled switch to perform functions such as rectification, inversion & regulation of power flow like diode. SCR is a unidirectional device, but the SCR can be made to operate either as open Circuit switch (or) as a rectifying depend upon how its gate is triggered.

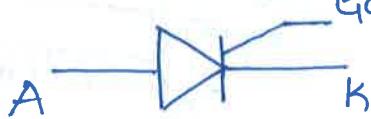
### Construction of SCR:

When a p-n junction is added to a junction transistor, the resulting three p-n junction device is called as Silicon Controlled Rectifier. It is as shown

in figure.



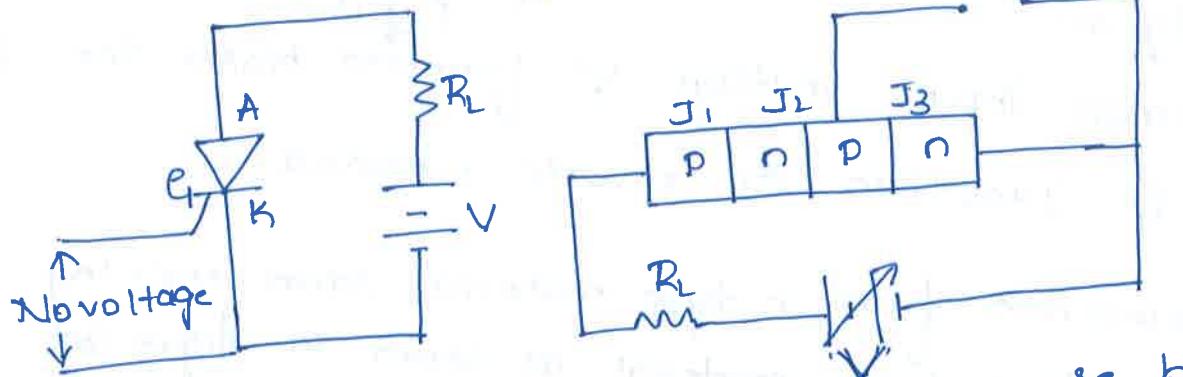
The three terminals are : Anode (A), Cathode (K) and Gate(G). The symbolic representation of SCR is :



## Working:

In normal operating Condition of SCR, anode is positive wrt Cathode & gate is small positive potential wrt Cathode.

### Case 1: When gate is open



\* Under this Condition junction  $J_2$  is reverse biased while Junction  $J_1$  &  $J_3$  are forward biased.

while Junction  $J_1$  &  $J_3$  works as a npn transistor

\* Hence the junctions  $J_1$  &  $J_3$  are forward biased with base (or) gate open.

\* Consequently, no current flows through  $R_L$  & SCR is in cut-off region.

\* If the applied voltage  $V$  is increased gradually, then the reverse biased junction will get break down. As a result SCR Conducts heavily & it said to be in ON state.

### Case 2: When gate is positive wrt Cathode:

The SCR can conduct heavily at smaller applied voltage by applying a small positive potential at the gate:

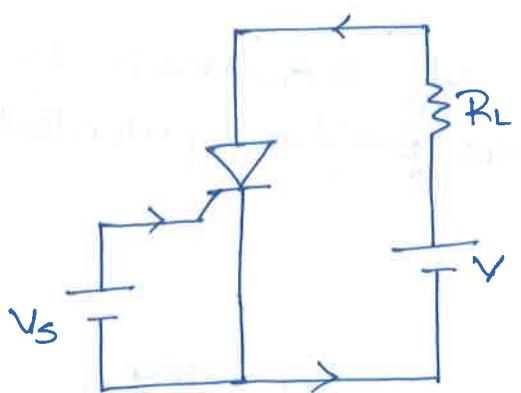
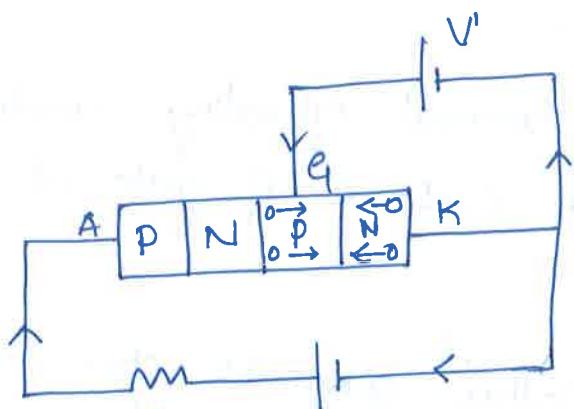


fig (a):



RL fig (b)

\* A small input voltage  $V'$  forward biases the junction

J3 & Junction is reverse biased.

\* The electrons from n-type material start moving across J3 towards p-type material as shown in figure (b).

\* Consequently the electrons from junction J3 are attracted across the junction J2 & gate current start to flow.

\* The increased current in turn makes more accumulation of more number of electrons in junction J2.

\* As a result, anode current also gets increases.

\* The small voltage  $V'$  breaks down the junction J2

& SCR conducts heavily, even if gate voltage is removed the gate anode current does not decrease.