POWER ON AND RESET AARDONYX

Power Rails:

1. **3.3V (VCCIO - IO voltage)**
2. **1.8V (VCC_CORE - core voltage)**

Aardonyx has 2 power rails. Nominally all the power rails are expected to ramp simultaneously. However, VCCIO must ramp first, to enable the external signals (like RESET#) to be applied to the on-chip logic. VCC_CORE voltage can ramp followed by VCCIO.

Clock Input:

Aardonyx will receive a nominal external system clock of 10-100MHz. The CLK will be provided by external XSTAL oscillator. The CLK signal should be valid before RESET is asserted. This CLK input is directly available to other logic modules by default.

RESET# signal:

During power up, the RESET# signal is held asserted (active low). RESET# is de-asserted ?? nS (or ?? CLKs) assertion, On RESET# de-assertion, additional Power-On Config pins are latched.

The following table have been referenced from RIMO power on & reset.

Power on and Reset sequencing:

Time	Event	Reset	Clock	Scan Enable
t0: 0ms	Insert Socket	Floating	Floating	Low/ Floating
t1: 800ms	3.3V stabilizes	Floating	Floating	Low/ Floating
	1.8V starts	Floating	Floating	Low/ Floating
t2: 810ms	1.8V stabilizes	Low	Active	Low/ Floating
t3: 820ms	-	High	Active	Low/ Floating