

IIT_MADRAS

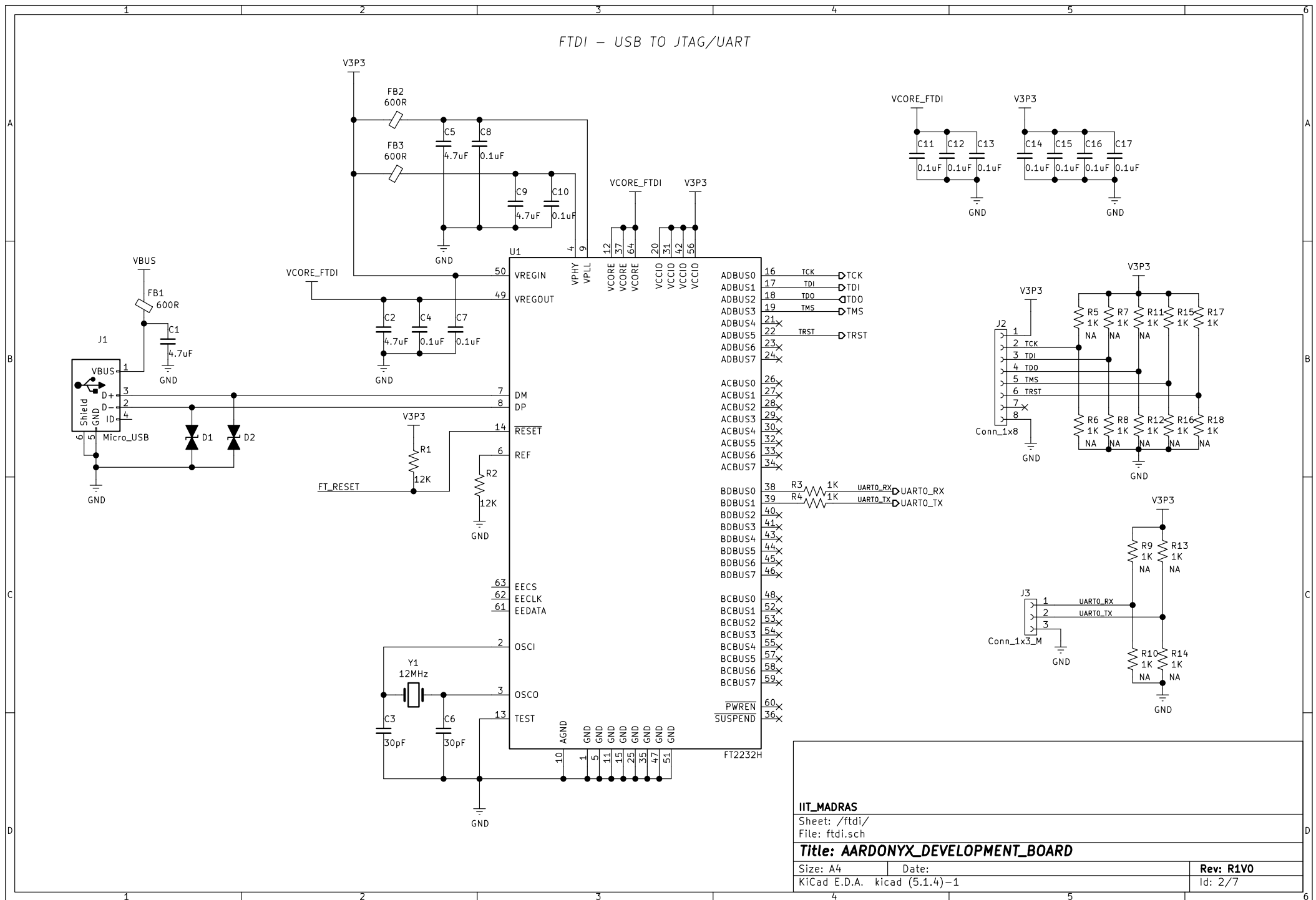
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File: Aardonyx.sch

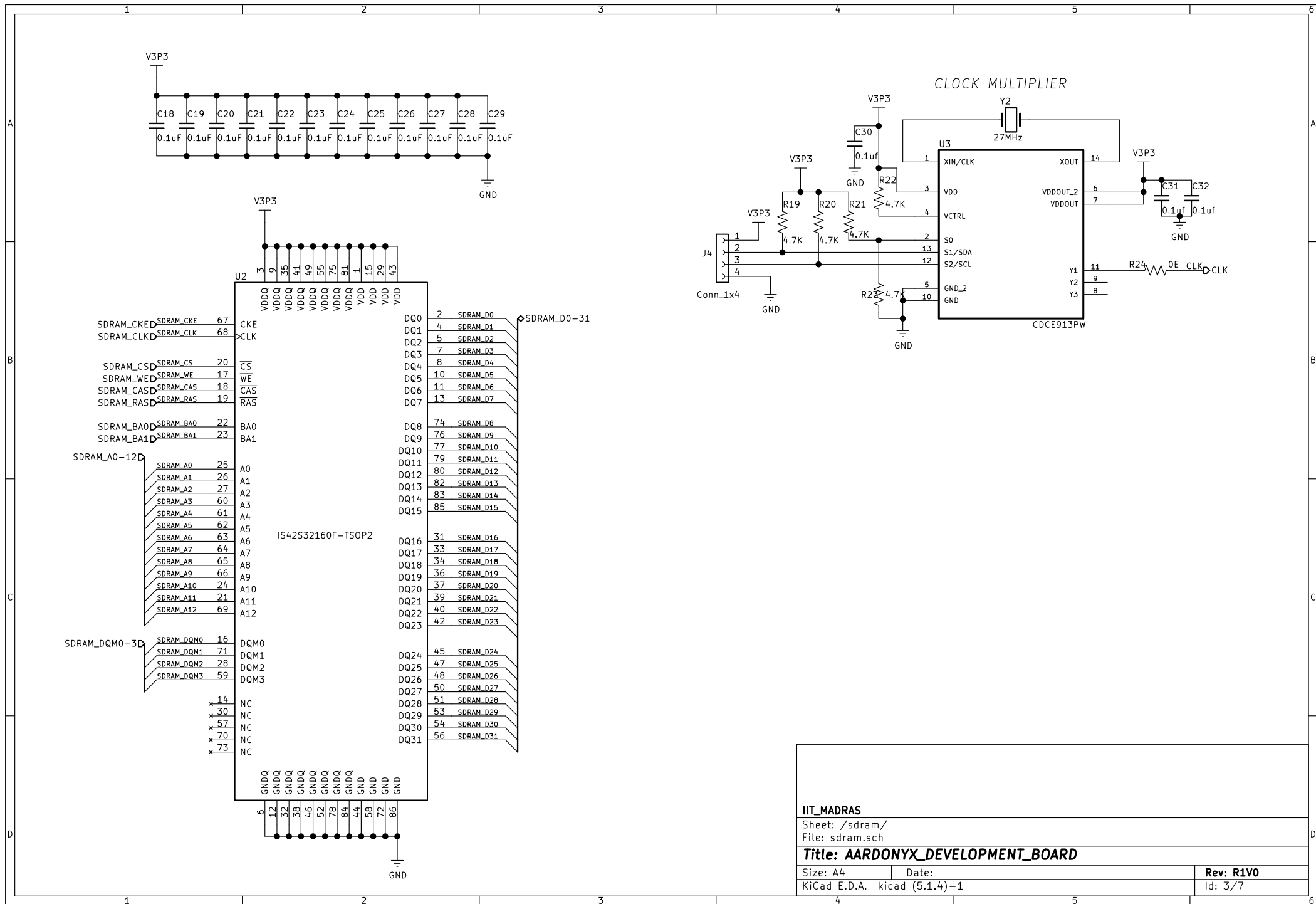
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Size: A4
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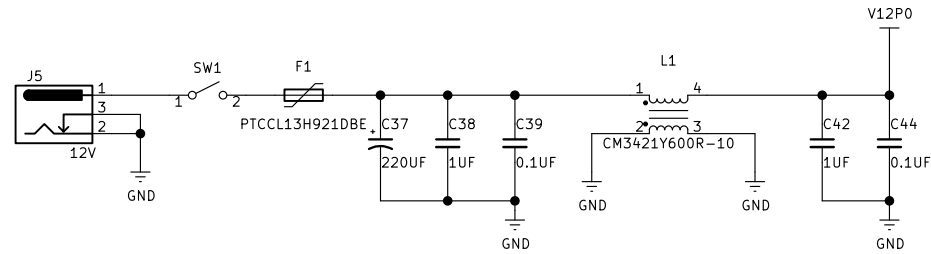
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Id: 1/7

Rev: R1V0

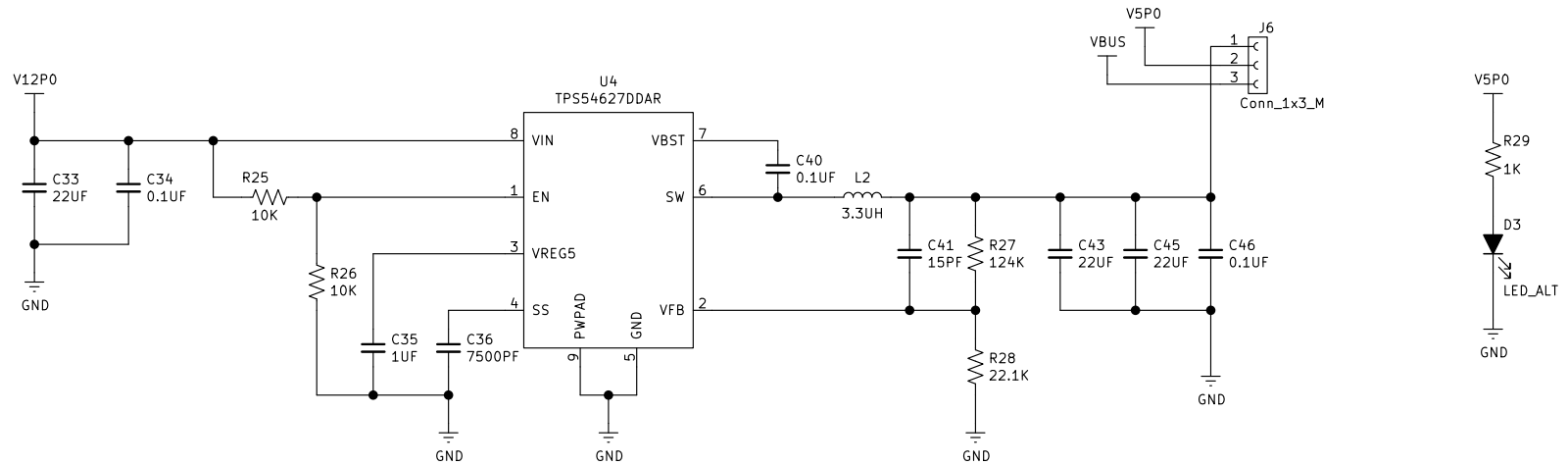




DC JACK POWER SUPPLY



SWITCHING REGULATOR FOR V5P0 POWER RAIL



IIT_MADRAS

Sheet: /power_1/
File: power_1.sch

Title: AARDONYX_DEVELOPMENT_BOARD

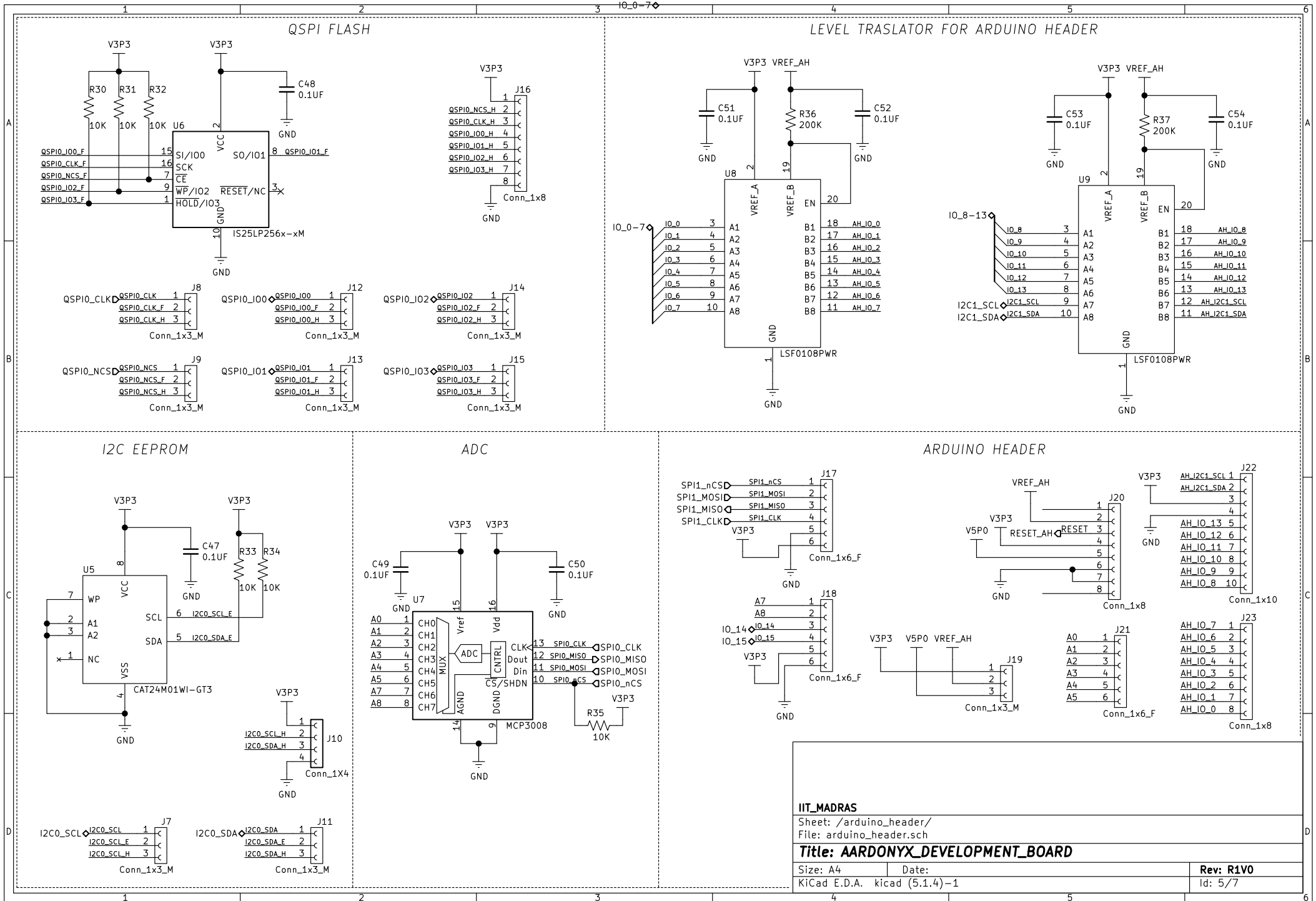
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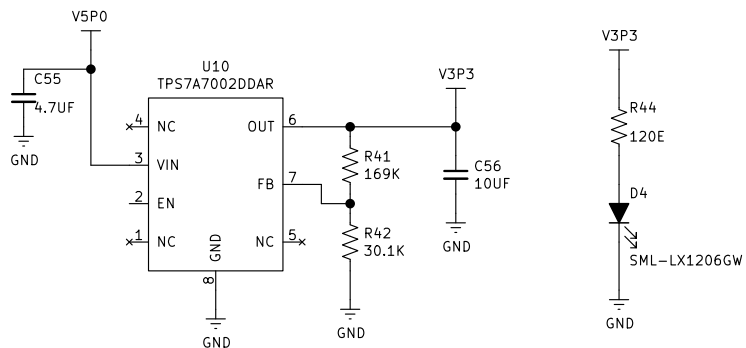
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Rev: R1V0

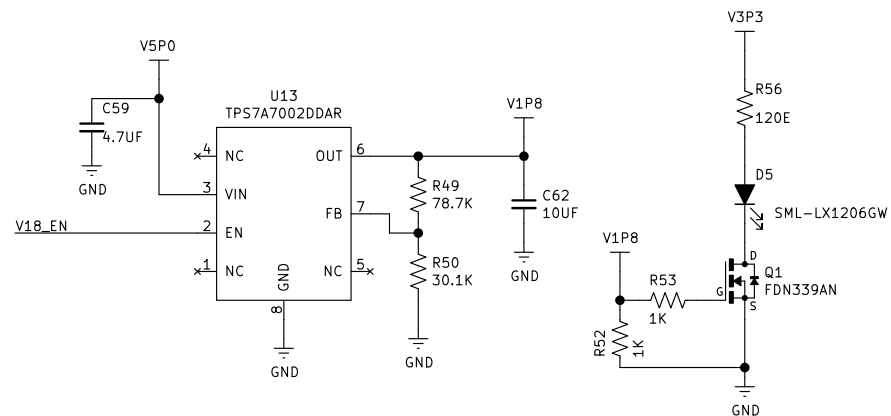
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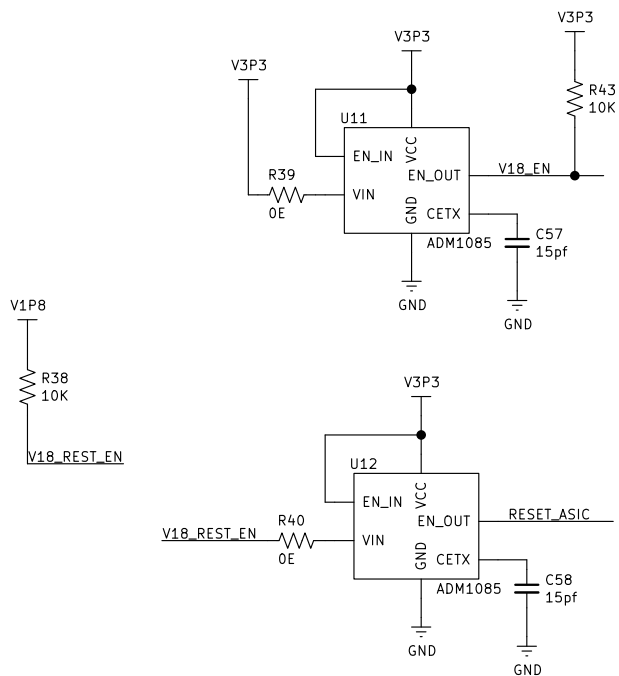
LDO FOR V3P3 POWER RAIL



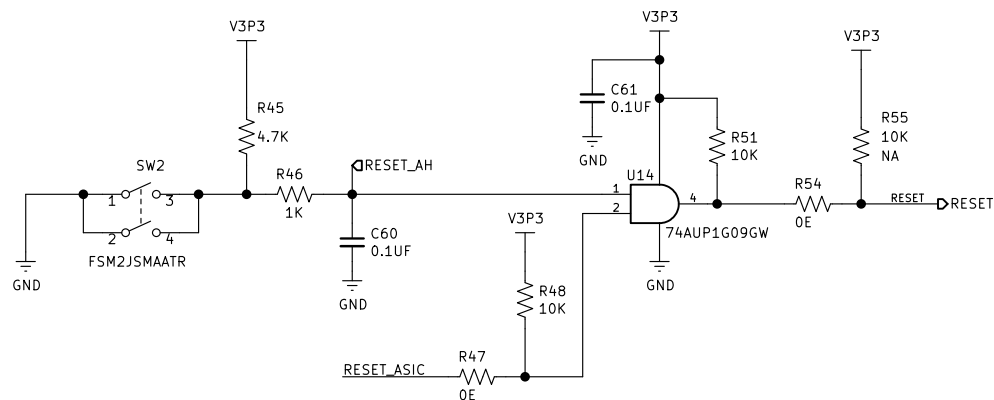
LDO FOR V1P8 POWER RAIL



VOLTAGE SEQUENCER



RESET FOR ASIC



IIT_MADRAS

Sheet: /power_2/

File: power_2.sch

Title: AARDONYX_DEVELOPMENT_BOARD

Size: A4

Date:

KiCad E.D.A. kicad (5.1.4)-1

Rev: R1V0

Id: 6/7

The diagram illustrates the PCB layout for the Aardonyx Development Board, organized into several functional blocks:

- SKT32E - PERIPHERALS:** This block contains the peripheral connections for the SKT32E chip. It includes SPI0 signals (nCS, CLK, MISO, MOSI) connected to U15A, UART0 signals (TX, RX), I2C0 signals (SDA, SCL), and various GPIO pins. It also shows connections for QSPI0 and QSPI1.
- SKT32E - POWER:** This block shows the power supply connections for the SKT32E chip. It includes VDD, VSS, and VSSO pins connected to the power plane (V1P8, V3P3) and ground (GND).
- SKT32E - SDRAM:** This block shows the SDRAM connections for the SKT32E chip. It includes SDRAM_A0-A12, SDRAM_D0-D31, and SDRAM_BA0-BA1 signals connected to U15B.
- MODE SELECT SWITCH:** This block shows a 3-position switch (SW3) used to select the boot mode (BOOT_MODE0, BOOT_MODE1, TEST_MODE). It includes pull-up resistors (R124, R125, R126) and a pull-down resistor (R127).
- Capacitors:** Numerous capacitors (C63-C87) are shown, primarily 0.1uF, connected to the power and ground planes to provide decoupling.

Metadata Table:

IIT_MADRAS			
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Title: AARDONYX_DEVELOPMENT_BOARD			
Size: A4	Date:	Rev: R1V0	
KiCad E.D.A. kicad (5.1.4) -1		Id: 7/7	