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Senior Design Project Report

on

Design and Layout of 8-bit Current Steering DAC

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SCHOOL OF ELECTRICAL AND ELECTRONICS ENGINEERING

CERTIFICATE

This is to certify that the project entitled **'DESIGN AND IMPLEMENTATION OF AN 8-BIT CMOS UNIT-ELEMENT CURRENT-STEERING DIGITAL-TO-ANALOG CONVERTER'** is a bonafide work carried out by the student team of **Akash Biradar (01FE22BEC287), Krishna Sebani (01FE22BEC302), Raju Baker (01FE22BEC274), Rohit Mandalollu (01FE21BEC257)**. The project report has been approved as it satisfies the requirements for the Mini Project work prescribed by the university curriculum for BE (VII Semester) in the Department of Electronics and Communication Engineering of KLE Technological University for the academic year **2025–2026**.

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-The project team

Abstract

The design and analysis of an 8-bit current steering Digital-to-Analog Converter (DAC) for high-speed, moderate-resolution applications are presented in this project. The suggested architecture uses current steering switches and binary-weighted current sources to translate digital input codes into analog output current, which is subsequently converted into voltage using a load resistor. Good linearity, low glitch energy, and quick settling time are prioritized. Through simulation, important performance metrics like power consumption, monotonicity, integral non-linearity (INL), and differential non-linearity (DNL) are examined. The findings show that high-frequency applications where accuracy and speed are crucial are a good fit for the current steering method. The 8-bit current steering DAC's full-custom layout was completed using analog VLSI layout best practices in addition to circuit design and simulation. In order to reduce process-induced mismatches, particular focus was placed on current source matching using symmetric routing, common-centroid layout techniques, and the use of dummy devices. While appropriate shielding and guard rings were used to increase noise immunity, critical signal paths were carefully routed to minimize parasitic effects. Design rule checks (DRC) and layout versus schematic (LVS) were successfully finished, and post-layout simulations were run to assess how parasitics affected DAC performance. The layout satisfies the design requirements with acceptable linearity and settling time degradation, according to the results, confirming the robustness of the suggested mixed-signal integrated circuit design.

Chapter 1

Introduction

In contemporary mixed-signal and communication systems, digital-to-analog converters (DACs) are essential components that allow digital data to be converted into continuous-time analog signals. Wireless transmitters, data converters, video processing systems, instrumentation, and high-speed communication interfaces are just a few of the many uses for DACs. The design of high-resolution, high-speed, and low-power DACs has grown more difficult as technology scales and system speeds rise. Because of its quick settling time, monotonic behavior, and compatibility with deep submicron CMOS technologies, the current-steering DAC is the most popular DAC architecture for high-speed applications. However, particularly during the major carry transition, purely binary-weighted current-steering DACs have significant glitch energy and poor linearity. Conversely, fully thermometer-coded DACs offer superior monotonicity and linearity but necessitate a large area and intricate decoding logic.

In order to get around these restrictions, this project uses an 8-bit segmented current-steering DAC, with a binary-weighted structure for the least significant bits (LSBs) and a thermometer-coded architecture for the most significant bits (MSBs). While preserving a respectable area and power efficiency, this segmentation successfully lowers glitch energy and enhances Differential Non-Linearity (DNL) and Integral Non-Linearity (INL).The DAC uses a 1.8 V supply voltage and is built using UMC 180 nm CMOS technology. A full-scale output current of roughly 490 µA is obtained by using a unit current of 1.925 µA. D-latches, which are powered by a single high-frequency clock, are integrated into each unit current cell to guarantee synchronous switching of the thermometer and binary current sources. To ensure matched propagation delays and reduce dynamic glitches at the output, additional delay elements are added to the binary path to offset the thermometer path's encoding delay.

The performance of high-speed current-steering DACs is largely dependent on layout. Layout symmetry, current matching, and power integrity are given particular attention in this project to guarantee that post-layout performance closely resembles schematic-level outcomes. To reduce the impact of process gradients and systematic mismatches, the unit current cells are arranged using a common-centroid and matrix-based configuration. To maintain matching accuracy, all unit cells have the same orientation and routing.Wide top-metal layers are used to create a reliable power distribution network (power mesh) that supplies VDD and VSS evenly throughout the DAC array. Multiple via arrays are used to guarantee low-resistance vertical connections between metal layers, and power rings and orthogonal power spines are used to minimize IR drop and electromigration effects.

1.1 Motivation

The need for DACs that can function at high frequencies while maintaining good linearity and low power consumption has increased due to the quick development of mixed-signal integrated circuits, data converters, and high-speed communication systems. Significant glitches, poor matching, and large non-linearity during major carry transitions plague conventional binary-weighted DAC architectures, particularly as resolution and speed rise. In applications like wireless transmitters and high-speed data links, these restrictions directly deteriorate signal quality.

By combining binary weighting for LSBs and thermometer coding for MSBs, the segmented DAC architecture offers a workable solution. This method eliminates excessive area or power penalties while increasing monotonicity and lowering DNL/INL errors. Furthermore, current-steering methods enable continuous current operation, which makes them ideal for high-speed settings. The need to comprehend and resolve practical non-idealities like delay mismatch, switching glitches, power distribution issues, and layout-induced errors in analog and mixed-signal design is what spurred this project. The project intends to close the gap between theoretical DAC behavior and realistic silicon implementation by implementing a segmented current-steering DAC at the transistor and layout level.

1.2 Objectives and specifications

Designing and implementing an 8-bit segmented current-steering Digital-to-Analog Converter (DAC) that achieves high-speed operation, good linearity, and dependable monotonic behavior appropriate for mixed-signal and communication applications is the goal of this project. By using binary weighting for the least significant bits and thermometer coding for the most significant bits, the design seeks to reduce common DAC non-idealities like glitch energy, delay mismatch, and non-linearity. Accurate current generation, digital and analog path synchronization, robust current summation, and accurate current-to-voltage conversion are all given special attention. In order to guarantee that simulated results closely resemble ideal DAC characteristics, the project also focuses on practical implementation elements like clocked switching, power distribution, and layout-aware design. The suggested DAC uses UMC 180 nm CMOS technology and is built as an 8-bit segmented current-steering architecture that runs on a 1.8 V supply voltage. A total of 256 discrete output levels are provided by the converter, which is composed of a 4-bit binary-weighted LSB section and a 4-bit thermometer-coded MSB section. Each thermometer unit current cell produces about 30.8 µA, which ensures a smooth transition across major carry boundaries. The LSB current is about 1.925 µA. With an 18 GHz clock and careful delay matching between the binary and thermometer paths to minimize glitches, the DAC can operate at high speeds. An instrumentation-amplifier-based I–V conversion stage is used to sum the differential output currents Iout-P and Iout-N and convert them into voltage.

1.3 Problem statement

Design and layout of 8 bit current steering DAC(Digital To Analog Converter).

Chapter 2

System Design

In this chapter, we will be looking towards the functional block diagram and also about the final design.

2.1 Block diagram and methodology

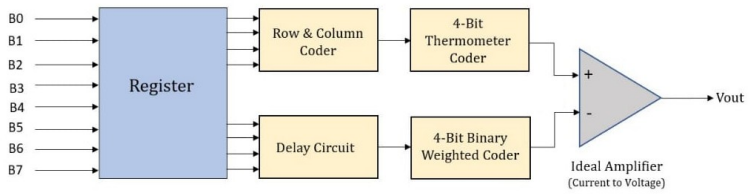

Figure 2.1: Block Diagram

2.2 Register

A vital digital interface between the input logic and the DAC core, the register block is in charge of guaranteeing steady, synchronized, and error-free operation. Eight D-gated latches, one for each input bit (D0–D7), make up the register in this project. The register's main function is to record the digital input data on a predetermined clock edge and maintain it throughout the conversion process. By doing this, undesired oscillations or transitions at the DAC input are avoided, which could otherwise cause distortion and glitches at the analog output.

The register makes sure that the binary-weighted LSB section and the thermometer-coded MSB section receive time-aligned input data by simultaneously clocking all latches using a common high-frequency clock. Because the thermometer encoder adds more logic delay than the binary path, this synchronization is crucial. By ensuring that all control signals driving the current-steering switches change at the same moment, the register and delay-matching techniques reduce glitch energy and enhance dynamic performance.

2.3 Final design

The project's final design is an 8-bit segmented current-steering DAC using a 1.8 V supply and UMC 180 nm CMOS technology. To achieve high speed, monotonicity, and improved linearity, the architecture is split into a 4-bit binary-weighted LSB section and a 4-bit thermometer-coded MSB section. The LSB section uses four scaled current sources for fine resolution, while the MSB section uses fifteen identical unit current cells arranged in a matrix to improve matching. To increase output resistance and current stability, each current cell uses a cascode current source. By directing current to either the positive output node (Iout-P) or the negative output node (Iout-N), differential current-steering reduces supply noise and guarantees a constant total current. All digital inputs are synchronized by a register stage with clocked D-latches, which reduces glitch energy and removes timing skew between the thermometer and binary paths.

The difference between the ideal LSB value and the actual step size between two consecutive DAC output codes is known as Differential Non-Linearity (DNL) at code k,

$$DNL(k) = \frac{I(k+1) - I(k)}{I_{LSB}} - 1 \tag{2.1}$$

The cumulative difference between the actual DAC output and the ideal transfer characteristic, normalized to the LSB, is known as Integral Non-Linearity (INL) at code k.

$$INL(k) = \frac{I(k) - I_{ideal}(k)}{I_{LSB}} \tag{2.2}$$

An instrumentation-amplifier-based current-to-voltage (I–V) conversion stage adds up the differential output currents and transforms them into a voltage. To minimize IR drop, substrate noise, and mismatch effects, careful power mesh design, symmetric routing, guard rings, and matched differential paths are employed at the layout level. The final output has low DNL and INL and closely resembles an ideal staircase waveform.

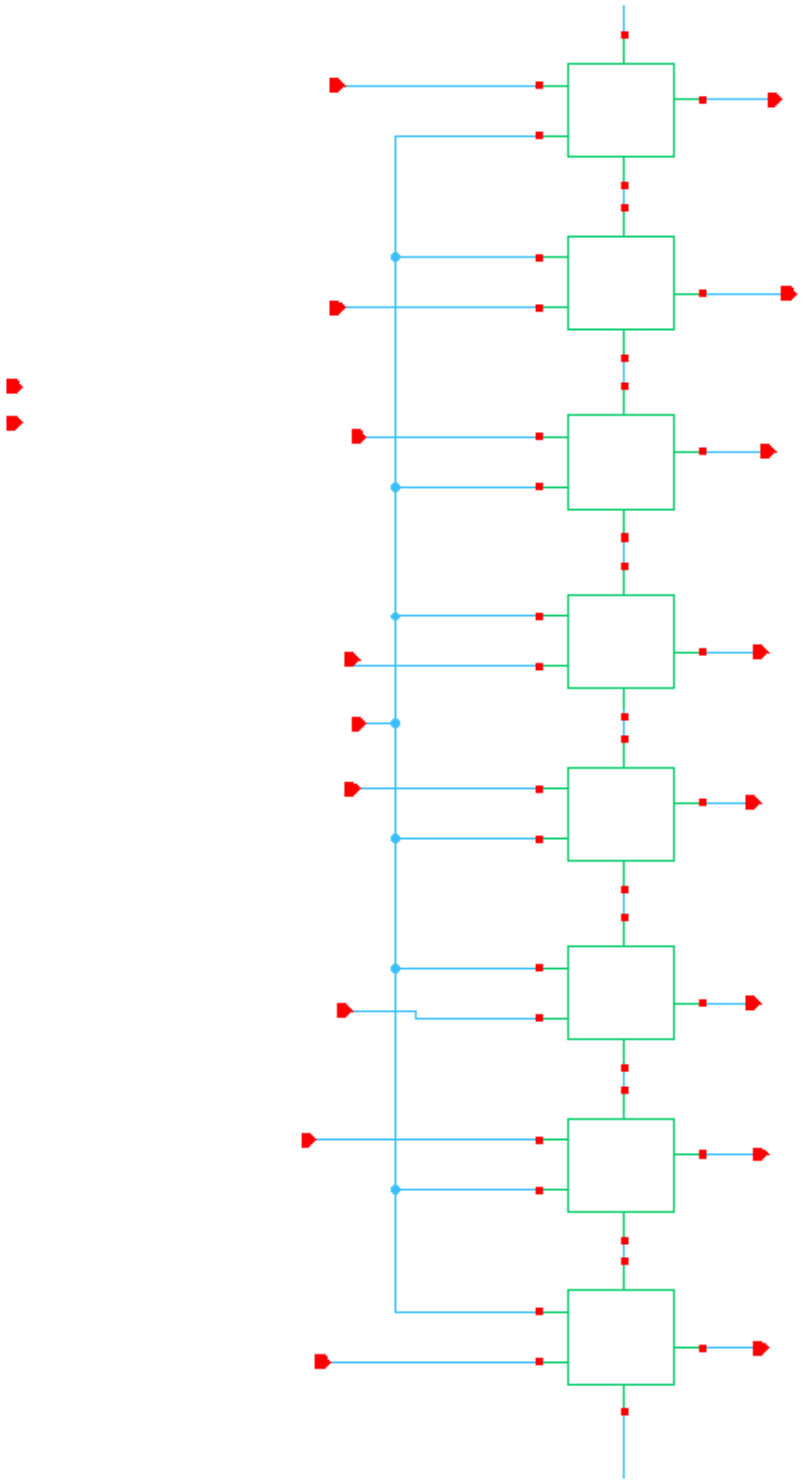

Figure 2.2: Register

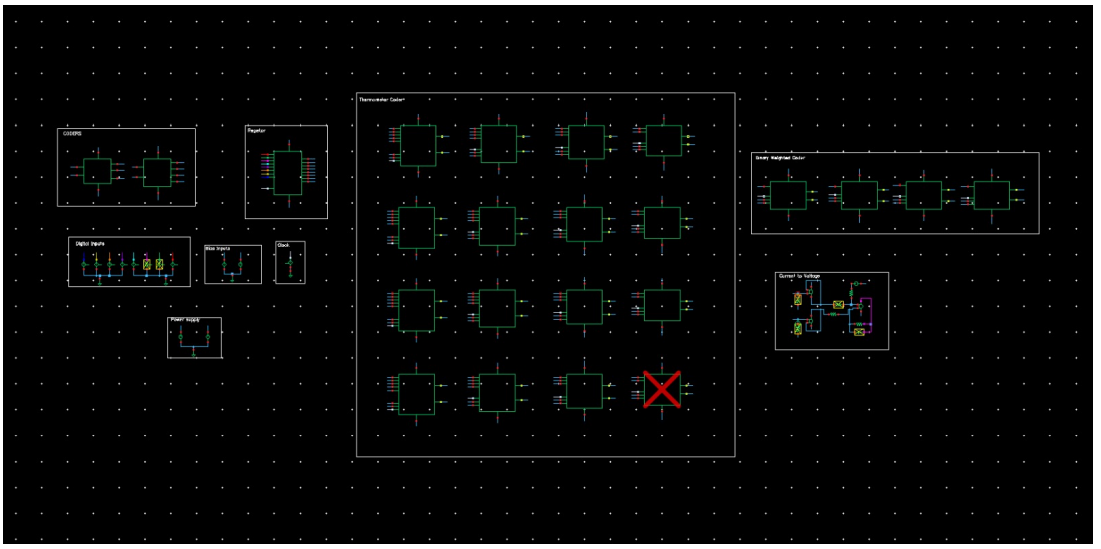

Figure 2.3: Final schematic design

Chapter 3

Implementation details

This chapter explains about individual components and their functions, we ensure that each component meets with required specs.

3.1 Final system architecture

3.1.1 Row and Column Coder

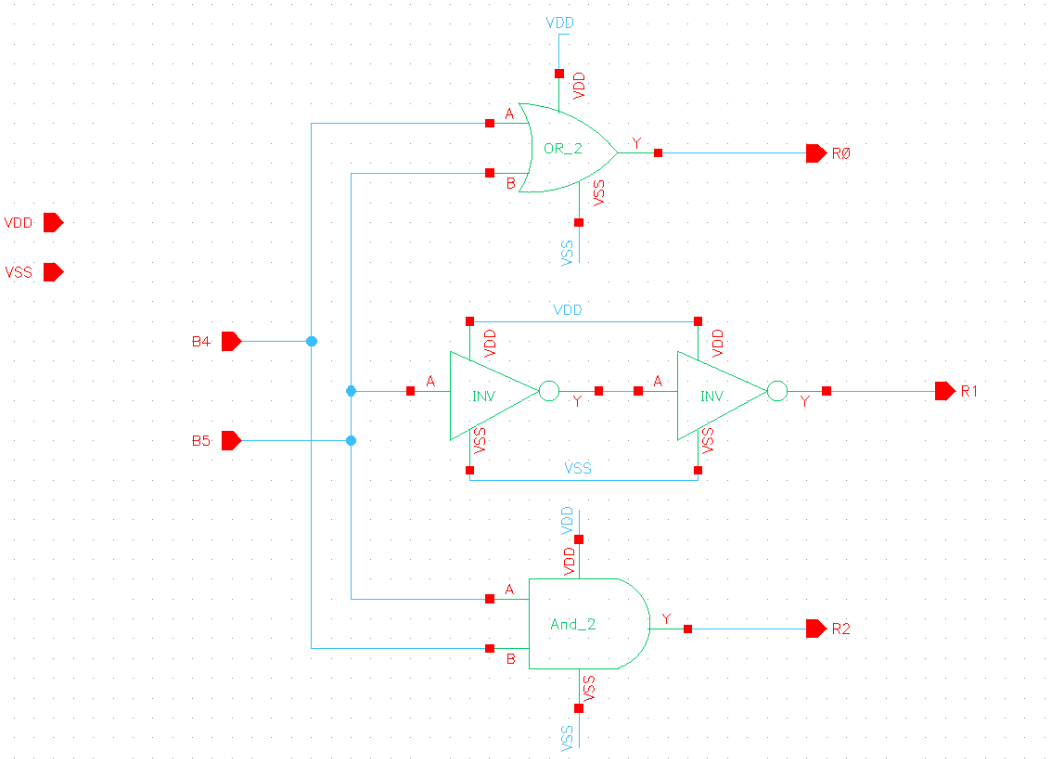

Figure 3.1: Row Coder

Row and column coders are used in the thermometer-coded MSB section of the proposed 8-bit segmented current-steering DAC to effectively control a large number of unit current

cells while preserving symmetry and reducing routing complexity. The thermometer code is divided into row and column signals to create a two-dimensional selection scheme for the current cell array rather than directly decoding every MSB bit into separate control lines.Whereas the column coder produces vertical enable signals, the row coder produces a set of horizontal enable signals. Only when the corresponding row and column signals are both asserted does a unit current cell become active. For a given MSB input code, this logical AND operation guarantees that the appropriate number of unit current sources are turned ON.

When compared to a single long thermometer decoder, such a structure greatly reduces capacitive loading, wiring congestion, and decoder complexity.Timing alignment and matching are also improved by using row and column coders. Delay mismatches are minimized because all row and column lines are routed symmetrically throughout the array, which lowers glitch energy during code transitions. The matrix arrangement also improves DNL and INL performance by averaging out process gradients and systematic mismatches.All things considered, the row and column coding technique makes thermometer decoding compact, scalable, and layout-friendly, which makes it ideal for high-speed and high-linearity current-steering DAC architectures.

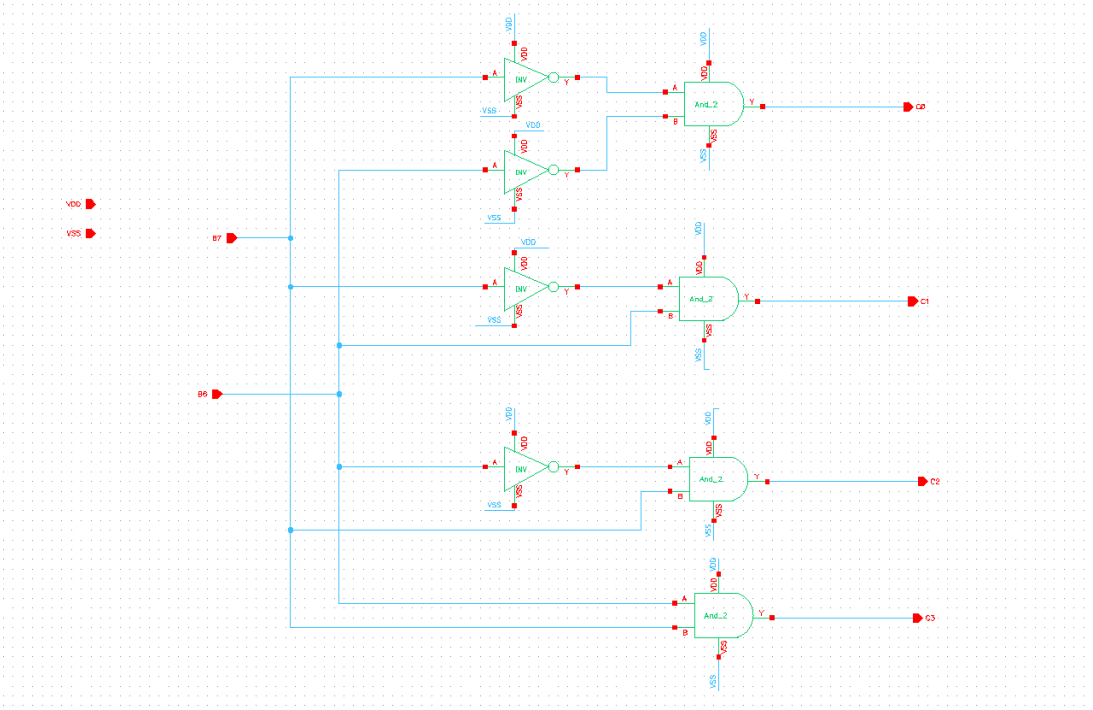

Figure 3.2: Column Coder

3.1.2 4-bit Thermometer Coder

The thermometer coder is a major role player in digital blocks for the MSB part of a segmented current-steering DAC that allows the circuit to operate properly and glitch-free. The coder changes a binary input word to a thermometer code, in which the amount of '1' bits equals to the value of the input. A thermometer coder with M bits provides an

output of $2^M - 1$ control signals, where all lower-order bits are at '1' and the rest of higher-order bits are at '0'.The thermometer coder in this architecture controls the same unit current cells, thus only one current source will be activated or deactivated per incremental code change. This feature is the reason why monotonicity is always assured, which means there are no missing codes and differential nonlinearity is greatly reduced. Thermometer coding in a binary-weighted switching method means less concurrent current transitions, so glitch energy is reduced and dynamic performance is better. To enable high-speed processing, the output of the thermometer coder is synchronized with a register stage such that all control signals switch at the same time. The coder is frequently integrated with row and column decoders to simplify wiring and allow for equal-sided processing of the present cell array. In conclusion, the thermometer coder is essential in achieving high linearity, low noise, and precise staircase signals in a current-steering DAC.

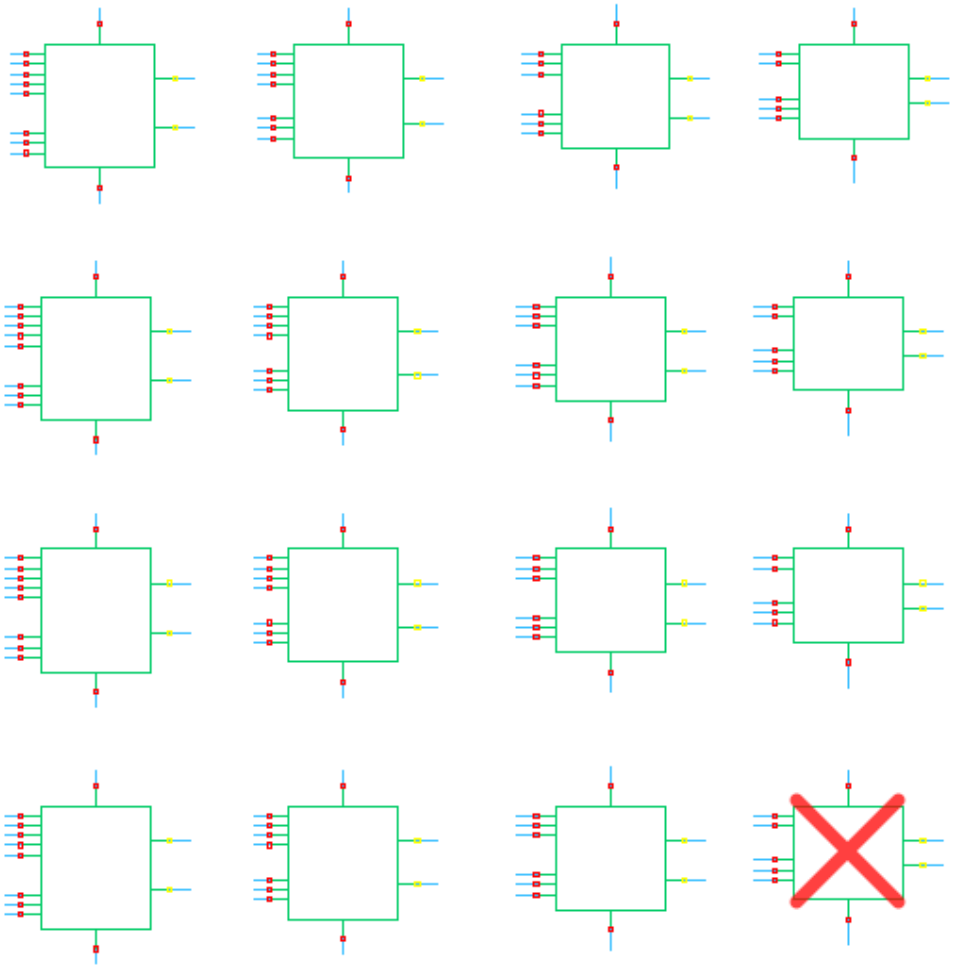

Figure 3.3: Thermometer Coder

3.1.3 4-bit Binary Weighted Coder

The binary-weighted coder is applied in the LSB part of a current-steering digital-to-analog converter. Its function is to offer a high degree of resolution with reduced com-

plexity. The binary-weighted coder simply assigns each digital input a current source with a magnitude proportional to a power of two. In an N-bit binary-weighted coder ,2^n relationship, which offers a precise incremental control of the DAC output.In this architecture, every single bit is responsible for a specific current source that is proportional to the respective bit weight, that is I_{LSB}, $2I_{LSB}$, $4I_{LSB}$ The output is loaded with the current from the current source when the bit is '1' and when the bit is '0', the current is brought to the complementary output. This method has a lesser current cell requirement compared to the full thermometer coding, thereby making the architecture area-efficient and suitable for the lower-significance bits.

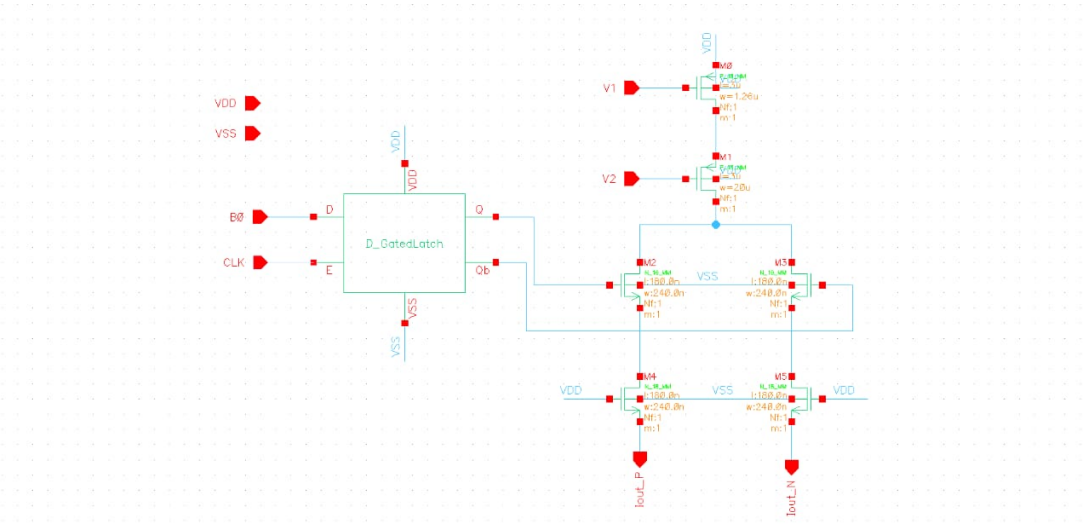

Figure 3.4: Binary Weighted Coder

However, since more than one bit can switch at a time during code transitions, binary-weighted coding is more prone to glitch energy and time mismatch. To counter these issues, the binary-coded outputs are synchronized utilizing a register stage and time-delayed to match the path of the thermometer-coder MSB. Through a combination of both binary-weighted coding for LSB and thermometer coding for MSB, an optimum trade-off in terms of linearity, speed, and silicon area is accomplished in a segmented DAC.

3.1.4 Unit Current Cell

The unit current cell marks the most basic element of the current-steering Digital-to-Analog Converter and generates a current that is accurate and stable as a reference. The proposed architecture has each current cell that contains a stacked MOS current source together with a differential current-steering switch. Cascode arrangement raises output resistance which in turn increases the accuracy of current and decreases the impact of voltage variations at the output nodes. All unit cells utilize the same transistor dimensions and biasing conditions in order to provide the highest matching accuracy. To counteract systematic mismatch and process gradient effects, the unit current cells are placed using a common-centroid and matrix-based layout arrangement with dummy cells at the corners. The unit cell during its operation directs the current to either the positive or negative

output node as per the digital control signal, thus facilitating monotonic and low-glitch DAC operation.

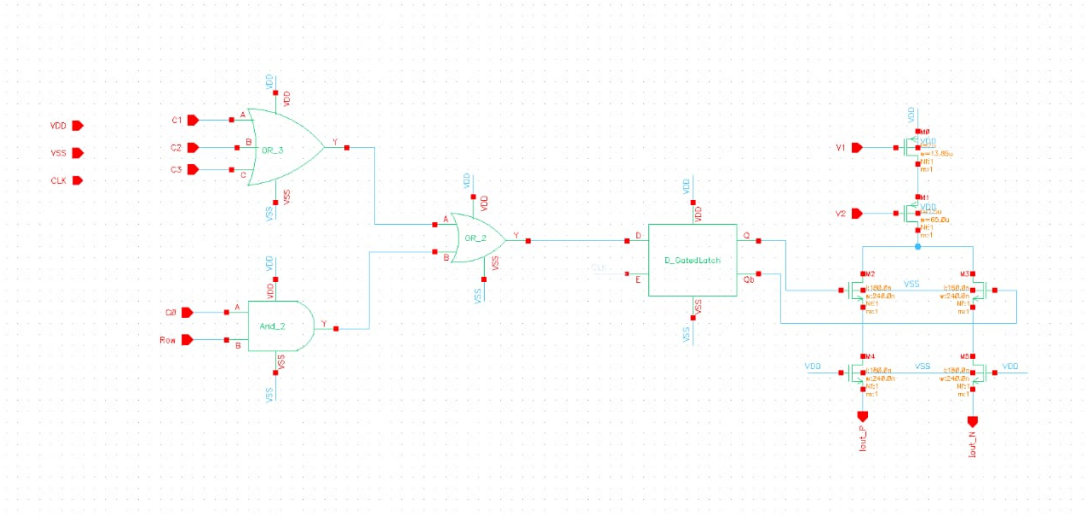

Figure 3.5: Unit Current Cell

3.1.5 Ideal Amplifier(Current to Voltage)

An ideal amplifier is one of the main tools in the circuit design and simulation process. Its characteristics are very close to the real amplifiers, as they exhibit no imperfections, therefore, in this project, an ideal amplifier is used with the output of the DAC to make the transition from a differential current to a voltage with no added non-ideal effects. When the ideal situation is considered, the influence of the DAC core, which includes current matching, switching behavior, and coding architecture, can be assessed separately from the limitations of the output amplifiers.

The ideal amplifier has infinite gain in the open loop, infinite input resistance, zero output resistance, infinite bandwidth, and zero input offset voltage. With these assumptions, it can be concluded that neither will the amplifier load the output of the DAC nor will it affect the output in any way, such that the output voltage will be linearly proportional to the input current. Therefore, all non-ideal effects of the staircase waveform will be solely a function of the DAC configuration and not of the amplification process. During the early design and verification phases, the use of an ideal amplifier is especially advantageous. It sets a standard for measurable parameters such as DNL, INL, and glitch energy to be clearly evaluated. After the DAC core has been aligned with the target parameters with the ideal amplification, the ideal block can subsequently be substituted with a real transimpedance or instrumentation amplifier for practical performance evaluation and silicon implementation.

3.1.6 DAC layout

During the layout stage, the perfect amplifier is modeled using a graphic/abstract box and placed near the DAC output nodes to reduce parasitic resistance and capacitance. The differential input signals from the DAC to the amplifier are laid out in a symmetrical

manner. Dedicated and broad VDD/VSS lines have proper metal stacking to provide a low IR drop and stable supply. Guard rings and sufficient distances from digital elements are observed in order to decouple the amplifier from substrate noise and digital switching.

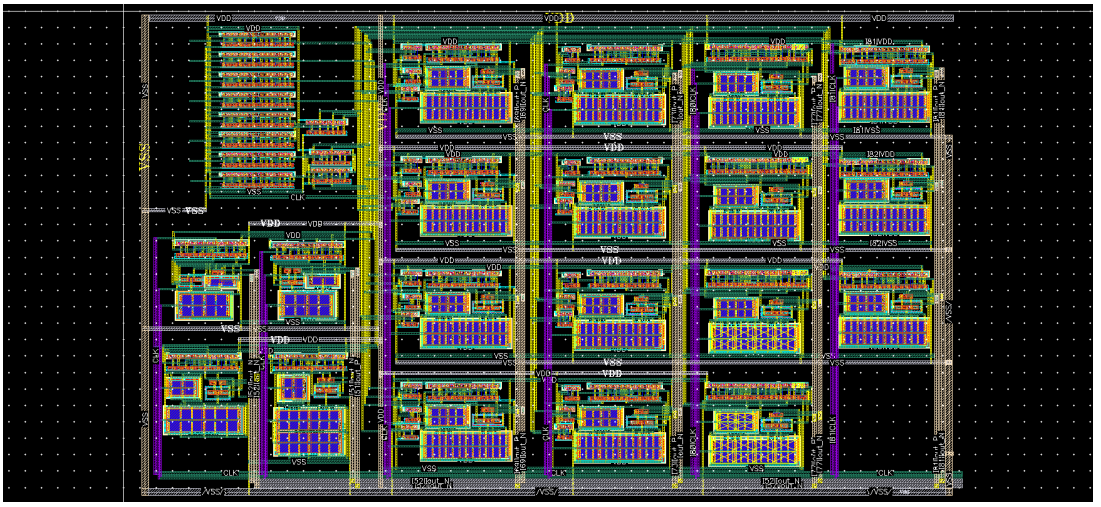

Figure 3.6: DAC Layout

Chapter 4

Result and conclusion

The design of the DAC was simulated running transient and DC analyses to characterize static and dynamic performances. A digital up-counter was applied to sweep all 256 input codes, while the registered outputs provided synchronized switching between the thermometer-coded MSB path and binary-weighted LSB path. The output current resulting from that exhibited step transitions that were uniform in amplitude and closely followed the ideal staircase behavior, which corroborates proper current scaling and accurate decoding of code.Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) were calculated based on the simulated output current to evaluate static linearity. The DNL was kept at ± 1 LSB for all codes, thus signaling the non-decreasing operation without any missing codes at the same time, in contrast to the INL which showed only a slight cumulative shift as a result of the finitecurrent-source mismatch and routing parasitics.

A reduction of glitch energy was observed during major code transitions in the dynamic analysis which confirmed the success of the segmentation and the synchronized register-based switching techniques.The results from the simulation overall validate that the recommended 8-bit segmented current-steering DAC is capable of achieving the desired specifications with respect to linearity, monotonicity, and output accuracy. The high similarity between the simulated and the ideal outputs indicates that the architecture chosen, the coding scheme as well as the layout-aware design techniques are applicable to the high-speed and high-resolution mixed-signal applications.

4.1 Output Waveform

The figure is a time domain representation of the 8-bit DAC system, including the digital inputs, the clock signal, the output voltage, and the differential output currents. The results of the simulations confirm the correct digital sequence, the switching, and the current to voltage conversion. The first eight waveforms represent the input bits of the DAC from the least significant bit (LSB) B0 to the most significant bit (MSB) B7. B0, as expected, switches with the highest frequency, and the rest of the bits follow down to the MSB toggling at the lowest frequency, thus confirming the right binary counting and proper register operation without any metastability or missing transitions.The input bits are displayed with the clock waveform below and the registers that latch the digital inputs are driven by it. The perfect and regular clock makes sure that all DAC control signals are updated at the same time, which is very important to reduce glitch energy during code transitions.

The Vout signal shows a steady staircase-like ramp that corresponds to the rising dig-

ital input codes. The minor sawtooth pattern seen in every ramp section is a result of the addition of current in steps and the limited time for updates. The lack of major spikes is proof of the low glitch energy and good matching of the thermometer-coded MSBs and binary-weighted LSBs.The positive branch currents of the differential DAC output are shown in the bottom waveforms. The input code causes these currents to rise linearly and regularly reset, which shows segmented switching behavior. The close matching of the two currents signifies excellent current-source matching and active common-mode error cancellation.The transient response has verified that the featuring 8-bit segmented current-steering DAC works correctly with precise digital control, steady current production, and continuous voltage offtake. The outcome proves that the selected design architecture and timing technique can bring down switching errors effectively and cater to fast DAC operation at the same time.

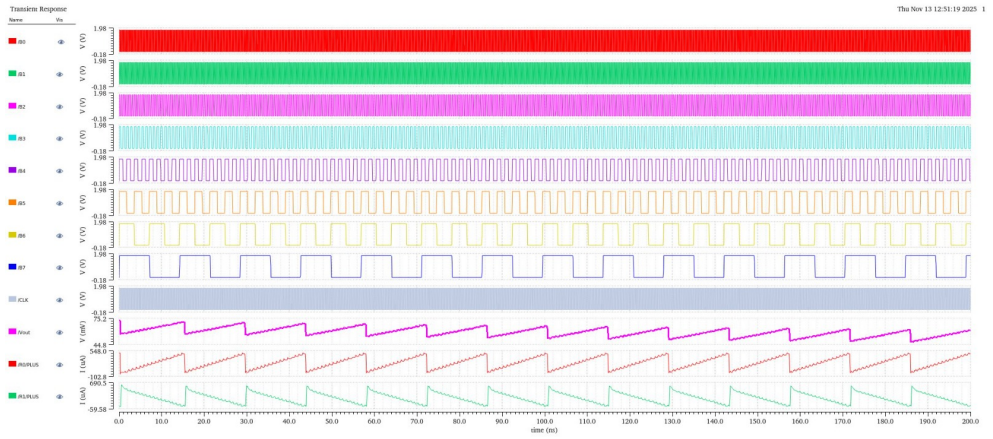

Figure 4.1: Output waveform

4.2 DRC(Design Rule Check) simulation

The simulation of the DRC verified that the entire DAC layout was in compliance with all UMC 180 nm design rules, and no violations were reported. All the corresponding layers of metal, poly, active, and vias meet the required minimum width, spacing and enclosure constraints.

4.3 Layout Versus Schematic (LVS) simulation

Layout Versus Schematic (LVS) checking was done to confirm that the schematic and the extracted layout were corresponding. The results of LVS indicated a complete match in terms of device count, connectivity, and net names which stated that the physical layout was a correct representation of the intended circuit design.

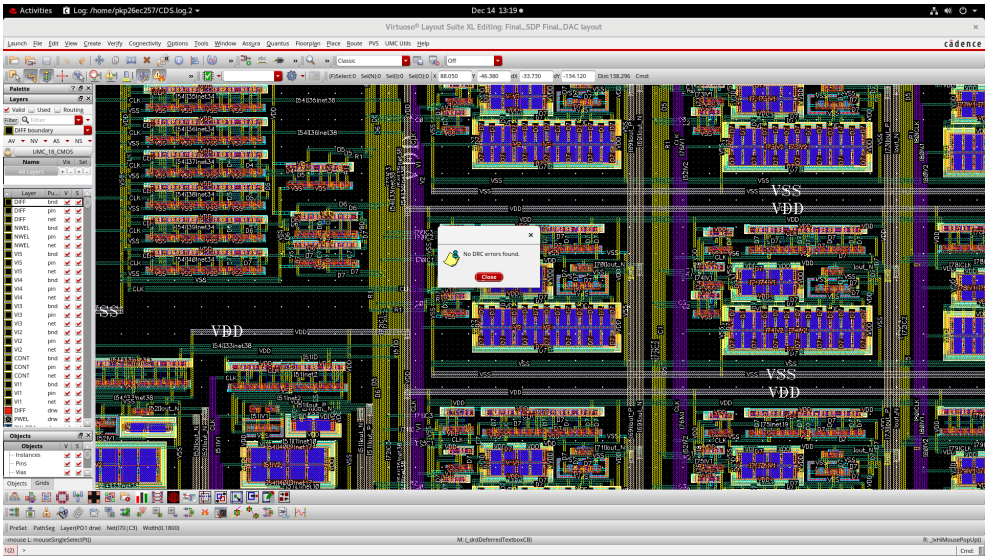

Figure 4.2: DRC results

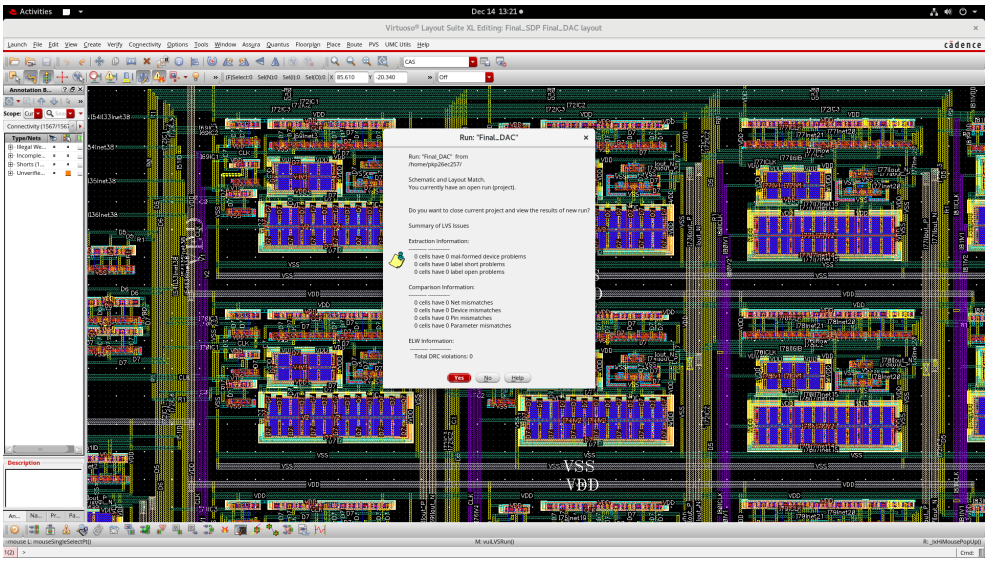

Figure 4.3: LVS results

Chapter 5

conclusion and future scope

5.1 Conclusion

It was possible to design, implement, and verify an 8-bit segmented current-steering Digital-to-Analog Converter using CMOS technology. The proposed architecture features improved linearity and monotonicity, without significant area penalty or excessive power consumption, thanks to thermometer coding for the Most Significant Bits and binary-weighted coding for the Least Significant Bits. The current generation, switching operation, and current-to-voltage conversion at the output stage were found to be appropriate in detailed circuit-level simulations. Layout-level verification had been performed using DRC and LVS and passed with full compliance to foundry rules and consistency of schematics. In general, the results obtained prove that the proposed DAC is a reliable and efficient solution for mixed-signal systems, and the methodology of the design can be further extended to higher resolution DACs.

5.2 Future scope

The suggested segmented current-steering DAC design has the potential for further enhancement by increasing its resolution past the 8-bit limit to cater to the needs of high-precision applications. The application of advanced techniques like dynamic element matching (DEM) could be beneficial for the sake of minimizing the effects of mismatch while enhancing DNL and INL performance. Speed and power usage could be upgraded by utilizing scaled CMOS technology for the redesign of the switching network and the output amplifier. Besides, the combination of chip calibration and digital correction techniques could be a plus for the DAC's ability to cope with variations of process, voltage, and temperature, thus making it suitable for both high-speed communication and low-power system-on-chip (SoC) applications.

Chapter 6

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