Digital to Analog Converter(DAC)

SDP-70

Rohit Mandalollu, Raju Barker, Akash Biradar, Krishna Sebani
Department of Electronics and Communication
Email : 01fe22bec257@kletec.ac.in, 01fe22bec274@kletec.ac.in, 01fe22bec287@kletec.ac.in 01fe22bec302@kletec.ac.in

Senior Design Project-2025-26

Problem Statement

Design and Layout of 8 Bit current steering Digital to Analog Converter

Objectives

- To design an 8-bit segmented current-steering DAC in UMC 180 nm technology
- To implement precision current cells with synchronized switching and robust power distribution
- To perform current-to-voltage conversion and validate performance through simulation and layout

Literature survey

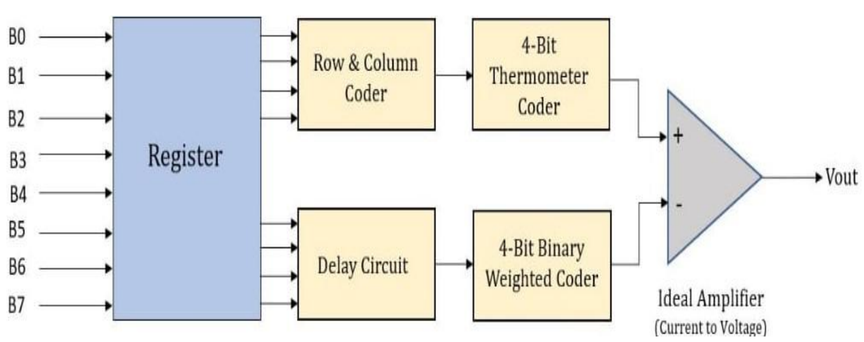
- Prior studies emphasize current-steering DACs effectively address major-carry glitches seen in binary DACs by using thermometer coding for MSBs while preserving area efficiency with binary-weighted LSBs.

Contributions

Full-custom layout of DAC:

- Segmented DAC Architecture with Optimized Current Scaling
- Layout Techniques for Current Matching and Linearity Enhancement

Proposed Methodology



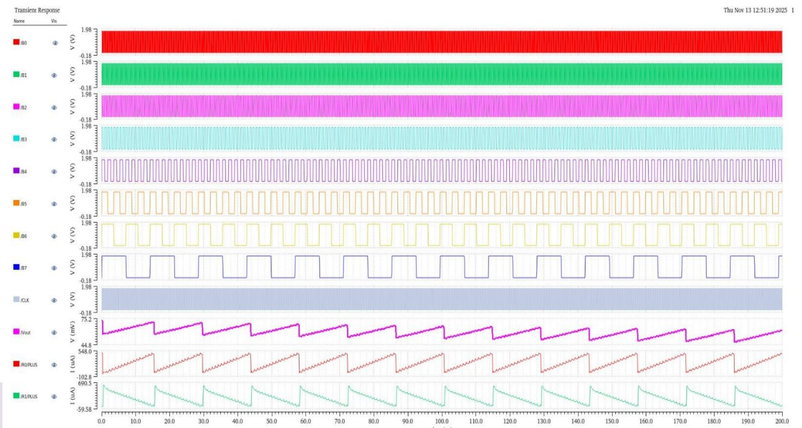
DAC Architecture: Designed an 8-bit high-performance segmented current-steering DAC with a 4-bit thermometer-coded MSB for improved linearity and a 4-bit binary-weighted LSB for fine resolution

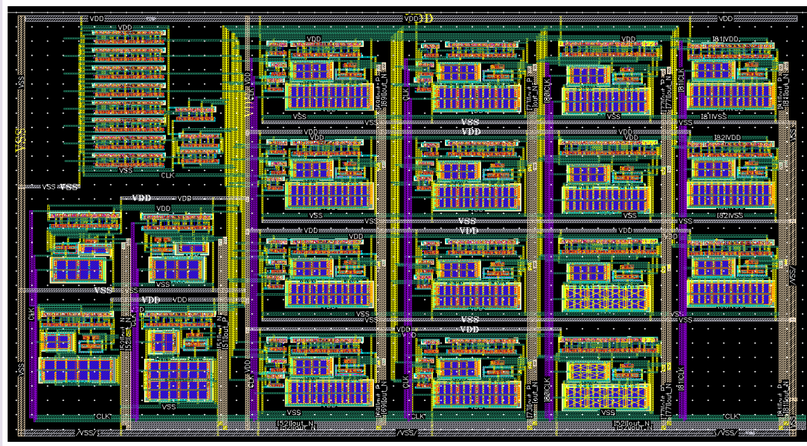
Digital Input Generation: Inputs generated via a synchronous up-counter and fed through registers to ensure stable timing and controlled data flow.

Current Cell Design: MSB (thermometer-coded): Identical cascode current cells for excellent matching and monotonicity. LSB (binary-weighted): Scaled current cells for precise LSB steps

Ideal Amplifier: An ideal amplifier is used at the DAC output to convert current to voltage without introducing non-ideal effects, enabling accurate evaluation of the DAC core performance. This helps isolate and analyze DAC parameters before replacing it with a real amplifier.

Results and Inferences





Conclusions

An 8-bit segmented current-steering DAC was designed and verified in CMOS, achieving good linearity and monotonicity using thermometer and binary coding. Simulations and DRC/LVS checks confirmed correct operation, showing the design is reliable and scalable to higher resolutions.

Semester: VII

Under the guidance of: Dr . Sujata S. Kotabagi