

Introduction to DSP with the ARM Cortex-M4 Microcontroller

Sergio Liberman
Senior Microcontroller Systems Engineer

CTEA Electronics Design and Manufacturing Symposium February 21, 2012





are trademarks of Freescale Semiconductor, Inc., Reg., U.S. Pat. & Tm. Off. BeeKlf, BeeSlack, Cold/Fire , CoreNet, Flexis, Kinelis, MXC, Platform in a Package, Processor Expert, CorlO Qonverge, Qorivva, QUICC Engine, SMARTMOS, TurboLink, VortiQa and Xtrinsic are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. © 2011 Freescale Semiconductor, Inc.

ARM Cortex Processor Families

Cortex-A









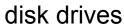
servers

set top boxes

netbooks

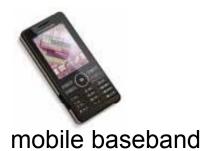
Cortex-R







digital cameras



Cortex-M





motors



ARM Cortex-M4: Efficient Blend

Ease of use C Programming Interrupt handling Ultra low power Cortex-M4 Cortex-M4 Cortex-M4 DSP Harvard architecture Single cycle MAC Floating Point Barrel shifter





















ARM Cortex-M4 Microarchitecture

ARMv7ME Architecture

- Thumb-2 Technology, 1.25 DMIPS/MHz
- Integrated NVIC and optional MPU
- Low cost debug and trace
- Integrated DSP and SIMD instructions
- Single cycle MAC (Up to 32 x 32 + 64 -> 64)
- Optional single precision FPU

Microarchitecture

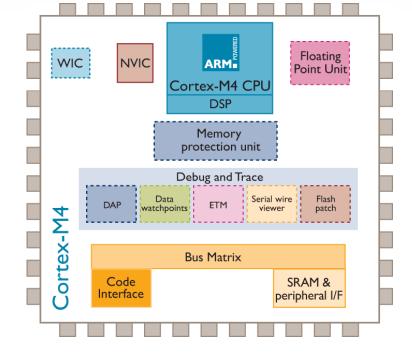
- 3-stage pipeline
- 3x AHB-Lite Bus Interfaces

Configurable for ultra low power

- Deep Sleep Mode, Wakeup Interrupt Controller
- Power down features for Floating Point Unit

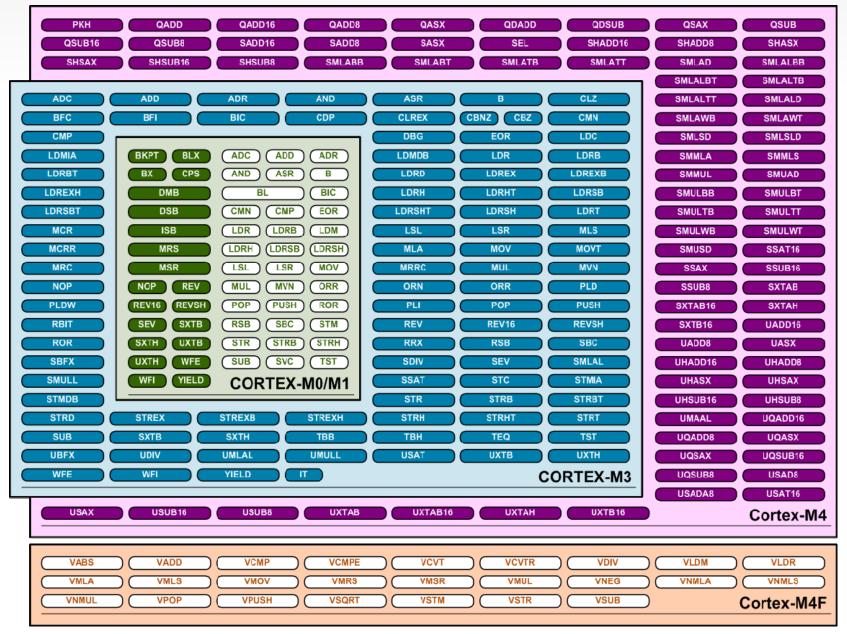
Flexible configurations for wider applicability

- Configurable NVIC and Debug & Trace. Optional MPU, WIC and FPU.





ARM Cortex-M Family Instruction Set





ARM Cortex-M4 DSP Instructions Compared

		Cyc	Cycle counts				
CLASS	INSTRUCTION	ARM9E-S		Cortex-M4			
Arithmetic	ALU operation (not PC)	1 - 2	1	1			
	ALU operation to PC	3 - 4	3	3			
	CLZ	1	1	1			
	QADD, QDADD, QSUB, QDSUB	1 - 2	n/a	1			
	QADD8, QADD16, QSUB8, QSUB16	n/a	n/a	1			
	QDADD, QDSUB	n/a	n/a	1			
	QASX, QSAX, SASX, SSAX	n/a	n/a	1			
	SHASX, SHSAX, UHASX, UHSAX	n/a	n/a	1			
	SADD8, SADD16, SSUB8, SSUB16	n/a	n/a	1			
	SHADD8, SHADD16, SHSUB8, SHSUB16	n/a	n/a	1			
	UQADD8, UQADD16, UQSUB8, UQSUB16	n/a	n/a	1			
	UHADD8, UHADD16, UHSUB8, UHSUB16	n/a	n/a	1			
	UADD8, UADD16, USUB8, USUB16	n/a	n/a	1			
	UQASX, UQSAX, USAX, UASX	n/a	n/a	1			
	UXTAB, UXTAB16, UXTAH	n/a	n/a	1			
	USAD8, USADA8	n/a	n/a	1			
Multiplication	MUL, MLA	2 - 3	1 - 2	1			
	MULS, MLAS	4	1 - 2	1			
	SMULL, UMULL, SMLAL, UMLAL	3 - 4	5 - 7	1			
	SMULBB, SMULBT, SMULTB, SMULTT	1 - 2	n/a	1			
	SMLABB, SMLBT, SMLATB, SMLATT	1 - 2	n/a	1			
	SMULWB, SMULWT, SMLAWB, SMLAWT	1 - 2	n/a	1			
	SMLALBB, SMLALBT, SMLALTB, SMLALTT	2 - 3	n/a	1			
	SMLAD, SMLADX, SMLALD, SMLALDX	n/a	n/a	1			
	SMLSD, SMLSDX	n/a	n/a	1			
	SMLSLD, SMLSLD	n/a	n/a	1			
	SMMLA, SMMLAR, SMMLS, SMMLSR	n/a	n/a	1			
	SMMUL, SMMULR	n/a	n/a	1			
	SMUAD, SMUADX, SMUSD, SMUSDX	n/a	n/a	1			
	UMAAL	n/a	n/a	1			
Division	SDIV, UDIV	n/a	2 - 12	2 - 12			





ARM Cortex-M4 Single Cycle MAC Instructions

OPERATION	INSTRUCTIONS
16 x 16 = 32	SMULBB, SMULBT, SMULTB, SMULTT
$16 \times 16 + 32 = 32$	SMLABB, SMLABT, SMLATB, SMLATT
16 x 16 + 64 = 64	SMLALBB, SMLALBT, SMLALTB, SMLALTT
$16 \times 32 = 32$	SMULWB, SMULWT
$(16 \times 32) + 32 = 32$	SMLAWB, SMLAWT
$(16 \times 16) \pm (16 \times 16) = 32$	SMUAD, SMUADX, SMUSD, SMUSDX
$(16 \times 16) \pm (16 \times 16) + 32 = 32$	SMLAD, SMLADX, SMLSD, SMLSDX
$(16 \times 16) \pm (16 \times 16) + 64 = 64$	SMLALD, SMLALDX, SMLSLD, SMLSLDX
$32 \times 32 = 32$ $32 \pm (32 \times 32) = 32$ $32 \times 32 = 64$ $(32 \times 32) + 64 = 64$ $(32 \times 32) + 32 + 32 = 64$	MUL MLA, MLS SMULL, UMULL SMLAL, UMLAL UMAAL
32 ± (32 x 32) = 32 (upper) (32 x 32) = 32 (upper)	SMMLA, SMMLAR, SMMLS, SMMLSR SMMUL, SMMULR

All the above operations are single cycle on the Cortex-M4 processor



ARM Cortex-M4 Floating Point Unit

- Single precision floating point unit
- IEEE 754 standard compliant
- Single-precision floating point math
 - Add, subtract, multiply, divide, MAC and square root
 - Fused MAC higher precision

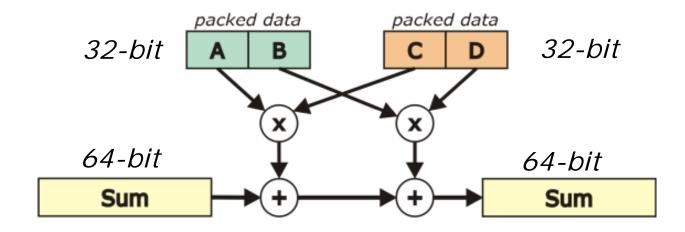
OPERATION	CYCLE COUNT
Add/Subtract	1
Divide	14
Multiply	1
Multiply Accumulate (MAC)	3
Fused MAC	3
Square Root	14



ARM Cortex-M4 SIMD Instructions

SIMD extensions perform multiple operations in one cycle

$$Sum = Sum + (A \times C) + (B \times D)$$



SIMD techniques operate with packed data



ARM Cortex-M4 8 and 16-bit SIMD Instructions

Prefix	S	Q	SH	U	UQ	UH			
	Signed	Signed	Signed	Unsigned	Unsigned	Unsigned			
Instr		Saturating	Halving		Saturating	Halving			
ADD8	SADD8	QADD8	SHADD8	USADD8	UQADD8	UHADD8			
SUB8	SSUB8	QSUB8	SHSUB8	USUB8	UQSUB8	UHSUB8			
ADD16	SADD16	QADD16	SHADD16	UADD16	UQADD16	UHADD16			
SUB16	SSUB16	QSUB16	SHSUB16	USUB16	UQSUB16	UHSUB16			
ASX	SASX	QASX	SHASX	UASX	UQASX	UHASX			
SAX	SSAX	QSAX	SHSAX	USAX	UQSAX	UHSAX			
USAD8	Unsigned Sum of Absolute Difference (8 bits)								
USADA8	Unsigned Sum of Absolute Difference and Accumulate (8 bits)								

ASX

- 1. Exchanges halfwords of the second operand register
- 2. Adds top halfwords and subtracts bottom halfwords

SAX

- 1. Exchanges halfwords of the second operand register
- 2. Subtracts top halfwords and adds bottom halfwords



Characteristics of DSP Processors

- Harvard architecture
- High performance MAC
- Saturating math
- SIMD instructions for parallel computation
- Barrel shifters
- Floating point hardware
- Circular and bit-reversed addressing
- Zero overhead loops
- Load and store operations in parallel with math operations

Text in **bold** indicates DSP processor advantage over Cortex-M4



Cortex-M4 DSP Code Optimization Strategies

- Circular addressing alternatives
- Loop unrolling
- Caching of intermediate variables
- Extensive use of SIMD and intrinsics



ARM Cortex-M4 FIR Performance

- DSP assembly code = 1 cycle
- Cortex-M4 standard C code takes 12 cycles
 - ✓ Using circular addressing alternative = 8 cycles
 - ✓ After loop unrolling < 6 cycles
 </p>
 - ✓ After using SIMD instructions < 2.5 cycles [note: 16-bit data]
 </p>
 - ✓ After caching intermediate values ~ 1.6 cycles

Cortex-M4 C code now comparable in performance



Cortex Microcontroller Standard (CMSIS)

- Cortex Microcontroller Software Interface Standard
 - Abstraction layer for all Cortex-M processor based devices
 - Developed in conjunction with silicon, tools and middleware partners

- Benefits to the embedded developer
 - Consistent software interfaces for silicon and middleware vendors
 - Simplifies re-use across Cortex-M processor-based devices
 - Reduces software development cost and time-to-market
 - Reduces learning curve for new Cortex microcontroller developers

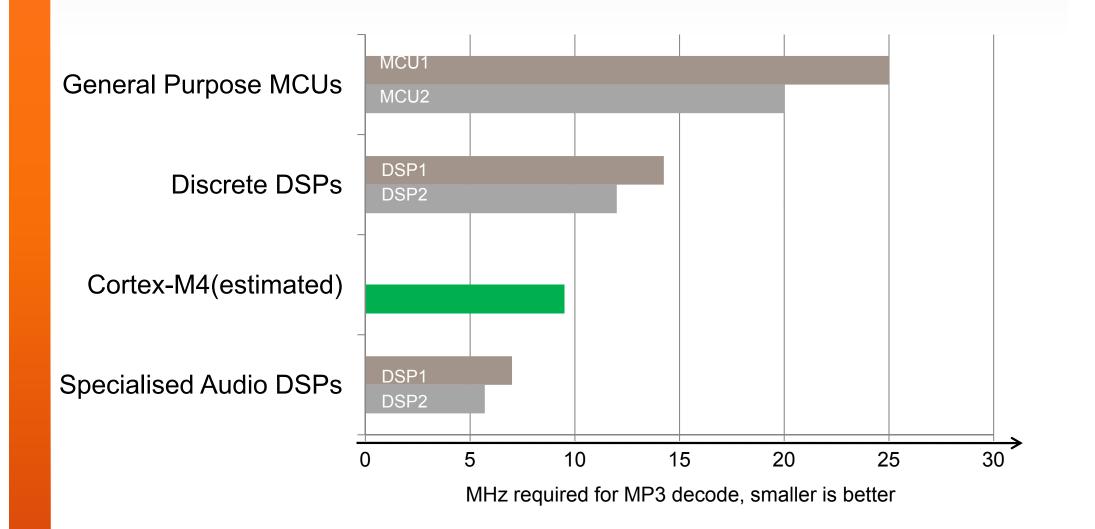


ARM CMSIS DSP Library Snapshot

- Basic math vector mathematics
- Fast math sin, cos, sqrt, etc.
- Interpolation linear, bilinear
- Complex math
- Statistics max, min, RMS, etc.
- Filtering IIR, FIR, LMS, etc.
- Transforms FFT(real and complex), Cosine transform, etc.
- Matrix functions
- PID Controller, Clarke and Park transforms
- Support functions copy/fill arrays, data type conversions, etc
- Available at http://www.onARM.com
 Variants for functions across q7,q15,q31 and f32 data types



ARM Cortex-M4: MP3 Decoder Performance





Kinetis Cortex-M4 Audio Player

Audio Input:

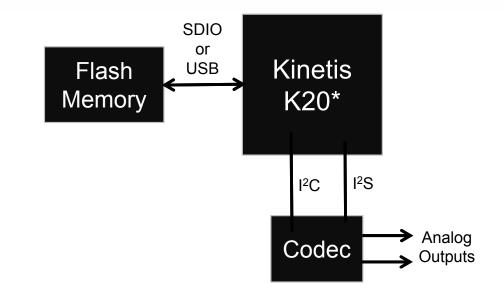
- WAV files
- MP3 files
- AAC files

Functions:

File decode

Output:

Stereo analog audio



* Could also use K40, K50, K60, or K70





Freescale Kinetis Cortex-M4 Microcontroller Family

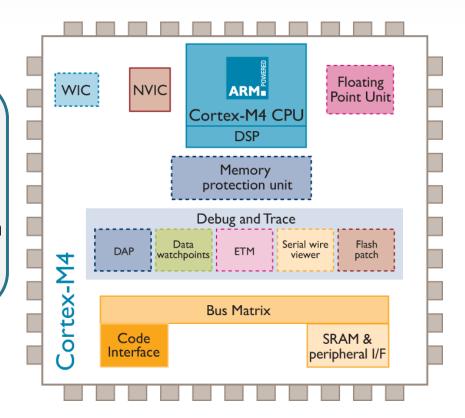




Ereascale, the Freescale loge, AlliVac, C-5, CodaTEST, CodelWarrior, ColdFire, C-Ware, I. he Energy Efficient Solutions logo, mobileGT, PowerQUICC, OorlQ, StarCore and Symphony are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. Beekli, BeeStack, ColdFire+, CoreNet, Flexis, Kinetis, MXC, Platform in a Package, Processor Expert, QorlQ Converge, Oorlvva, QUICC Engine, SMARTMOS, TurboLink, VortiQa and Xtrinsic are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. © 2011 Freescale Semiconductor, Inc.

Kinetis Cortex-M4 Processor Microarchitecture

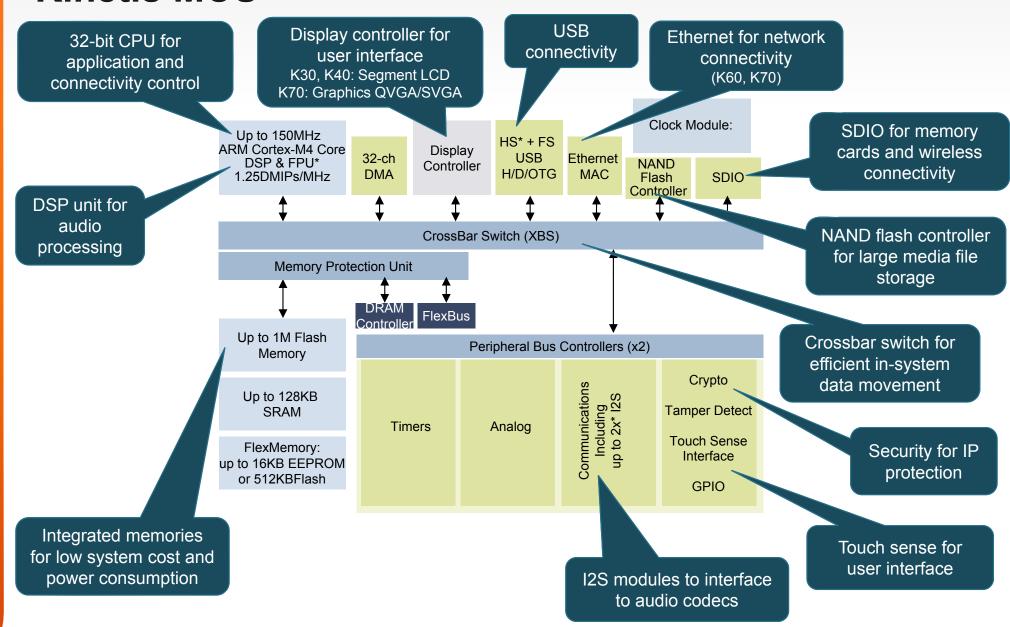
- Backwards compatible with ARM Cortex-M3
- New features
 - DSP extensions
 - Single precision floating point unit
- Freescale IP and innovation
 - Available on-chip cache for instructions and data enhanced performance reaching zero wait states
 - Crossbar switch for concurrent multi-master/slave accessing improves system throughput
 - MPU with multi-master protection enhances system safety and security
 - Low-leakage wake-up unit adds flexibility for lowpower operation
- Architected for digital signal processing
 - Motor Control advanced algorithms, longer lifespan, power efficiency
 - Automation high calculation and algorithm bandwidth at a low cost
 - Power Management designed for low/batterypowered systems
 - Audio and Video 5x performance improvement over software, helping batteries last longer



http://www.freescale.com/kinetis



Kinetis MCU





Kinetis Product Families

NOTE: Floating point unit and NAND flash controller are only offered on 120/150MHz K10/20/60/70 devices.

Sample availability:

144 256nin now 106nin now

	ect					<u>ت</u> ک	S	ect		Official	ea on <u>120/130MHz</u>	1(10/20/00/10 dev	1003.
	H2)		(889)	fion	S	trolle z onl	it z on	. Det	<u>\$</u>	Sample availabil	ity:		
MCU	USB OTG (FS & HS) + Device Charger Detect		Ethernet (IEEE 1588)	Hardware Encryption	LCD (Segment/Graphics)	NAND Flash Controller (120MHz/150MHz only)	Floating Point Unit (120MHz/150MHz onlv)		DRAM Controller (256MAPBGA only)	144pin now , 80-121pin now, <80pin now			ow
Family	G (F Che	Z		e En	t/Gra	lash 2/15(Poir 2/15(- Tal	ontro				NW .
	3 OT	Dual CAN	rnet	Jwar	men	E H	ating MH;	ware	DRAM Controller (256MAPBGA on	144pin now, 80-121pin now, <80pin now			
	USE + De	Dua	Ethe	Harc	LCD (Seg	NAN (120	Floa (120	Hard	DRA (256	144-256pin now, 196pin now			
K70 120-150MHz 512KB-1MB										Common System IP	Common Analog IP	Common Digital IP	Development Tools
196-256pin K60 100-150MHz										32-bit ARM Cortex-M4 Core	16-bit ADC	CRC	Bundled IDE w/ Processor
256KB-1MB										w/ DSP Instructions		I ² C Expert	Expert
100-256pin K50										Next Generation Flash Memory			Bundled OS
72-100MHz 128-512KB								 		High Reliability, Fast Access	Programmable Gain Amplifiers	SAI (I ² S)	USB, TCP/IP, Security
64-144pin K40										FlexMemory w/		UART/SPI	Modular Tower H/ware
72-100MHz 64-512KB										EEPROM capability		Programmable	Development System
64-144pin										SRAM	12-bit DAC	Delay Block	Application
K30 72-100MHz 64-512KB						l I				Memory Protection Unit		External Bus Interface	Software Stacks, Peripheral
64-144pin										Low Voltage,	•	Motor Control	Drivers & App.
K20 50-120MHz										Low Power Multiple Operating Modes,	Comparators	Timers	Libraries (Motor Control,
32KB-1MB 32-144pin										Clock Gating (1.71V-3.6V with 5V		eSDHC	HMI, USB)
K10										tolerant I/O)	Low-power Touch Sensing		Broad 3rd party
50-120MHz 32KB-1MB 32-144pin										DMA		RTC	ecosystem



-40 to 105C



Kinetis: Freescale Enablement Bundle

Freescale Tower System

Freescale CodeWarrior IDE

Freescale MQX RTOS

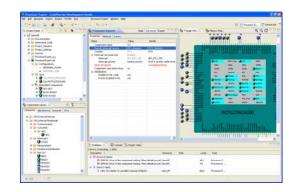
Kinetis MCU modules from \$69



- Modular, expandable, open-source h/ware development platform for 8/16/32-bit MCUs/MPUs
- Rapid evaluation and prototyping with maximum h/ware reuse
- Supported by a growing range of peripheral plug-in boards (WiFi, Sensing, Graphics LCD, Audio,...)
- www.freescale.com/tower

Open source, reusable hardware platform

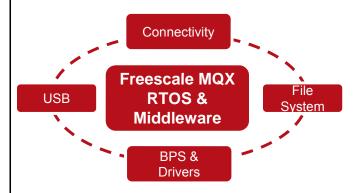
Free of charge up to 128KB



- Eclipse environment
- Includes Processor Expert code generation wizard
- Creates MQX-aware drivers
- Build, debug and flash tools
- Software analysis
- Kernel-aware debug
- Special Edition \$0 up to 128KB
- www.freescale.com/codewarrior

Powerful IDE with code generation wizard for \$0!

Free of charge (\$95K est. value)



- Full-featured, scalable, proven RTOS with TCP/IP, USB, Graphics, Security and File Systems plug-ins
- Makes application code more stable, more maintainable and easier to upgrade – reduces time-to-market!
- Compatible with CodeWarrior, IAR, Keil & Green Hills IDEs
- www.freescale.com/mqx

Bundled RTOS for \$0!

One Stop Shop for Silicon, IDE & RTOS





Kinetis Tower System: Reusable, modular development platform www.freescale.com/tower www.towergeeks/org

MCU Families Supported	TWR Part Number	Contents	Price (SRP)
K30/40	TWR-K40X256	TWR-K40X256 (144MGA), TWRPI-SLCD	\$69
	TWR-K40X256-KIT	TWR-K40X256 (144MBGA), TWRPI-SLCD TWR-SER, TWR-ELEV	\$139
	TWR-K53N512	TWR-K53N512 (144MBGA), TWRPI-SLCD	\$109
K50	TWR-K53N512-KIT	TWR-K53N512 (144MBGA), TWRPI-SLCD, TWR-SER, TWR-ELEV	\$179
	TWR-K60N512	TWR-K60N512 (144MBGA)	\$69
	TWR-K60N512-KIT	TWR-K60N512 (144MBGA), TWR-SER, TWR-ELEV	\$139
K10/20/60	TWR-K60N512-IAR	TWR-K60N512-KIT (144MBGA), TWR-PROTO, Segger J-Link Lite Debug Probe, IAR EWARM IDE (eval. version)	\$239
	TWR-K60N512-KEIL KEIL Tools by ARM	TWR-K60N512-KIT (144MBGA), UNLINK-ME Debug Probe, KEIL MDK IDE (eval. version)	\$199





TWR-SENSOR-PAK



TWR-LCD

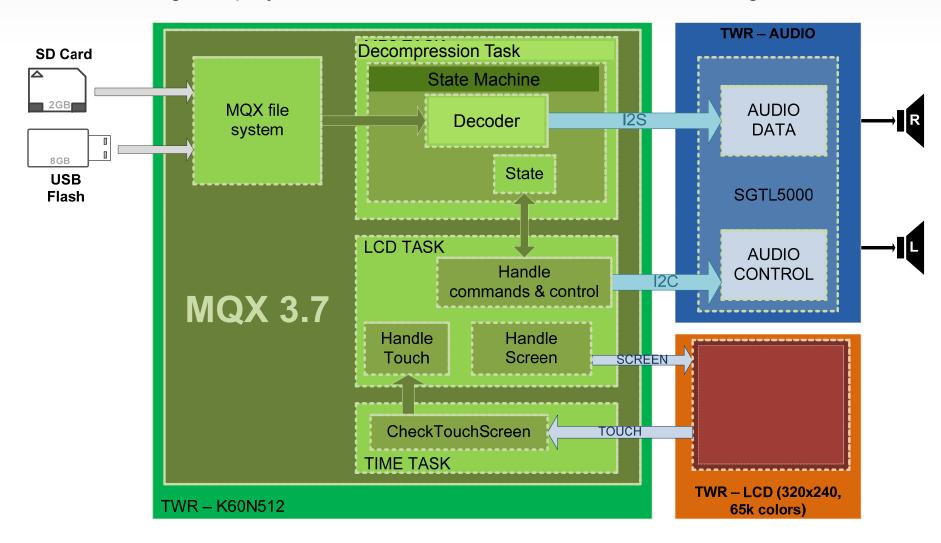


TWR-WIFI-RS2101

- IDEs: FSL CodeWarrior, IAR Embedded Workbench, Keil MDK, ...
- Freescale MQX RTOS
- OSJTAG Debug circuitry program & debug with USB cable
- Low power touch sensing & plug-in socket for expansion: Sensors, Radio, etc...
- Fully compatible with all Tower peripheral modules

Kinetis K60 Audio Player Demo: Block Diagram

S/W MP3 decoding and playback under MQX with touch screen LCD using Kinetis K60 MCU





Kinetis K60 Audio Player Demo: Screen Features of Audio Player demo

Main features:

- basic control features (play, stop, pause, play next, play previous)
- basic song information display (title, artist, album, year, name of file)
- plotting of both channels samples in a time domain
- display of actual time and current position of song
- current position change possible using slide bar moving
- volume and balance control

Spectrum Analyser:

- whole frequency spectrum (~40Hz 20kHz) is divided into16 frequency sub-bands
- display 16 frequency sub-band lines with 10 pixel resolution
- spectrum analyser is based on sub-bands data hidden in every mp3 frame
- each of sub-band line includes average value of both channels in a specific frequency band

Other:

- equalizer setting
- select from playlist



