```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.ALL;
3   USE ieee.numeric_std.ALL;
4   ENTITY data_mem IS
5   PORT(
6   clk         : IN STD_LOGIC;
7   addr        : IN UNSIGNED(7 DOWNTO 0);
8   data_in     : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
9   wen         : IN STD_LOGIC;
10  en          : IN STD_LOGIC;
11  data_out    : OUT STD_LOGIC_VECTOR(31 DOWNTO 0));
12  END data_mem;
13
14  ARCHITECTURE Description OF data_mem IS
15  -- define array type and signal to store data
16  type tmatrix is array(0 to 255) of std_logic_vector(31 downto 0);
17  signal matrix : tmatrix;
18
19  BEGIN
20  --Make it work!
21     process(clk)
22     begin
23        if falling_edge(clk) then
24
25        if en = '1' then
26           if wen = '0' then
27              data_out <= matrix(to_integer(addr));
28
29           elsif wen = '1' then
30              matrix(to_integer(addr)) <= data_in;
31              data_out <= x"00000000";
32           end if; -- conditional for wen
33        elsif en = '0' then
34           data_out <= x"00000000";
35        end if; -- conditional for en
36        end if;
37     end process;
38
39  END Description;
```